IF A/D Converters for a DSP-based FM-receiver

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Abstract

DSP-based FM receivers should be designed paying special attention to the implementation of the A/D converter. This paper overviews the available solutions for these systems by addressing advantages and drawbacks. Large emphasis is given to an implemented bandpass multibit ΣΔ modulator, deriving its specifications from system requirements, and motivating each design option. Experimental results of both a test chip and a complete receiver are provided as well.

1. Introduction

Most analog FM receiver systems use a super-heterodyne architecture, as shown in Fig. 1. The RF FM signal is shifted to a first Intermediate Frequency (IF), which is historically fixed at 10.7 MHz, in order to properly position the image component of the mixer. The signal amplitude is adjusted in gain by an Automatic Gain Control loop (AGC), to avoid saturation in the following stages. The IF signal is filtered by one or more high-selectivity ceramic or SAW filters, which attenuate undesired neighbor channels and out-of-band energy, thus reducing the system dynamic requirements. In some cases, the filter implements also the channel selection function.

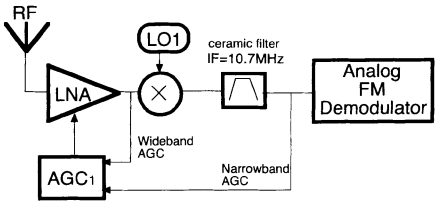

Fig. 1 – The super-heterodyne receiver architecture

Nowadays, in the wireless broadband communication scenario, the general trend aims at the software-defined radio receiver, as an answer to the request of re-configurable and multi-standard systems [[1],[2],[3]]. In such systems, the receiver is capable of modifying the digital processing depending on its configuration. The software-radio approach can be adopted for FM receivers in the automotive industry as well, where car-radios have to deal with different broadcasting standards for the three main areas (Europe, America and Japan), and the consumer

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market requires advanced functions (e.g. audio and channel equalization, and MPEG-1 Layer 3), along with the integration with multimedia devices (e.g. CD-players, phone handsets, and GPS navigation). State-of-the-art sub-micron technologies ease the design of high-frequency circuits, which can effectively digitize the IF signal; mixed-signal devices can thus be implemented, sampling the FM signal centered at the IF, and demodulating it by means of a programmable digital processor.
This work at first describes the possible architectures for an IF-sampled system, focusing on the advantages and the drawbacks of each possible solution; then, it concentrates on the definition of the specification of the selected design for the ADC; finally, the architecture and the circuit design of the A/D converter is analyzed in detail.

2. Architectures for a DSP-based FM Receiver

FM transmission systems are among the oldest standards in wireless telecommunications. The actual broadcasting FM signal is the result of an evolution, during which the amount of transmitted information has increased, though maintaining backward compatibility. As a consequence, an FM receiver does not present a set of full specifications as for recent digital communication standards (GSM, GPS, UMTS, 802.11a/b/g, etc ...). The broadcasting FM channel bandwidth is about 200 kHz and its carrier signal frequency ranges in between [88 MHz - 108 MHz].
As a consequence an FM receiver has to be designed trading among several target specifications. For instance, in crowded channel situations, the key aspect is the selectivity of the receiver (i.e. its capability of selecting the desired channel even in presence of close and powerful adjacent channels). On the other hand, in presence of coarsely spaced FM stations, with weak signal amplitude, the receiver sensitivity (i.e. its capability of processing signal with very small amplitude, with a low-noise electronics) is of primary importance. These two possible approaches are complementary: for instance high-selectivity is obtained with high-Q and noisy filters, which, on the other hand, limit the sensitivity.
Recently, the possibility of realizing DSP-based FM receiver has been investigated, and the resulting most popular architectures are the IF solution [[8],[9],[13],[14],[15],[16],[17],[18],[19]] (shown in Fig. 2) and the low IF (LIF) solution [[20],[21]] (represented in Fig. 3).
In both cases the RF front-end is assumed to be the same with a 10.7MHz-IF bandpass ceramic filter, which is intended to protect the A/D converter from strong interfering signals.
In the first architecture, the signal is digitized at the 10.7 MHz IF, and additional filtering and downconversion is performed in the digital domain. In both cases $\Sigma\Delta$ modulators are typically adopted, providing the required SNR only in the 200 kHz bandwidth of interest.

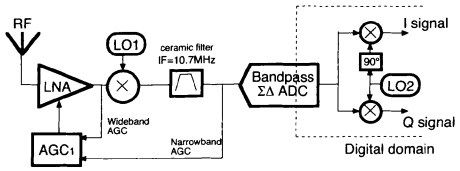


Fig. 2 – The digital-IF receiver architecture

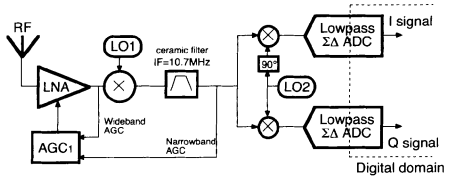


Fig. 3 – The digital-LIF receiver architecture

The second architecture is the LIF implementation; it uses an additional analog mixer to shift the signal to a lower IF before digitization; in this case, two ADCs are required to implement the image-rejection relative to the 2nd mixer.

2.1. IF-ADC approach

The direct digitization of the channel at IF with a single ADC presents the following advantages:

- the scheme uses a single digitizer (BPΣΔM), while I&Q (In-Phase & Quadrature) signals are separated in the digital domain (by means of a Cordic, for instance), guaranteeing 'infinite' matching;
- the image frequency is far from the signal frequency, therefore no image-rejection filtering is needed.

On the other hand, the digitalization of the 10.7 MHz signal requires more stringent requirements for the analog blocks (opamp, switches, oscillator, etc.....). For instance, the resulting low fs/f_{IF} ratio corresponds to have few samples for each signal period, giving large voltage steps between consecutive samples. This results in the necessity of ensuring large slew-rate capability, to avoid distortion. Similar arguments are valid also for the sampling clock jitter, which results in a DR reduction.

Regarding the possible implementations of this kind of architecture, the main alternatives reported in literature are:

- switched-capacitor (SC) technique [[8],[9],[14]–[19]]: requiring higher speed for the active devices (opamps) but less sensitive to jitter and with more stable frequency response; the eventual anti-aliasing filtering function is implemented by the external ceramic filter;
- continuous-time (CT) technique [[15],[20],[21]]: characterized by smaller bandwidth requirements for the active devices – and so less power consumption – but higher sensitivity to jitter and parameter spread, thus requiring a tuning circuit, which may affect the DR performance. On the other hand they do not need any anti-aliasing filter in front of the ADC.

The choice of the sampling frequency is an important parameter for the overall performance. According to literature, the sampling frequency can be chosen as:

- $fs/f_{IF}=4$ [[14],[16],[17]]: this allows a very efficient digital downconversion to baseband, but it may result in a DR reduction due to the folding of

the odd harmonics into the signal band. The image frequency is far from the signal frequency, therefore, no image-rejection is needed.

- $3 < f_S/f_{IF} < 4$ [[8],[15]]: the linearity performance is improved with respect to the previous case, but the demodulation requires a digital mixer circuit. As before, no image-rejection filtering is needed.
- $f_S/f_{IF} = 4/3$ [9]; this is an undersampling technique. It reduces the bandwidth for operational amplifiers, but tightens the requirements for the image-rejection filter. The digital demodulation is as efficient as for $f_S/f_{IF}=4$.

2.2. LIF & VLIF approach

This approach exploits the consideration that high linearity is achievable at low frequencies (or at large f_S/f_{IF} ratios) with relaxed requirements for the analog blocks in the ADC. A 2nd mixer stage can be used to additionally downconvert the IF signal to a lower frequency, and separate the I and Q signals, which are then processed by two ideally identical paths. The 2nd mixer can be implemented with an efficient fully-passive structure [[20],[21]]. When the IF is downconverted to dc, the system is called "zero-IF" (ZIF); when the signal is shifted few hundred kilohertz from the dc, the system is named "near-zero-IF" or "very-low-IF" (VLIF).

Also these methods have both advantages and disadvantages. In the ZIF, the baseband signal (at dc) accuracy is corrupted by the superimposition of the dc-offset (which is generated by path mismatches, and local oscillator leakage), and of the $1/f$-noise. This motivates preferring the VLIF systems. They however require a high image-rejection (IR), due to closely spaced adjacent channels, and image. The achievable IR is limited by the negative-to-positive frequency crosstalk of the in-phase and quadrature signals, determined by the path mismatch.

The Image Rejection (IR) depends on the matching of the phase/quadrature paths, and it can approximately be expressed as in (2), where $\Delta A/A$ represents the relative gain mismatch between I and Q paths, and $\Delta\phi$ is the phase error in radians [10].

$$IR = 10 \cdot \log_{10} \frac{4}{\left(\frac{\Delta A}{A}\right)^2 + (\Delta\phi)^2} \qquad (1)$$

2.3. Other implementation considerations

In the above discussion architectural issues have been addressed. However, the final performance of the receiver depends also on other parameters, more related to the particular implementation solutions adopted for the realization of the ADC. In the following sub-sections some of these parameters are introduced and their effects on the different implementation approach are compared. In this analysis literature-found silicon implementations will be considered. For the IF approach,

both SC and CT implementations are available in literature, while for the VLIF only a CT solution has been proposed.

2.3.1 ADC input impedance

The input impedance of the ADC is of primary importance in its coupling with the analog tuner front-end. For CT-ADCs, it is generally not critical, provided that proper impedance is taken into account in designing the tuner. On the other hand, when an SC-ADC is adopted, the tuner output stage is loaded by a switched-capacitor, whose value may be up to 8-10 pF. The resulting large (about 10 mA) impulsive current may decrease the front-end performance, unless the SC-ADC input stage be carefully designed.

2.3.2 Frequency response accuracy and tuning system

The accuracy of the time-constant of a CT circuit depends on the poor precision of the integrated components (with variation up to ±40% with respect to its nominal value). This motivates the use of tuning systems capable of controlling the frequency response of the CT-ΣΔM [[15],[34],[35]]. This is more necessary for the BP case (IF-ADC), while for the LP case (VLIF-ADC) is less important, but necessary as well to achieve large DR by implementing an aggressive NTF. As a drawback, state-of-the-art tuning solutions may reduce the DR due to their interaction with the CT-ΣΔM.

On the other hand, SCΣΔM are less sensitive to component spread, and thus at the first order the tuning can be avoided. As a general consideration, in both cases the use of a low-order BPΣΔM limits the useful bandwidth, thus reducing the system robustness. To fit the bandwidth even for these cases, it may be necessary to adjust the frequency response also in SC systems and, on the other hand, it may disable the adoption of CT systems.

2.3.3 Anti-Alias Filter

Before digitization, an anti-alias filter is generally required to remove the image. However, in CT-ADCs the CT-loop itself implements this function. Similarly, in a digital-IF system, the IF ceramic filter removes the alias, allowing using an SC-ADC without a dedicated image-rejection filter.

2.3.4 Sampling clock jitter

According to the study of Tao *et al.* [[11]] the sampling clock jitter sets an upper bound on the achievable dynamic range in both SC and CT converters. Eq.s (2), (3), and (4) give this upper bound for the case of SC, CT with a Non-Return-to-Zero DAC and CT with a Return-to-Zero DAC, respectively. Fig. 4 reports the dependence of the maximum DR vs. the clock jitter for the three above cases, under typical conditions.

2.3.5 Comments and Results

A summary of the characteristics of three literature found solutions, an SC and a CT for the IF approach, and a CT for the VLIF approach is reported in Table I. Up and down arrows indicate respectively advantages and weak points.

$$SNR_{SC} = 10 \cdot \log_{10}\left[\frac{\frac{f_S}{2 \cdot B}}{\left(2 \cdot \pi \cdot \Delta \cdot IF\right)^2}\right] \quad (2)$$

$$SNR_{CT\_NRZ} = 10 \cdot \log_{10}\left[\frac{\frac{f_S}{2 \cdot B} \cdot \sin c^2\left(\frac{\omega_o \cdot T_s}{2}\right)}{2 \cdot \alpha \cdot \left(\Delta \cdot IF\right)^2} \cdot \left(\frac{A}{\Lambda}\right)^2\right] \quad (3)$$

$$SNR_{CT\_RZ} = 10 \cdot \log_{10}\left[\frac{\frac{f_S}{2 \cdot B} \cdot \sin c^2\left(\frac{\omega_o \cdot T_o}{2}\right)}{\left(2 \cdot \frac{\Delta}{T_o}\right)^2} \cdot \left(\frac{A}{\Lambda}\right)^2\right] \quad (4)$$

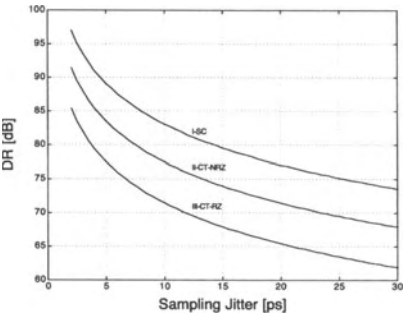


Fig. 4 - DR Sampling Jitter upper-bound

TABLE I
CHARACTERISTICS OF SOME ADC IMPLEMENTATIONS FOR FM RECEIVER (DR>78dB)

	IF-ADC (BPΣΔM)		VLIF-ADC (LPΣΔM)	
Implementation	CT [15]	SC [8]	CT [21]	
f_{IF}	10.7 MHz	10.7 MHz	300 kHz	
f_S	40 Mhz	37.05 MHz	41.6 MHz	
ΣΔM Order & Structure	Single-bit 6^{th} order BP	Multi-bit 2^{nd} order BP	Single-bit 5^{th} order LP	
Power consumption	Higher ⇓	Higher ⇓	Lower	⇑
Additional Block Req.ments				
Anti-Aliasing Filter	No ⇑	Yes ⇓	No	⇑
Image Rejection Filter	No ⇑	No ⇑	Yes	⇓
Tuning circuit	Yes ⇓	No/Yes ⇓	Yes	⇓
Sensitivity				
Clock Jitter	Yes ⇓	No ⇑	Yes	⇓
Channel mismatch (Gain and phase)	No ⇑	No ⇑	Yes	⇓
Tuning system	Yes ⇓	No ⇑	Yes	⇓
Cross Coupling Noise Sensitivity	High ⇑	Low ⇓	High	⇑

3. A DSP-based FM receiver

According to the above discussion, a DSP-based FM receiver has been developed [8]. The partitioning of the receiver is shown in Fig. 5. The car-radio system, in which the IF processor is embedded, operates under severe field conditions but it is nevertheless required to ensure high-fidelity audio quality. The chip photo is shown in Fig. 6. The device has been realized in 0.18 μm CMOS technology, using a die area of 15.2 mm^2. For this device, an SC IF-ADC has been chosen for its intrinsic robustness to process parameters spread, and to the noise of the environment. The main drawback of this choice is the power consumption larger than for the VLIF approach. However, most dissipation in a car-radio system is due

to the digital processing (hundreds milliWatts), and this makes the large power consumption of the SC-IFADC acceptable.

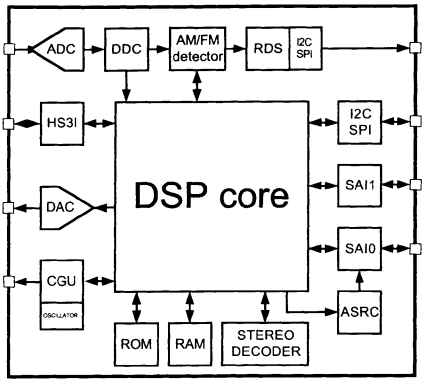


Fig. 5– Single-chip IF processor architecture.

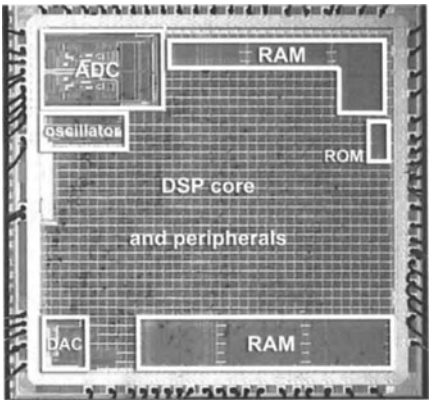


Fig. 6 – IF processor chip photograph.

4. IF-ADC dynamic range design considerations

Assessing the dynamic range (DR) of the ADC converter is a key issue in the design of the FM radio system, since it does not only determine the sensitivity of the receiver but it also establishes the specifications for the analog tuner front-end. Throughout this work, the dynamic range is defined as the ratio of the full-scale sinusoidal input signal power, to that which results in an SNR of zero over the band of interest. The case study is the superheterodyne receiver shown in Fig. 2. In the following, some design equations are derived, expressed in decibels, for assessing the AGC characteristic and the necessary ADC dynamic range, under the assumption of ideal noise-free tuner-front end.

As an effect of the AGC loop, the antenna input signal is linearly amplified by a gain, until its level is below a threshold; otherwise it is saturated. In the latter condition, the input signal to the A/D converter is chosen to be the maximum allowed in order to have the ADC still linearly operating. It results that:

$$V_{\mathrm{AGC}} + G_{\mathrm{tot}} = V_{\mathrm{AD_{max}}} \tag{5}$$

where, V_{AGC} is the AGC threshold, G_{tot} is the gain from the antenna to the ADC converter input, and V_{ADmax} is the highest input signal of the ADC for which linearity in the conversion is guaranteed.

Other design considerations can be derived in presence of both a desired and a neighbor channel, whose level is higher than the AGC threshold; the AGC attenuates both of them by the same amount, corresponding to the difference between the attenuated undesired signal level and the AGC threshold.

Anyhow, the AGC-adjusted desired signal level has to be higher than the minimum acceptable antenna level. This situation, illustrated in Fig. 7, can be expressed by :

$$V_{\mathrm{D}} - \left[V_{\mathrm{U}} - V_{\mathrm{AGC}} - A_{\mathrm{CF}}(\Delta f_0)\right] \geq V_{\mathrm{ant_{min}}} \tag{6}$$

where V_U is the undesired signal level, V_D is the desired signal level, $A_{CF}(\Delta f_o)$ is the attenuation of the ceramic filter evaluated at $f_{IF}+\Delta f_o$ relative to IF, and $V_{ant_{min}}$ is the minimum acceptable signal level from the antenna, for which the minimum acceptable SNR is achieved on the audio signal.

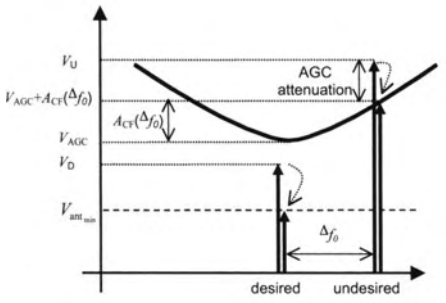


Fig. 7 - Desired/undesired signal relations used in the definition of the AGC

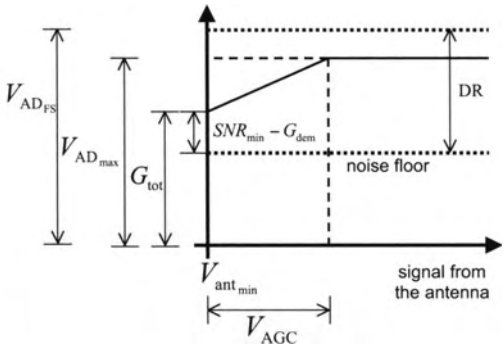


Fig. 8 - Signal levels for the receiver

From equation (3), considering the case limit, it results that:

$$(V_U - V_D)_{max} = V_{AGC} + A_{CF}(\Delta f_0) - V_{ant_{min}} \quad (7)$$

This represents the fact that the maximum difference between the undesired and the desired signal level cannot be larger than the difference between the AGC threshold, at the undesired signal frequency, and the minimum acceptable antenna signal level.

After having characterized the front-end using the previous equations, it is possible to derive the required ADC dynamic range; referring to the signal level diagram shown in Fig. 8, it can be inferred that:

$$V_{ant_{min}} + G_{tot} = (V_{AD_{FS}} - DR) + (SNR_{min} - G_{dem}) \quad (8)$$

where $V_{AD_{FS}}$ is the ADC full-scale signal level, DR is the dynamic range of the ADC, SNR_{min} is the minimum acceptable audio SNR, evaluated in a 15 kHz bandwidth for FM, and G_{dem} is the demodulation gain defined as the ratio between the signal-to-noise value at the ADC output and the audio SNR.

Eq. (5) expresses the condition that the minimum acceptable antenna signal level is amplified in order to reach a level higher than the noise floor, resulting from the A/D conversion, by the minimum acceptable SNR at the output of the A/D converter.

The combined results from equations (2), (4) and (5) are shown in TABLE II. For an FM modulated signal with a 40-kHz frequency deviation, the demodulation gain, considering also 50μs-deemphasis filtering, is about 26 dB, provided that the demodulator is operating above threshold. As a practical critical condition, a 200 kHz-off neighbor channel can be 75 dB higher with respect to the desired signal.

Typical ceramic filter attenuation at this frequency is 20 dB, relative to IF. The ADC full scale and its maximum input signal level guaranteeing linearity are chosen based on design experience. It results that the starting point of the AGC is 55 dBμV while the antenna-to-IF gain is 59 dB; the dynamic range required for the ADC to meet the system specifications results in 78 dB.
Simulations of the described radio receiver have been used to validate the proposed design methodology. Simulated audio SNR, evaluated over a bandwidth of 15 kHz, is reported in Fig. 9, in conjunction with experimental results of the implemented system. The simulated curve saturates to an unpractical 97 dB of audio SNR, while the measured is 30 dB lower; this can be explained by the fact that the tuner VCO phase noise was not modeled in the simulator, and this results to be the limiting factor in the saturation region. However, the simulation model is appropriate in the linear region.

TABLE II - DETERMINATION OF ADC DR

Description	Symbol	Unit	Value
Specifications			
Maximum undesired/desired ratio for SNR_{min}	$(V_U - V_D)_{max}$	dB	75
ADC maximum level input for linearity	$V_{AD_{max}}$	dBμV	114
Minimum acceptable antenna signal level	$V_{ant_{min}}$	dBμV	0
Minimum audio SNR	SNR_{min}	dB	40
Demodulation gain	G_{dem}	dB	26
Ceramic filter relative attenuation at Δf	$A_{CF}(\Delta f_0)$	dB	20
ADC full scale	$V_{AD_{FS}}$	dBμV	123
DESIGN VARIABLES			
AGC threshold	V_{AGC}	dB	55
Gain from antenna to ADC input	G_{tot}	dB	59
ADC dynamic range	DR	dB	78

In Fig. 10, the power spectra of the signals at various stages of the system prove that the AGC characteristic, derived from equations (2) and (4), allows handling undesired signals higher than the desired up to 75 dB. The interferer does not decrease the audio SNR since the desired is still recognizable at the ADC output, as imposed by equation (4), and because the undesired is completely removed by the channel filtering.

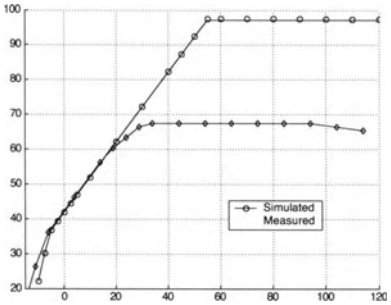


Fig. 9 - Audio SNR evaluated over 15 kHz bandwidth, for 1kHz mono signal using 40 kHz frequency deviation, in function of the tuner input signal level.

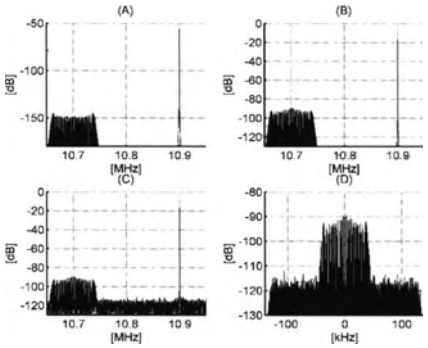


Fig. 10 - Simulated power: (A) ideal tuner input signal, (B) signal at ADC input, (C) signal after A/D conversion, (D) complex baseband signal. Desired singnal has 40 kHz deviation, while the interferer is an unmodulated carrier.

5. The Bandpass ΣΔ Modulator

The technological trend toward scaled-down device sizes is a key issue for the realization of single-chip systems, which include both analog and digital parts. While for the digital blocks the scaled down technologies allow a reduction in area and power consumption, for the analog sections the relatively poor analog performance of the scaled MOS devices results in a considerable design challenge, which makes it difficult to achieve the performance previously obtained with larger minimum size device. This motivates the research of novel architectures for the mixed signal blocks (like ADCs, DACs, etc.....), which take advantage of the improved digital circuitry in order to compensate for the poorer analog circuitry.
The IF-ADC, embedded in the presented DSP-based FM receiver, is a BandPass ΣΔ Modulator (BPΣΔM). The following key choices characterize the proposed device:

- use of a SC implementation to guarantee performance robustness versus clock jitter;
- use of a 2^{nd}-order modulator (the minimum order for a pure BP solution) to reduce the amount of analog circuitry, and so the analog penalty;
- use of a single opamp for the realization of the 2^{nd}-order loop filter (resonator), to reduce power consumption
- use of a multibit (33-level) quantizer to increase the relatively low Dynamic Range (DR) of the 2nd-order modulator and, in addition, to improve system stability
- use of a bandpass Dynamic Element Matching (DEM) technique to linearize the multibit feedback DAC;
- use of a self-calibrating system to increase the accuracy of the Noise Transfer Function (NTF) notch bandwidth position (fo) and depth (Q), in order to avoid DR losses;

- use of an input switched-buffer to reduce input impulsive current sunk from the previous block driving the BPΣΔM.

Further details on these choices are given in the following sections.

5.1. The BPΣΔM Architecture

The adopted BPΣΔM architecture is shown in Fig. 11. The fundamental blocks are: the input switched buffer, the bandpass loop filter, the 33-level quantizer, and the multibit feedback DAC with DEM circuitry. In addition a dither signal is generated and injected in the signal path. Finally the NTF *fo* and *Q* are adjusted with two dedicated control systems.

In the architecture of the FM receiver of Fig. 2, the BPΣΔM input signal is the output signal either of the analog mixer or of the ceramic. The BPΣΔM input switched-capacitor, being some pFs large under low-noise and robust design considerations, generates large input current spikes, which are detrimental to the performance of the previous block. For this reason a high-performance switched-buffer has been conceived, that significantly reduces the amplitude of current spikes at the input.

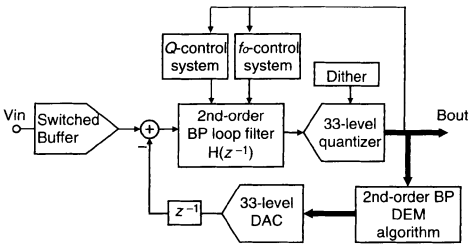


Fig. 11 - The adopted overall BPΣΔM architecture

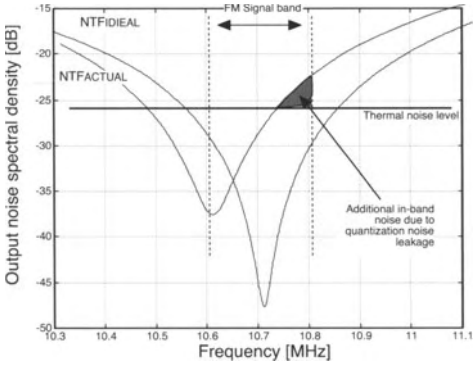


Fig. 12 - Output spectrum with NTF error

Regarding the BPΣΔM, a 2nd-order structure has been adopted, since it presents the minimum amount of analog components for the realization of a "true" bandpass system. Previous solutions use single-bit higher order modulators to achieve similar performances, however they suffer from the stability issue, which force reductions in the DR.

Thus, a 33-level quantizer is adopted. The multibit quantizer gives 6dB SNR–improvement for each extra bit, and increases the system stability. This is also important in order to implement a more aggressive noise shaping, which improves the accuracy. In addition, the multibit quantizer linear behavior reduces the spurious-tones typically present in 1st-order structures. However, for very low-level signals, the multibit quantizer operates as a single bit quantizer. This results in the relatively poor performance of the 2nd-order BPΣΔM (which corresponds to a 1st-order single-bit low-pass modulator). To reduce this weakness, a digital dither

signal at *fs*/4, with amplitude of a single LSB, is added to the quantizer output. Such a dither is necessary, since the noise shaping could be lost at low signal levels, resulting in a significant DR loss.
The main problem for using a 33-level quantizer is the linearity requirement of the feedback DAC. Since it is in the feedback loop, its accuracy needs to be at least as good as the converter resolution in order not to deteriorate the BPΣΔM performance. Several solutions to relax the linearity requirements have been proposed in literature. In this design, the linearity is ensured by means of a DEM algorithm, which implements a 2^{nd}-order bandpass noise shaping algorithm.
On the other hand, the use of 2^{nd}-order loop filter gives a NTF notch bandwidth (~300kHz), which is slightly larger than the FM signal bandwidth (~200kHz) centered at 10.7MHz. This arrangement reduces the DR losses, which occur with a misadjusted notch location or bandwidth (as shown in Fig. 12), which can be due for instance to a 0.5% capacitor mismatch, to a 200MHz opamp bandwidth, and to a gain lower than 80dB. These requirements cannot be relaxed in order to achieve high yield in mass-production. Thus, performance robustness is guaranteed also by means of two calibration algorithms, which control the frequency (*fo*) and the quality factor (*Q*) of the NTF zeros.

5.2. Switched buffer

The switched-capacitor (SC) circuits in the sampling structure of Fig. 13.a (where a superlinear switch [12] is assumed to be used), due to their sampled-data nature, operate with large transients, which correspond to large input current spikes. The amplitude of these current spikes depends on the size of the capacitor, on the conductance ($1/R_{on}$) of the switches, and on the signal amplitude.

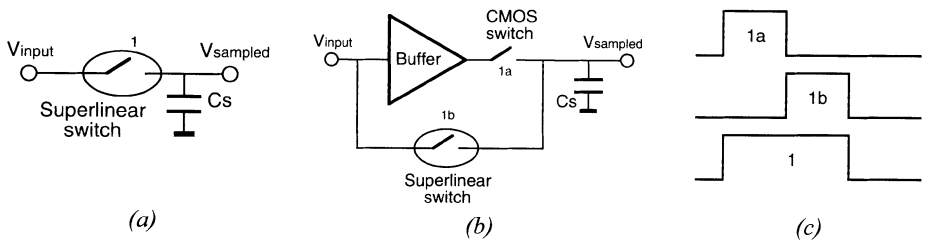
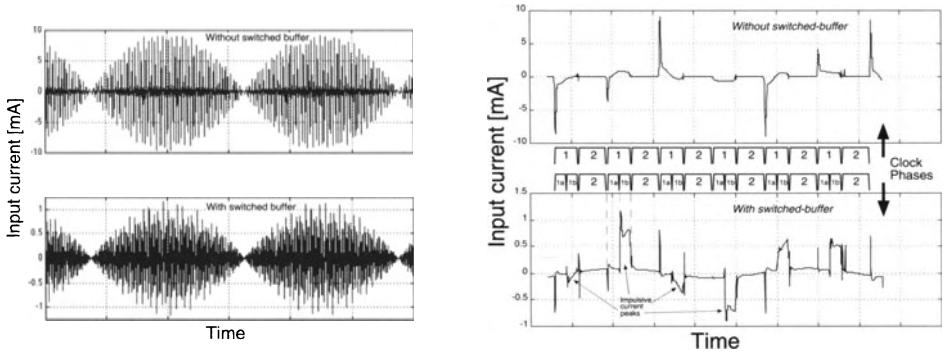


Fig. 13 - Two possible input branch solutions

The plot at the top of Fig. 14.a shows the input current required by the BPΣΔM (with a 5.8 pF input capacitance) for full-scale input signal amplitude (4 V_{pp}) with a standard SC input branch of Fig. 13.a. The input current spikes, even in the presence of the real series switches, are large up to 10 mA and they may deteriorate the performance of the previous stage that has to source them. A more detailed view is given in Fig. 14.b where the upper plot shows the current amplitude during the different clock phases. A first level solution to reduce these spike effects is to insert a buffer, which is always connected to the previous stage

and drives the input SC-branch. In this way, the previous stage is loaded with constant (i.e. non-switched) impedance and, thus, it is not required to source current spikes. This solution is expensive in terms of area and power consumption. In fact, the input buffer must exhibit high-quality performance in order not to deteriorate the modulator performance in terms of frequency response, noise, and linearity. Therefore, the buffer has to exhibit a large gain and unity-gain bandwidth in order to guarantee an accurate sampling operation. In addition, the contribution of the input buffer to the sampled voltage in terms of noise and distortion must be minimized. This can be achieved at the cost of large area and power consumption. It should be noted that bandwidth, noise, and linearity are not critical if the standard un-buffered passive SC structure of Fig. 13.a is used.



(a) overall waveform *(b) detail of the waveform*

Fig. 14 – Comparison of the input current for the two solutions

In the proposed design, a switched buffer [[8]], shown in Fig. 13.b, has been adopted. The sampling phase (1) of the standard scheme of Fig. 13.a is divided in two parts as shown in in Fig. 13.c (1a and 1b):

- in the first part (1a) an active buffer (always connected to the input voltage) pre-charges the sampling capacitor Cs to a voltage close to the input voltage and, in particular, it reduces the level of the input current spikes, which are larger during the initial part of the sampling phase;
- in the second part (1b), the active buffer is disconnected from sampling capacitor and the final settling is achieved with a standard passive switch (superlinear in this implementation), which ensures high linearity, low noise and large bandwidth.

This solution is advantageous for the following reasons:

- the active buffer is not required to have high-speed response, since the final value is fixed by the switch performance;
- the accuracy of the transition between the two phases 1a and 1b of the switched buffer is not critical: thus their generation can be very simple and with a small overhead;

- the capacitor is pre-charged to a value close to the final one. This is more efficient than in [[31]], in which the capacitor is pre-charged to the previous sample. This approach could be not only ineffective but also dangerous in our case due to the small ratio f_s/f_o;
- the level of the current spikes is reduced by 85%.

A further optimization [[29]] of the complete switched-buffer is possible in order to pre-charge the capacitance internal to the superlinear switch with the same buffer, avoiding the supplementary load, which is typically applied to the input signal source.

The effectiveness of the proposed solution can be appreciated from Fig. 14.a and Fig. 14.b, where it is compared to the standard solution. For the switched buffer a single stage CMOS opamp with 6 mA current consumption is adopted. The bottom plot of Fig. 14.a shows the impulsive input current for the switched-buffer for the overall input waveform. The current spikes are limited to a maximum value of about 1.2 mA, which is a factor of about 8 times lower than the standard solution (the input current is 0.19 mA_{rms} and 0.76 mA_{rms} respectively, for the solution with and without the switched–buffer). A detailed view of this behavior is given in Fig. 14.b. It can be observed that for each phase there are two current spikes corresponding to the edge of the phases 1a and 1b. At the begining of phase 1a, the spike is due to the current necessary for the buffer capacitance, while the current spike at the beginning of phase 1b is due to the charging of the sampling capacitor. The above simulation shows the achievable large reduction of the input current spikes, which allows different stages to be coupled together without deteriorating their stand-alone performance.

5.3. Loop Filter Design

The 2^{nd}-order BP loop filter is realized using SC technique, operating with a 37.05 MHz sampling frequency. This value has been chosen since it is a multiple of frequencies available in the system (the 57 kHz RDS carrier and the 50 kHz VCO tuning frequency step). Fig. 15 and Fig. 16 show the architecture and the SC implementation of the BPΣΔM, respectively.

A single time-shared opamp for 2^{nd} order resonator is used. This solution results in a 35–40% power saving with respect to the two-opamps solution. This is also slightly area effective since the opamp area is much smaller than the capacitor area (see chip photo in Fig. 18). On the other hand, in the single opamp solution, two critical switches have been added in series with the two integration capacitors (C_B, C_D in Fig. 16). These switches are connected to the output node in order not to corrupt the charge conservation at the virtual ground node. However, according to this, their conductances depend on the signal amplitude. Thus, super-linear switches are used in order to prevent degradation of the SNDR performance. With the single opamp solution the layout design requires attention to avoid path crossing between the different connections to the virtual ground, which would result in parasitic charge transfers during the two different integration phases.

A linearity improvement (of about 10dB in IMD) has been experimentally obtained by sampling the input signal with capacitor C_{in1} toward ground instead than towards a virtual ground, whose accuracy depends on the opamp bandwidth performance.

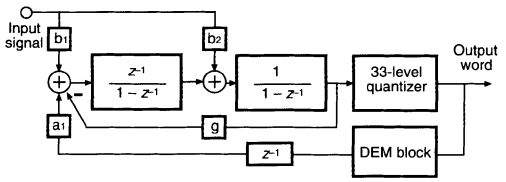


Fig. 15 - Modulator architecture

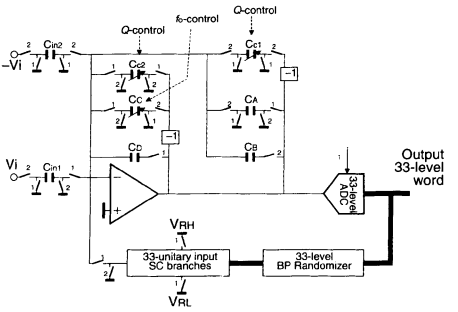


Fig. 16 - Single-opamp structure SC implementations of the BPΣΔM

The BPΣΔM implements the following loop filter transfer function (H), the Signal Transfer Function (STF) and the Noise Transfer Function (NTF), under the assumption of ideal performance for the analog parts of the BPΣΔM:

$$H(z^{-1}) = \frac{z^{-1}}{z^{-2} + 0.4827 \cdot z^{-1} + 1} \tag{9}$$

$$STF(z^{-1}) = \frac{z^{-1}}{0.4827 \cdot z^{-1} + 1} \tag{10}$$

$$NTF(z^{-1}) = \frac{z^{-2} + 0.4827 \cdot z^{-1} + 1}{0.4827 \cdot z^{-1} + 1} \tag{11}$$

5.4. The f_o and Q Calibration Block Design

In a BPΣΔM several non-idealities (mainly the capacitor mismatch and the opamp finite gain and bandwidth) cause a displacement of the NTF zeros from their nominal position. Therefore, even though an SC implementation has been used, a calibration system for the positioning of the NTF zeros has to be adopted [[28]] to guarantee performance robustness even in production. The nature of the mentioned sources of inaccuracy with respect to the required precision makes ineffective the use of master-slave calibration structures [[34],[35]] (which are based on component matching). Instead a two-step self-calibration approach has been used in the device:

- in the first step the resonator quality factor (Q) is increased in order to guarantee a certain depth in the NTF notch
- in the second step the notch frequency (f_o) is adjusted at the center of the signal band.

Notice that the Q-tuning is not strictly necessary for the modulator performance (thermal noise is dominating quantization noise in the signal band) but it is needed

to guarantee the proper working of the f_o-tuning algorithm. The calibration algorithms are based on the fact that the nominal loop filter transfer function $H(z^{-1})$ (and, as a consequence, the loop filter nominal transient response to an input impulse) is known *a priori*. So the modulator structure can be reconfigured in order to measure some specific parameters in its transient response, which are correlated to its frequency response. In both the calibration algorithms, the BPΣΔM is reconfigured by turning off the feedback DAC. A very-simple training signal (a one clock cycle impulse) is applied at the input of the loop filter (operating without the feedback DAC, i.e. as a resonator). The number of the zero-crossings with respect to a given threshold at the output of the loop filter is counted in the digital part and compared to its nominal value. This solution is convenient for two reasons: for the natural presence of the quantizer at the loop filter output and for the simplicity of the training signal. The elaboration of the number of zero-crossings allows to adjust the loop filter frequency response by setting the value of parameters C_{C1} and C_{C2} (responsible for Q-factor) and C_C (responsible for f_o).

The Q-factor calibration block is designed to maintain the Q-factor at a level above a certain value. This is done by adding a SC positive feedback (C_{C1} and C_{C2}) on both integrators. This positive feedback is accurately controlled by the algorithm, in order to avoid system instability. In this way the algorithm prevents the Q-factor from exceeding a given value. The capacitor ratios C_{C1}/C_B and C_{C2}/C_D have to be very small (in the range of 0.016-0.8), and they cannot be realized directly using a single capacitor. In fact, C_{C1} and C_{C2} have to range between fractions of one fF to several fFs. Since in the adopted technology the minimum feasible capacitor is 50 fF, a digitally programmable T-network has been adopted.

The f_o calibration block is used to move the center frequency by changing the resonator feedback capacitor C_C, which is realized with a 15-capacitor array controlled by the f_o control algorithm, with a minimum step of 21 fF.

These calibration procedures allow the NTF notch frequency f_o to be set with a resolution of 40 kHz, which meets the application requirements. The digital calibration circuitry requires a maximum time of 28,800 time slots (i.e. less than 0.8 ms) and occupies an area as small as about 3.5 kgates in the 0.18 μm technology.

Such a proposed self-calibration procedure disables the signal processing, so it has to be executed according to the timing of the overall system in which the BPΣΔM is embedded.

5.5. Analog Block Design

The minimum feasible capacitor size for a robust design in the adopted technology is 50fF, which has been applied as the minimum capacitor in the f_o and Q calibration circuits. As a consequence, the BPΣΔM capacitors result to be the following: C_A=2pF, C_B=1.12pF, C_C=7.94pF, C_D=5.7pF, C_{C1}=3.2pF, C_{C2}=3.2pF, C_{in1}=3.19pF. The unitary-element capacitor in the feedback DAC is 100fF. Notice that, in order to optimize the opamp performance, the capacitive load and the

feedback factor have been maintained constant in both the opamp operating phases. With the above values, the opamp load is up to 15pF. This makes the thermal noise of the switches (kT/C) negligible with respect to the opamp noise. The capacitive loading and the following considerations make the design of the opamp of key importance. The opamp has to exhibit:

- low noise (to match the DR requirement)
- high speed (to settle in half a period of the sampling frequency)
- high gain (to reduce the integrator phase error)
- high slew rate (to reduce distortion and to properly 'jump' in the single opamp configuration)
- high output swing ($4V_{pp}$ differentials from a 3.3V power supply).

The class AB single stage output boosting structure, shown in Fig. 17 [[32],[33]] has been used. The input stage devices operate in the sub-threshold region in order to achieve a large transconductance. An eventual large offset may be sustained by the bandpass application.

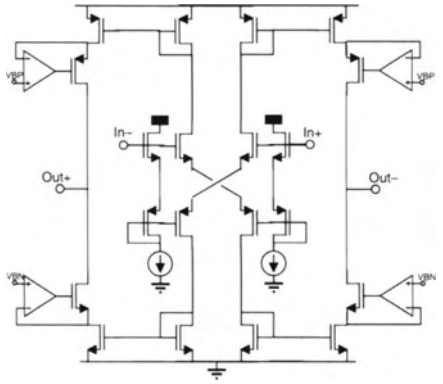


Fig. 17 - The opamp schematic

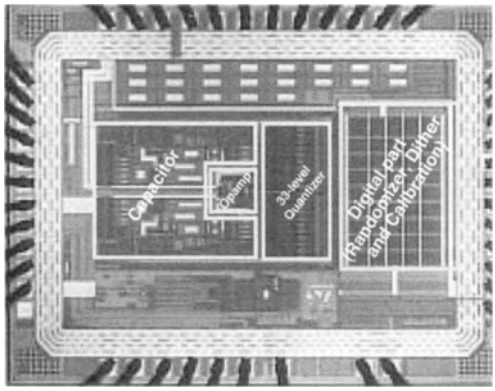


Fig. 18 - Chip photograph

The typical open loop opamp performance (taking into account the feedback factor) is: DC-gain=112 dB, unity-gain bandwidth=350 MHz, current consumption=17.6 mA. This nominal opamp performance does not require any calibration, however in technological worst case conditions it still requires the use of f_o and Q tuning circuits.

The 33-level quantizer is realized with a flash architecture. The number of levels is relatively high in order to increase linear range and DR. The case of the digital output word with all 0's corresponds to no unit elements being selected and does not require any DEM algorithm. Thus the DEM is applied to a 32 levels. Each level is selected by a comparator, which is the cascade of an auto-zero SC amplifier, to avoid kick-back noise, and a latch. The reference levels are

implemented with two resistive strings. Finally, the 33-level quantizer total current consumption is 4.5 mA from a 3.3 V supply.

5.6. Experimental results

The proposed BPΣΔMs have been integrated in a 0.18 μm CMOS technology, which features two oxide thicknesses. This makes available two MOS devices: a 0.18 μm CMOS with a 1.8 V maximum supply and a 0.35 μm CMOS with a 3.3 V maximum supply. The technology features 6 metal levels and high-linearity metal-metal capacitor. The device has been realized in a test-chip, where the clock is supplied by an external signal generator, and also embedded within a complete fully-integrated mixed-signal FM receiver. In the latter case the clock is generated on-chip by a 3rd overtone quartz oscillator, which guarantees a better jitter performance (lower than 10 ps_{rms}). Fig. 18 shows the chip photograph of the device in the stand-alone version. The die active area is about 1mm^2. In the photo the different parts of the device have been indicated. The large portion of the area is dedicated for capacitors and calibration blocks, which makes the opamp area relatively negligible. In the realized device the current consumption of the analog part is 22 mA from 3.3 V, while the digital part consumes 8.5 mA from 1.8 V. In addition, the eventual use of the switched-buffer requires a 12 mA additional current.

The experimental results have been obtained with a dither signal, which can be clearly seen in the output spectrum at $f_s/4$. The effect of the dither is a DR improvement of about 2dB with respect to the case when the dither is turned-off. Fig. 19 shows the output spectrum for a –20dBFS input signal in the passband. Similar performance has been obtained for the test chip and in the complete receiver. In addition, in the receiver where the switched-buffer can be enabled, similar performance is also achieved with and without the switched-buffer, which is then demonstrated not to be the limiting block. The corresponding SNR vs. input amplitude is shown in Fig. 20 for the FM (200 kHz) bandwidth. For all of the versions a considerable DR and SNR_{peak} are achieved. A minimum SNR_{peak} of 67 dB is performed in the test-chip version, while for the receiver version it is larger than 70 dB, and reaches 72 dB activating the switched-buffer.

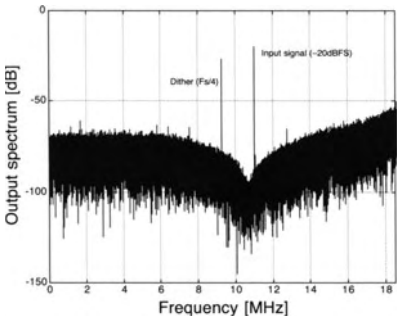


Fig. 19 - Output spectrum @ –20 dBFS input

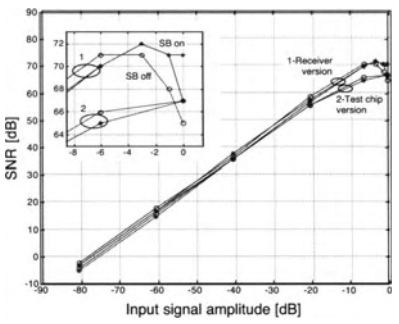


Fig. 20 - SNR vs. input signal amplitude

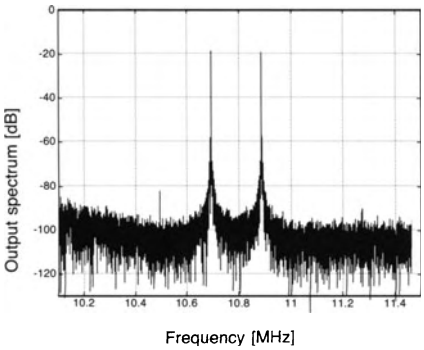


Fig. 21 - IMD measurement

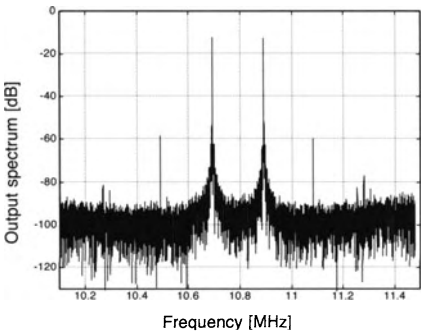


Fig. 22 - IMD measurement with DEM algorithm turned off

The DR is better for the receiver version (a minimum value of 78 dB is achieved in production, with some samples featuring up to 81 dB), in spite of the noisy environment, due to the better jitter of the on-chip quartz oscillator. This indicates that the external clock jitter is the limiting factor of the test-chip version. This is also valid for the SNR-peak as shown in the magnified inset within Fig. 20. Regarding the effect of the switched-buffer, it results in a 1 dB DR loss, which is negligible for the application. On the other hand, the switched-buffer becomes effective for large signals, i.e. it gives a 1dB SNR-peak improvement, as can be seen in the magnified inset. If the inputs are shorted on-chip (mute state), the DR (mute-DR) moves to 80 dB for the FM band and 95dB for the AM band. Moreover, a DR improvement has been observed by reducing the sampling frequency. Using f_s=35 MHz the mute-DR is larger than 95 dB (for FM band) and this is within 1dB of the MATLAB simulated value. For this reason, the limiting factor could be the opamp finite speed of response (bandwidth and/or slew-rate).

The linearity of the modulator has been evaluated with a two-tone intermodulation (IMD) test (f_1=10.71 MHz, f_2=10.77 MHz). For two tones at –11 dBFS, the IMD is about –65 dBc (as shown in Fig. 21).

The effect of the DEM can be seen in the IMD measurement. The output spectrum with the DEM algorithm turned off is given in Fig. 22, where a larger IMD can be observed. The DEM gives an IMD improvement of about 19 dB. Table III summarises features and performance.

Finally the effect of the calibration system can be seen in Fig. 23.

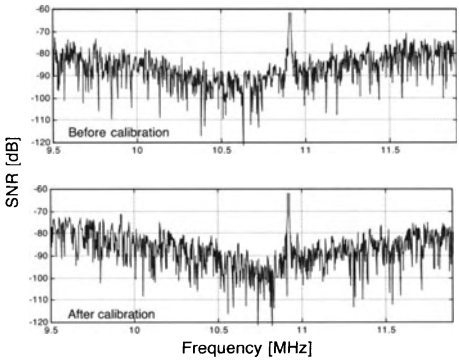


Fig. 23 - Output spectrum before and after calibration

The curve on top refers to the uncalibrated case: an error in the notch frequency of about 150kHz is present (>1% error). The bottom curve corresponds to the calibrated case. The notch frequency is centered at its nominal value and this gives a 3dB SNR improvement. This demonstrates that even in the presence of significant technology spread and opamp performance loss, the BPΣΔM exhibits the maximum achievable performance in the signal band.

6. Conclusions

A 2^{nd}-order multibit BPΣΔM has been realized both in a stand-alone test-chip and also embedded in a complete fully-integrated mixed-signal FM receiver which generates a noisy environment. In the final application solution (the receiver version with the switched-buffer on), the modulator features 78dB DR, 72dB peak-SNR within a 200kHz bandwidth (FM bandwidth) with a 84 mW power consumption. The IMD for a –11dBFS two tones test is about –65dBc. These experimental results demonstrate the validity of the proposed design especially in terms of performance robustness, since they have been achieved when the BPΣΔM is embedded in a complete FM receiver.

TABLE III - BPΣΔM PERFORMANCE SUMMARY

Parameter	Value
f_s/f_0	37.05MHz/10.7MHz
Signal bandwidth	200kHz (FM)
OSR	92.6 (FM)
Architecture	Single-loop
Modulator order	2^{nd}
Input full-scale	4Vpp
Technology	CMOS 0.18μm @ 1.8V 0.35μm @ 3.3V
Active die area	1mm^2
Test chip (FM band)	DR = 76 dB
Switched-buffer OFF	IMD (–11dBFS) = –65 dBc
Full receiver (FM band)	DR = 78 dB
Switched-buffer OFF	IMD (–11dBFS) = –62 dBc
Full receiver (FM band)	DR = 78 dB
Switched-buffer ON	IMD (–11dBFS) = –65 dBc
Mute-DR	80dB (FM bandwidth) 95dB (AM bandwidth)
Power consumption	88 mW

7. Aknowledgments

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system evaluation, S. Galantin, and M. Tonella for the applications, F.A. Mancuso, P. Mastromatteo and P. Volontieri for analog layout, and M. Porta and his team for top-level assembly and back-end.

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