ANALOGUE-TO-DIGITAL CONVERSION TECHNIQUES

by Julian Nolan

The rapid growth in the digital sector of the electronics market has given rise to continued demands for more and more increases in the resolution and conversion speed of digital-to-analogue and analogue-to-digital converters. In spite of the industry meeting these demands, the selling price of all types of device has continued to fall. This is particularly true for medium speed/resolution flash devices: an 8-bit, 30 MHz type, for instance, is now available in quantity for well under £20. Advances in the digital-to-analogue converter field have been typified by higher specifications rather than lower prices.

Three main analogue-to-digital (A-D) conversion techniques are in common use: successive approximation, flash and integrating conversion.

Successive approximation has the advantage that for an n-bit converter only n number of stages are necessary in the successive approximation register (SAR), which makes this technique ideal for applications that require high resolution or low cost or both. The technique is illustrated in Fig. 1.

Initially, all output bits of the SAR are set to zero and then each bit, starting with the most significant, is set provisionally to one. If the output of the converter does not exceed the input signal voltage, the bit is left at one, otherwise it is reset to zero. From this, it is clear that an n-bit converter will require only n such conversion steps. This makes this type of converter relatively fast in comparison with those that use other techniques like single- or dual-slope integration.

Should the input voltage be altered during the conversion process, the resulting error will be no larger than the change during that time. Noise spikes, however, can cause totally erroneous output and must be avoided at all costs.

In general, it is advisable to use a sample-and-hold device in conjunction with this type of converter.

Typical conversion times range from 1 µs to 50 µs, while accuracies of 8–16 bits are available.

Flash conversion requires 2^n-1 comparators, thus limiting the resolution that can be achieved with this technique. Current IC fabrication technology permits up to 12 bits.

Two typical flash devices are Analog Devices' AD770 (8 bits at 200 MSPS) and TDC1020 (10 bits at 20 MSPS).

The technology relies more on 'force in numbers' than subtle design techniques at component level. As shown in Fig. 2, a reference voltage is applied to a resistive divider, whose equi-spaced outputs are applied to $n-1$ voltage comparators. The Gray-code output from the comparators is encoded by the priority encoder to form a usable binary output. Typical conversion rates vary from 10 MSPS to 500 MSPS, while resolutions of up to 12 bits are currently available.

Resolutions above 16 bits are generally the domain of integrating converters. These offer good linearity and resolutiuon while maintaining a reasonable cost/performance ratio. Typical applications include digital voltmeters, data acquisition systems, weighing and medical systems where the slow conversion rate inherent in these converters is not significant. An example of integrating conversion, dual slope, is shown in Fig. 3.

Initially, switch S1 is closed by the control logic. Switch S4 is then opened and the input voltage integrated for n clock periods, where n is usually the maximum count of the counter. At the end of this time, the integrator voltage, V_o, is

$$V_o = -V_{in} n T_c / RC \qquad [1]$$

where T_c is the clock period.

During this period, the polarity of the

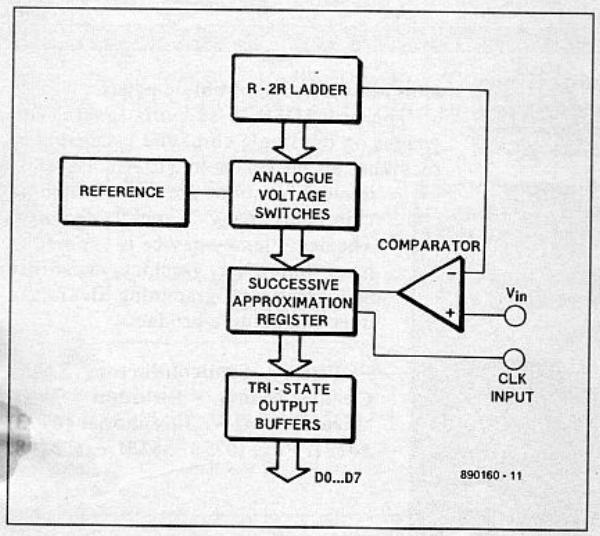

Fig. 1

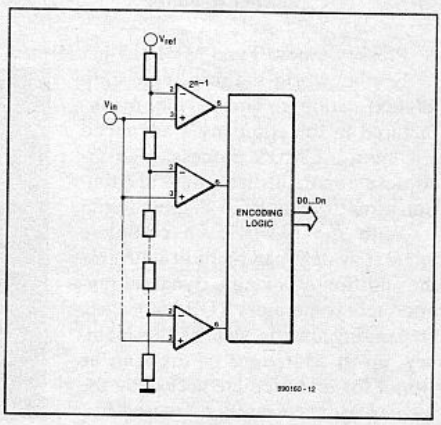

Fig. 2

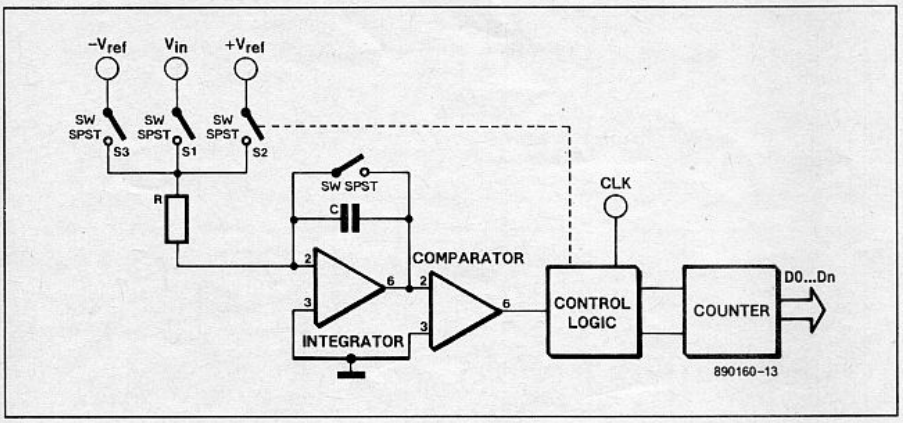

Fig. 3

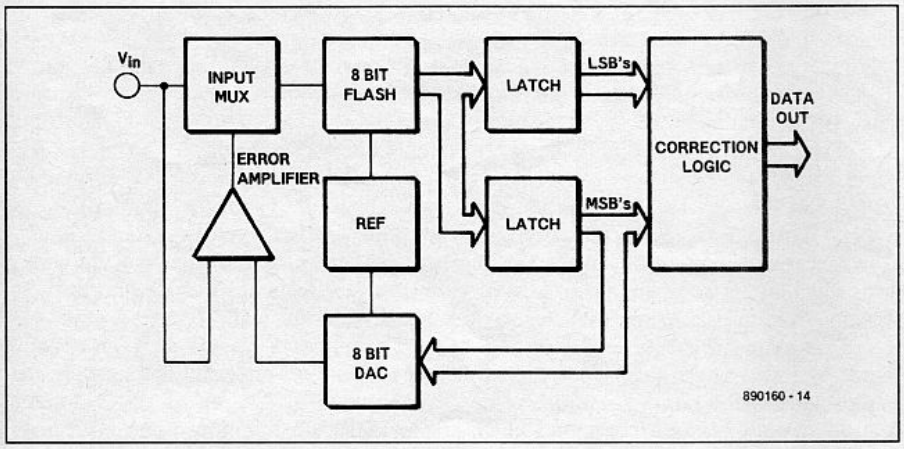

Fig. 4

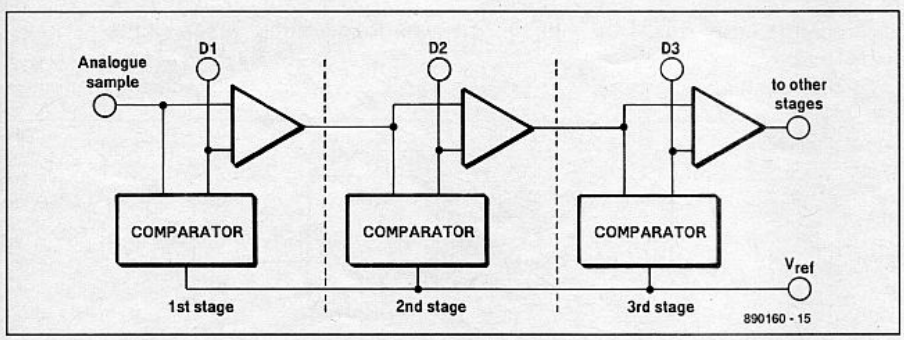

Fig. 5

input signal is detected by the comparator. At the end of the integration period, S1 is opened and, depending on the polarity of V_{in}, either S2 or S3 is closed to connect the integrator to the reference voltage that has a polarity opposite to that of V_{in}. Next, the counter is clocked from zero until the integrator output reaches 0 V: the output of the comparator then changes state and the count is stopped. Since integration takes place over the voltage range V_o,

$$V_o = -V_{ref} n_x / RC, \qquad [2]$$

where n_x is the count reached by the time the integrator output passes zero.

Combining and rearranging [1] and [2] gives

$$n_x = V_{in} / V_{ref} \qquad [3]$$

Since n and V_{ref} are both fixed, the output count is directly proportional to the input voltage. Because both the first and the second integration occur under identical circumstances, the converter is not affected by any long-term variations in T_c, R or C, as confirmed by the disappearance of these terms from equation [3].

The major factors affecting the stability of the converter are:

(1) the stability of V_{ref};
(2) drift in integrator and comparator opamps;
(3) the stability of the 'on' resistance of S1 and S3.

Other techniques of integrating conversion are available, such as single-slope integration and charge balancing. These methods are relatively slow, however, and their use is restricted to applications that can support their relatively high conversion times.

As is seen, none of the three methods discussed provides both a high resolution and a high conversion speed. Where these are required in combination, say, 16 bits at 2 µs, use is made of subranging techniques, which are normally based on a single high-speed flash A-D converter as shown in Fig. 4.

In practice, these types of device are implemented in hybrid form. Some suffer from a reduced signal-to-quantization noise ratio at relatively high input frequencies, although those are not uncommon in A-D converters.

Initially, the input is sampled by the track and hold circuit. Subsequently, the most significant portion of the signal is converted by feeding the output word into a fast, highly accurate D-A converter, whose output is subtracted from the input. The resulting residue is converted to digital form at high speed and combined with the results of the earlier conversion to form the output word. Owing to the very high performance this technique demands from the adder and DAC, it is usual to incorporate some sort of error correction: a commonly encountered type is digitally corrected subranging (DCS). In this, the two bytes are combined in a manner that corrects the error of the LSB of the most significant byte. With the use of, for instance, an 8 and 5 bit conversion, an accuracte, high-speed 12-bit converter may be configured, although it should be noted that the resolution of the D-A converter must be greater than the resolution required to maintain conversion accuracy.

Future developments

Digital error correction, using a variety of techniques, from integrating to subranging, is now being introduced into a wide range of devices. This trend is likely to continue and, with the ever decreasing cost of data conversion products, will become increasingly relevant to the low-cost end of the market.

As regards conversion techniques, the serial converter or cascaded encoder as shown in Fig. 5 may well make a come back. First used in the 1960s as a method of A-D conversion, the serial converter is based on a number of comparators, each taking the residue of the previous stage and comparing it to a reference voltage. If the input is higher than the reference, a 1 is produced at the output, and the residue of the original input signal is subtracted

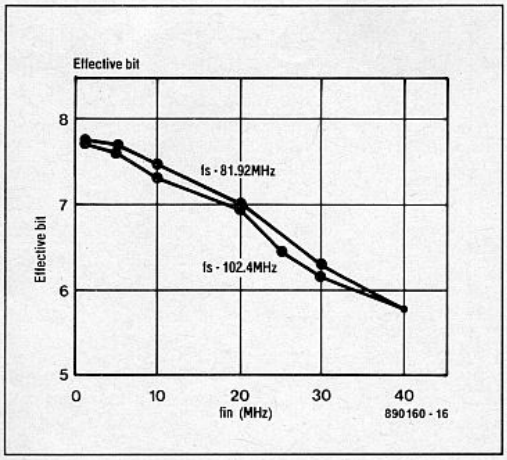

Fig. 6

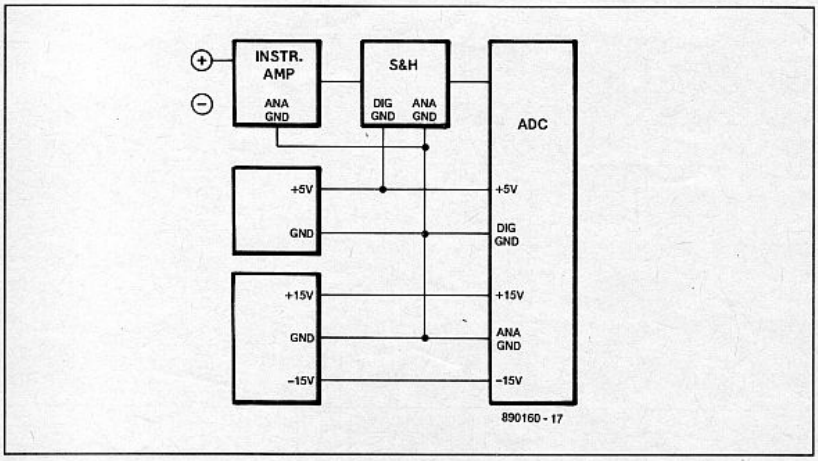

Fig. 7

from the reference and passed on to the next stage. If the input does not exceed the reference, the signal is passed to the next stage unaltered. It is usual to incorporate a ×2 amplifier to enable the use of a single reference voltage and restrict problems with noise.

In practice, this system has provided difficult to implement owing to errors introduced by the comparators and amplifiers, noise and also poor transfer characteristics in high-speed systems. With the advent of high-performance analogue components, however, some manufacturers are reconsidering this technique, since it offers a unique blend of speed, resolution, and low component count – at least in theory.

Design considerations

The effective resolution at a specified input frequency is usually not quoted in the manufacturers' data sheets and can often be well below the stated optimum. A graph of the SNR/effective number of bits vs the input frequency of an 8 bit, 100 MHz sampling A-D converter with a bandwidth of 40 MHz from a well-known manufacturer is shown in Fig. 6.

It is seen that at an input of 40 MHz and a sampling rate of 102.4 MHz, the effective resolution is about 6 bits. That means that only 64 possible output states are provided instead of the 256 that would have been available if the full 8-bit resolution had been maintained.

For applications that require a specified resolution to be maintained over the greater part of the input frequency, it is well worth considering, in situations that are not cost critical, over-specifying the AD converter to meet the requirement.

Although problems are evident in AD converter applications below 12 bits, most occur with accuracies of 12 bits or more, or with high-speed systems, where the problems are accentuated at higher resolutions.

If successive approximation is chosen for the A-D conversion, a sample-and-hold stage is essential and this may be a source of trouble in itself. Increasingly, however, some manufacturers, such as Datel in their 12-bit, 500 kHz ADS-111, are incorporating a S&H in the A-D converter package. However, there may be advantages, such as a reduction in cost or an improved specification, in using a separate S&H stage.

Three main building blocks are contained in a S&H stage: a capacitor, an analogue switch and a buffer amplifier. Some require an external hold capacitor, which must be chosen with great care as regards its dielectric absorption properties. Teflon or polystyrene capacitors, whose dielectric absorption is fairly small, are well suited to this purpose.

If the sampling system is used as the front end in an FFT system, particular attention should be paid to the aperture uncertainty and aperture time. The time should be chosen so that at the highest frequency the component does not change by more than one bit in the allotted time. It should also be noted that the S&H will always add errors to the A-D converter owing to effects such as non-linearity of the S&H off-set.

The use of a sin gle package containing the AD converter and the S&H has the advantages that some of the problems mentioned are minimized and noise may be less of a problem, especially in high-resolution systems.

Apart from the Datel device already mentioned, some other single-package units are the Sipex HS9474 and Analog Devices AD1332 (which includes an anti-

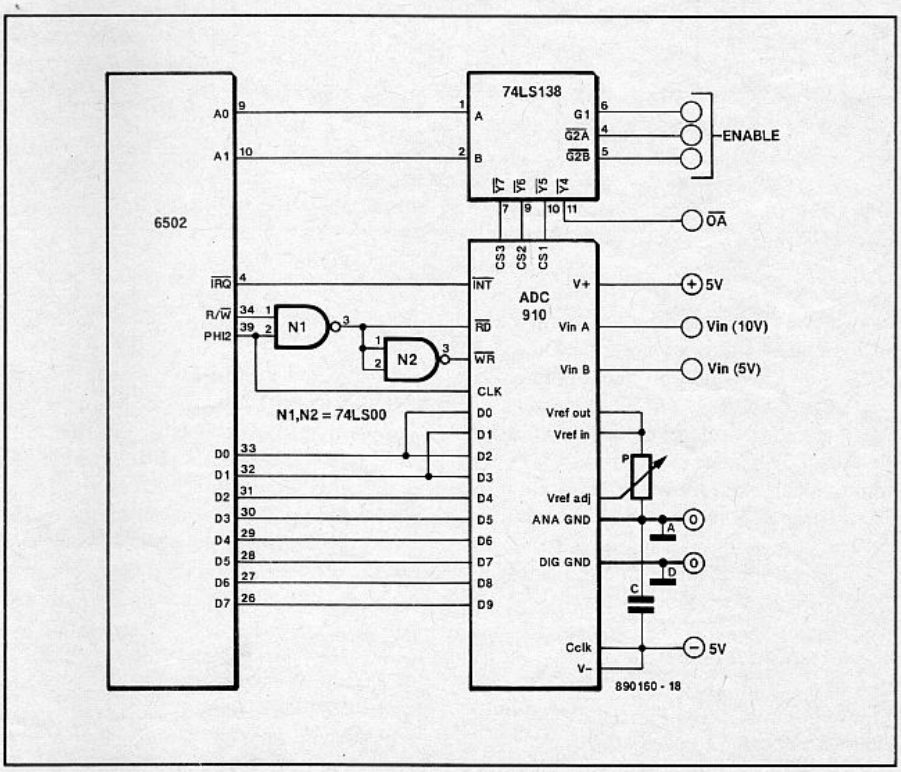

Fig. 8

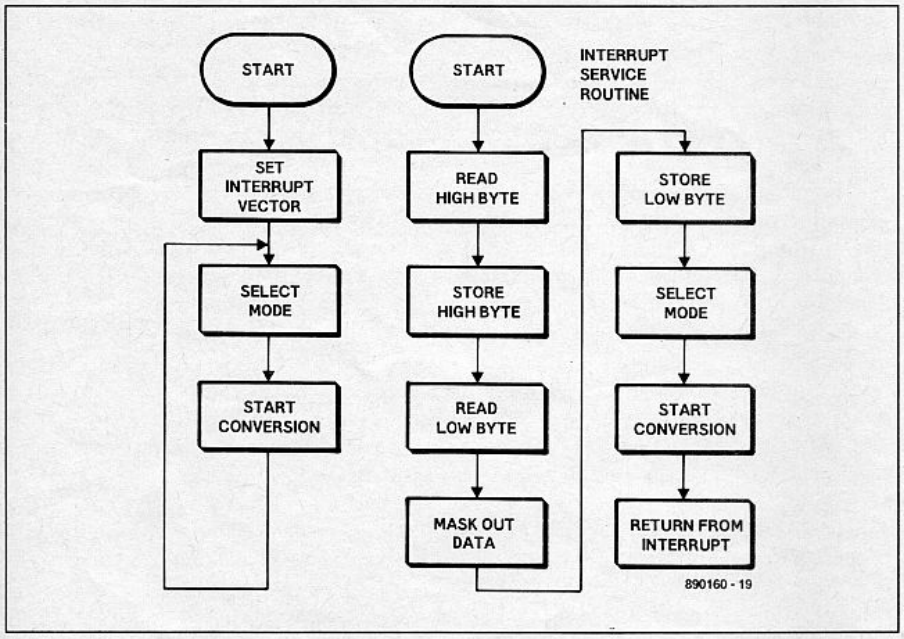

Fig. 9

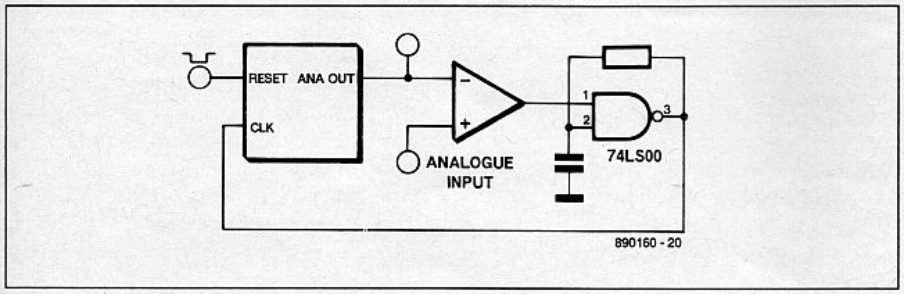

Fig. 10

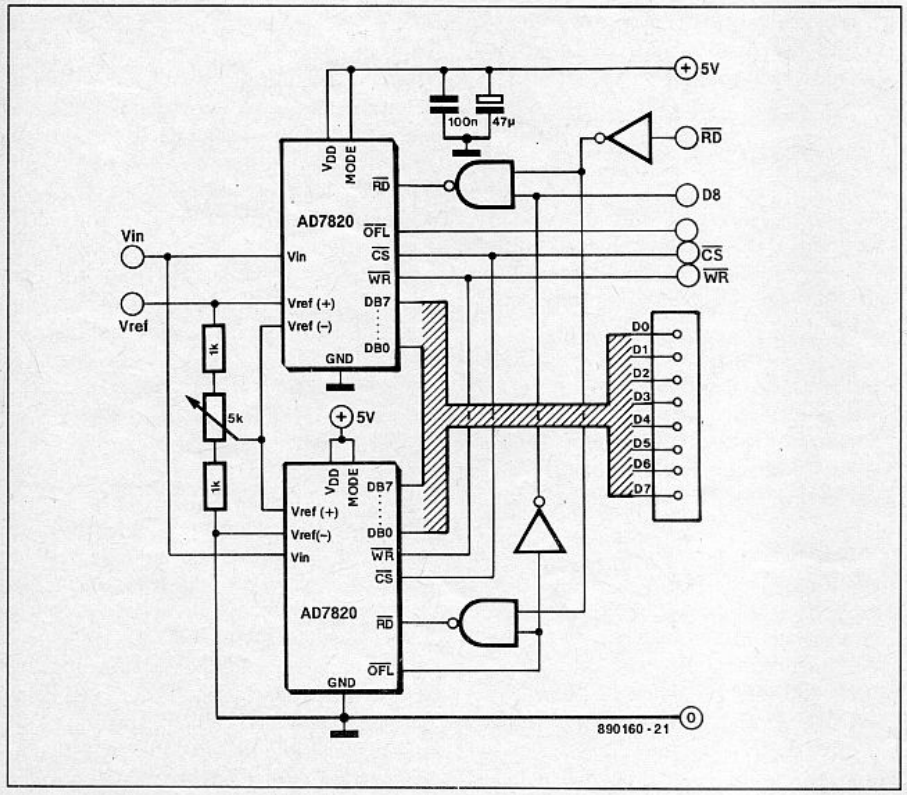

Fig. 11

aliasing filter).

Whatever technique is used, the analogue input section is vital to the operation of the converter, and usually includes one or more references in addition to conversion technique specific components like comparators and DA converters.

In ratiometric conversion, the reference is usually external and variable. In general, an on-chip reference usually helps to minimize noise, but in a number of cases advantages may be obtained from an external reference.

It is worth noting that the current-switching action of the D-A converter, at the typically fast clock rates used in successive approximation converters, may disturb the output of the analogue signal source, especially if it is a high-precision opamp.with a low slew rate. In that case, buffering will be necessary.

Design techniques

Whereas digital circuits may have noise margins of a few hundred millivolts, there is no room whatsoever for noise in analogue circuits. For instance, a 12-bit resolution A-D converter with a full-scale range of 3 V has a 0.5 LSB corresponding to 0.61 mV.

Power supplies are among the major sources of noise: the output of switch-mode types may have a noise level of more than 100 mV. Although the ability of an A-D converter to suppress DC supply changes, such as long-term drift (expressed as the power supply rejection ratio – PSRR), is usually good, HF noise is normally not suppressed to any great extent. Wherever possible, the supply voltages for the analogue section should be provided by a linear supply and bypasssed direct at the A-D converter. A multi-layer capacitor in parallel with a tantalum capacitor provides a suitable bypass.

To avoid ground loops, it is advantageous to have a 'star point' as close to the AD converter as possible – see Fig. 7. All ground lines should be of low impedance, necessitating wide ground tracks on the PCB or, preferably, particularly if double-sided or multi-layer boards are used, a separate ground plane underneath the AD converter package. In some cases, shielding the converter package from the top may be necessary.

Unless the analogue signal is free of noise, there is little point in taking the protective measures mentioned. To reduce the noise, suitable filters and shielded cables should be used.

Applications

Some of the factors worth considering when choosing an A-D converter for a particular application are:

- type of converter;
- required conversion speed;
- required resolution;
- cost-to-performance ratio;
- accuracy required;
- interface requirements;
- power requirements;
- physical dimensions.

The applications of A-D converters are numerous and have increased at almost the same rate as their performance. Common applications include, among others, data acquisition, measurement systems, analytical and medical systems, and filter control. A typical application: an A-D convertor-to-microprocessor interface, here between a PMI ADC-9012 and a 6502, is shown in Fig. 8. The circuit is fairly straightforward, except that the two LSBs are connected to data bits DB2 and DB3. The ADC-9012, a 10-bit 6 µs converter, makes special provision for this. A suitable interrupt service routine flow diagram is shown in Fig. 9.

Peak detection is one field of applications not usually associated with A-D converters, but it has become feasible with Ferranti's 8-bit converter Type ZN425E, which has an 8-bit counter on board.

The circuit diagram of a basic implementation of this is shown in Fig. 10 – note that only a small number of external components is required. The comparator enables pulses from the trigger circuit to be clocked by the internal counter and this produces a ramp output until it attains the level of the analogue input. Although rather inaccurate in this particular configuration, the circuit can be readily modified by the use of higher resolution A-D converters.

The AD7820 is a 1.36 µs, 8-bit microprocessor compatible A-D converter that has the advantage of not requiring user trims. The circuit shown in Fig. 11 enables a 9-bit resolution to be obtained by the use of two of these devices: full microprocessor interfacing is provided. Usually, this type of circuit is of limited application, because of its significantly increased chip count and cost if increases in resolution of more than a few bits are required. Nevertheless, this type of configuration is still worth considering in applications where either the cost or availability of a more conventional single-package solution would prove prohibitive.

References

Data Conversion Products Handbook – Analog Devices, 1988.

Data Converters and Reference ICs – Ferranti Semiconductors, 1986.

Data Conversion Handbook – PMI, 1988; Datel, 1988; Sipex 1988.