A Low-cost A/D Converter

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This simple, useful circuit employs "current mirrors" instead of conventional op amps

MORE and more digital techniques are finding applications in formerly exclusive domains of analog electronics-tests and measurements, communications, and the recording and reproduction of speech and music, to name a few. One necessary stage in any digital system that processes information originating in analog form is the analog-to-digital or A/D converter. In this article, we will present a low-cost A/D converter that you can build using readily available parts. The circuit can be used to experiment with the conversion of voltages, currents, and transduced physical quantities from analog into digital form.

About the Circuit. The A/D converter circuit, as shown in the schematic, employs a 12-bit CMOS counter and an LM3900 quad operational amplifier. Each of the op amps in an LM3900 IC employs the concept of a "current mirror" to amplify differential signals. They are known as Norton current-differencing amplifiers (CDAs) and are shown schematically as containing current 'sources to distinguish them from conventional operational amplifiers. Among the advantages of Norton CDAs are circuit simplicity, low cost, and the requirement of only a single-ended power supply from which each amplifier sinks a constant current independent of the supply voltage.

Stage ***ICIA*** generates a train of pulses whose duration is determined by the values of ***R5*** and Cl. The frequency of the pulse train can be varied by adjusting potentiometer ***RI.*** Pulses generated by ICI ***A*** are applied to the noninverting input of ICIB. This Norton CDA is employed as an integrator which generates a staircase waveform. The staircase increases in amplitude as pulses are received from ***ICIA.*** It is applied to the inverting input of comparator ICI C.

The analog input signal is applied to the noninverting input of this comparator. As long as the staircase amplitude is less than that of the input signal, the output of comparator ICI C remains at +V, the positive supply voltage. The staircase continues to increase in amplitude until it just exceeds the input signal's amplitude, at which point the differential input current at ICI C becomes negative. This causes the output of the comparator to go to ground potential, and the resulting negative transition is capacitively coupled to the inverting input of comparator ***ICID.***

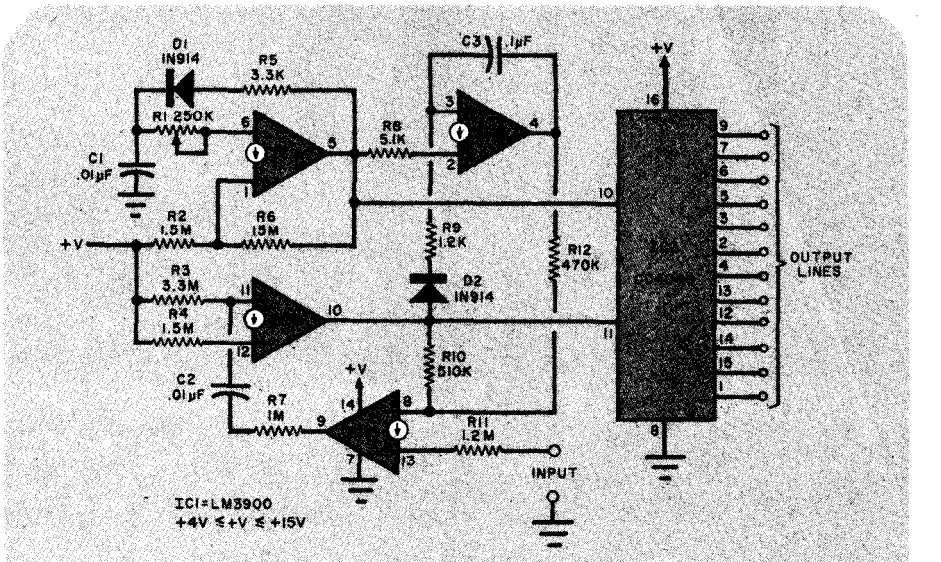
The negative pulse momentarily toggles the output of ***ICID*** from its normal (ground) state to the positive supply voltage. The resulting positive pulse resets both integrator ***ICIB*** and counter IC2, causing the output lines of the counter and the output of the integrator (that is, the staircase waveform) to go to ground potential. The process begins all over again as new pulses are generated by ***IC1A*** and applied to the integrator and counter.

In operation, the amplitude of the staircase waveform is continuously compared to the analog input signal. If the input is a constant dc level, the staircase increases to a certain amplitude during each cycle until integrator IC1 ***B*** is reset by ICI ***D.*** Similarly, IC2 will count up to a certain binary number and then be reset. If the input waveform changes with time, the amplitude attained by the staircase and the magnitude of the binary count generated by IC2 just before the reset pulse is applied will vary. Accordingly, the larger the input signal, the greater the amplitude of the staircase and the count at the output lines of IC2 at the instant before the reset pulse causes the outputs of ***ICIB*** and IC2 to go to ground. The smaller the input signal, the lower the amplitude of the staircase and count of IC2 at the instant before the reset command takes effect. The highest count attained by IC2 be-

fore the output lines are reset to zero describes the amplitude of the analog input signal at the instant that comparator ICI C changes states.

Because Norton CDAs are employed, only a single-ended power supply is needed. National Semiconductor, the manufacturer of the LM3900, states in its data sheet that a supply delivering from +4 to +36 volts can be used to power the chip. The power supply rating project. Also, use the minimum amount of heat and solder consistent with the formation of good connections. Before applying any supply voltages, double check your wiring for errors that might cause damage to the ICs.

To calibrate the circuit, connect its input to the positive supply voltage. Then monitor the output lines of IC2 and adjust ***RI*** for the desired weighting factor. This factor ***n*** will equal N_C di-



Schematic of the converter. The Norton CDAs are shown as containing current sources to distinguish them from standard op amps.

PARTS LIST

C1,C2—0.01-μF disc ceramic, silver mica or polystyrene capacitor
C3—0.1-μF disc ceramic, silver mica or polystyrene capacitor
D1,D2—1N914 diode
IC1—LM3900 quad Norton CDA
IC2—CD4040 counter
R1—250,000-ohm, linear-taper trimmer potentiometer
The following are ¼-watt, 5% tolerance, carbon-composition resistors.
R2,R4—1.5 megohms
R3—3.3 megohms
R5—3300 ohms
R6—15 megohms
R7—1 megohm
R8—5100 ohms
R9—1200 ohms
R10—510,000 ohms
R11—1.2 megohms
R12—470,000 ohms
Misc.—Printed circuit or perforated board, IC sockets, suitable power supply and enclosure, hookup wire, hardware, etc.

of the CD4040 CMOS counter is + 1 to + 15 volts. Accordingly, a supply furnishing a voltage greater than or equal to +4 volts and less than or equal to + 15 volts can be used to power the entire circuit. Current demand is modest, so either a battery or small, well-filtered, line-powered supply is suitable.

Construction. Printed-circuit, point-to-point wiring, or wrapped-wire assembly techniques can be used to reproduce the analog-to-digital converter circuit. The use of IC sockets is recommended, and the standard precautions for the handling of CMOS devices should be employed with respect to IC2. Be sure to observe the polarities and pin basings of the semiconductors employed in this

vided by + ***V*** where + ***V*** is the positive supply voltage, N_C is the highest count attained by IC2 before it is reset, and ***n*** is the number of counts per volt.

This low-cost A/D converter can be used to gain hands-on experience with one type of A/D conversion. It can also form the nucleus of some useful projects. For instance, a latch, decoder, driver and display network can be added to provide a seven-segment readout of the digital numbers generated by IC2. One interesting application would be a digital current meter that can be made by adding, such a display network and by eliminating ***RI 1.*** This can then in turn be converted into a high-impedance (as much as 10 megohms) digital voltmeter. 0