ODDS 'N' ENDS *(Continued from earlier issues)*

by James Bryant

TIME REFERENCES *(continued from 26-1—AA-11)*

Q. Why do you say that the clock of a system is a reference?

A. This comment does not necessarily apply to the conversion clock of an ADC; it applies principally to the sampling clock of a sampled-data system. In these systems, the signal is required to be sampled repeatedly at predictable (usually equal) intervals for storage, communication, computational analysis, or other types of processing. The quality of the sampling clock is a system-performance-limiting factor.

Q. But crystal oscillators are very stable, aren't they?

A. They have good long-term stability, but they are often used in ways which introduce short-term phase noise. Phase noise is also introduced by designers who, instead of using crystal oscillators, use R-C relaxation oscillators (such as the 555 or the 4046)—which have a great deal of phase noise.

Q. How can I ensure that my sampling clock has low phase noise?

A. Don't use the crystal oscillator circuitry in your microprocessor or DSP processor as the source of your sampling clock. If at all possible, do not use a logic gate in a crystal oscillator. Crystal oscillators made with logic gates generally overdrive the crystal; this is bad for its long term stability, and usually introduces worse phase noise than would a simple transistor oscillator. In addition, digital noise from the processor—or from other gates in the package if a logic gate is used as an oscillator—will appear as phase noise on the oscillator output.

Q. But crystal oscillators are very stable, aren't they?

A. Ideally, use a single transistor or FET as your crystal oscillator and buffer it with a logic gate. This logic gate, and the oscillator itself, should have a well-decoupled supply; the other gates in the package should not be used because logic noise from them will phase-modulate the signal. (They may be used for dc applications but not for fast-switching operations.)

If there is a divider between the crystal oscillator and the sampling clock input of the various ADCs, the divider power supply should be decoupled separately from the system logic to keep power supply noise from phase-modulating the clock.

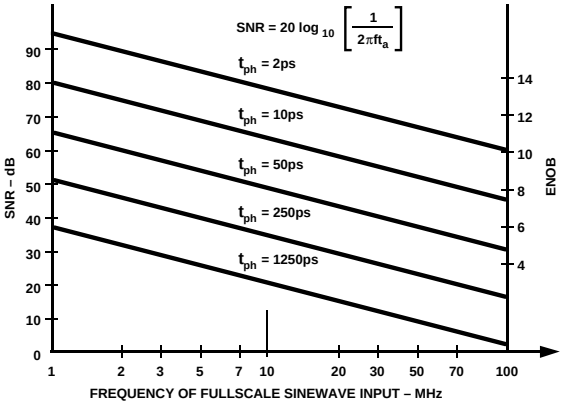
The sampling clock line should be kept away from all logic signals to prevent pickup from introducing phase noise. Equally, it should be kept away from low-level analog signals lest it corrupt them.

Q. You have told me not to use the clock oscillator of my processor as the sampling clock source. Why not? Isn't it sensible to use the same oscillator for both, since there will then be a constant phase relationship between the signals?

A. True. But in such cases, it is often better to use a single discrete low-noise oscillator to drive the processor clock input and the sampling clock divider *through separate buffers* (though they may share a package) than to use the oscillator in the processor. In medium-accuracy systems with low sampling rates it may be possible to use the processor's internal oscillator—but check with the diagram below).

Q. Just how serious is this problem of noise on a sampling clock? I hardly ever see it mentioned in articles on sampled data systems.

A. The phase noise of the sampling clock is often ignored, because the limiting factor on system performance used to be the aperture jitter of the of the sample-hold—but if we consider the system as a whole, aperture jitter is just one component of the total phase noise in the sampling clock chain. With modern sampling ADCs the aperture jitter may be less important than other components of phase noise.



The diagram shows the effect of the total phase jitter of the sampling clock on signal-to-noise ratio (SNR) or effective number of bits (ENOB). This jitter has the rms value of t_{ph}, which is made up of the root-sum-of-squares of the phase jitter on the sampling clock oscillator, the phase jitter introduced by pickup during transmission of the sampling clock through the system, and the aperture jitter of the SHA in the sampling ADC. This diagram may be somewhat unsettling, as it shows just how little phase noise is required to corrupt a high-resolution sampled-data system.

MORE ON TRIMMING

Q. I don't have enough range to adjust the offset of my circuit—and it seems to have rather more drift than I'd expected.

A. I'll bet the amplifier is a bipolar type and you are using its offset-trim terminals to trim other circuit voltages.

Q. How did you guess?

A. The range of offset adjustment of an op amp is normally 2 to 5 times the maximum expected offset of the lowest grade of the device (in some early op amps, it was much larger, but such a wide range is not ideal). If the lowest grade has a V_{OS} (max) of ±1 mV, then the likely adjustment range with the recommended circuit is ±2 to ±5 mV.

If the external voltage you are attempting to compensate for is larger than this (referred to the op amp's input), you will not be able to do so with the amplifier's offset-trim terminals.

Furthermore, if you are using a *bipolar-input* op amp, it is inadvisable to use these terminals for external offset correction because drift will be increased. Here's why: the input stage thermal drift is proportional to the internal offset; if this has been trimmed to a minimum, the drift will also be a minimum. If you then trim the amplifier to compensate for an external offset, drift will no longer be minimized. However, *FET-input* op amps have separately trimmed offset and drift, their offset adjustment terminals may thus be used for small system adjustments.