



PERFECT TIMING: PERFORMING CLOCK DIVISION WITH JITTER AND PHASE-NOISE MEASUREMENTS

AS CLOCK SPEEDS AND COMMUNICATION CHANNELS OPERATE AT EVER-HIGHER FREQUENCIES, ACCURATE JITTER AND PHASE-NOISE MEASUREMENTS BECOME MORE IMPORTANT, EVEN AS THEY BECOME MORE DIFFICULT AND EXPENSIVE TO MANAGE. SOME PRACTICAL POINTERS AND OBSERVATIONS ASSIST IN HANDLING THESE PROBLEMS.

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When measuring ultra-low-jitter devices and equipment, engineers must constantly ask whether the measurement values are from the DUT (device under test) or from the test equipment. Engineers are also always looking for methods of expanding the reach of the equipment at hand. This article describes some practical ways to handle situations in which clock signals have been divided down from higher-frequency VCOs (voltage-controlled oscillators).

IMAGE: THINKSTOCK

Most modern equipment that measures jitter can be placed into one of two broad categories: time domain or frequency domain. Time-domain equipment typically comes in the form of a high-speed digital oscilloscope with high single-shot sampling bandwidth. Frequency-domain equipment usually comes in the form of a spectrum analyzer, a spectrum analyzer with phase-noise measurement capability, or a phase-noise analyzer. Each of these two categories of equipment has its own set of advantages and disadvantages. However, both measure the same phenomena, albeit with different approaches.

Peak cycle-to-cycle jitter is the maximum difference between consecutive, adjacent clock periods over a fixed number of cycles—typically, 1000 or 10,000. It is used whenever there is a need to limit the size of a sudden jump in frequency. For example, when driving a PLL (phase-locked loop), you may want to limit the size of an instantaneous change in frequency to ensure that downstream PLLs remain in lock (**Reference 1** and **Figure 1**).

The peak-to-peak period jitter is the difference between the largest clock period and the smallest clock period for all clock periods within an observation window—again, typically 1000 or 10,000 cycles (**Figure 2**). It is a useful specification for guaranteeing the setup-and-hold time of flip-flops in digital systems. “Peak-to-peak” refers to the difference between the smallest and the largest sampled period value during a measurement.

TIE (time-interval-error) jitter, or accumulated jitter—also known as phase jitter—is the actual deviation from the ideal clock period over all clock periods (**Figure 3**). It includes jit-

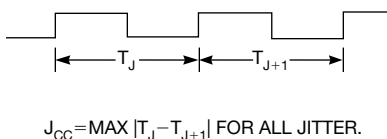


Figure 1 When driving a PLL (phase-locked loop), you may want to limit the size of an instantaneous change in frequency to ensure that downstream PLLs remain in lock.

AT A GLANCE

Time-domain equipment is better than frequency-domain systems at measuring data-dependent jitter, making it useful for high-speed serial links that use SERDES (serializer/deserializer) technology.

High-quality frequency-domain instruments have lower noise floors than their time-domain counterparts, making frequency-domain units the instruments of choice for ultra-low-phase-noise clock-signal measurements that are free of data-dependent jitter.

An instrument's noise floor can become the limiting factor of a measurement of phase noise of very-low-jitter clocks at low clock frequencies.

ter at all jitter-modulation frequencies and commonly finds use in WAN (wide-area-network) timing applications, such as SONET (synchronous optical network), synchronous Ethernet, and OTN (optical-transport networking).

You can create various types of statistics, such as rms (root-mean-square), peak-to-peak, cycle-to-cycle, period, and TIE jitter, although some are more

commonly used than others. Whenever peak-to-peak statistics are used, the number of samples taken must be large enough to produce confidence in the measurement. Such measurements typically include 1000 to 10,000 samples.

Time-domain equipment can directly measure peak-to-peak, cycle-to-cycle, period, and TIE jitter. This measurement approach permits the measurement of jitter for low-frequency clock, or carrier, signals. By employing FFTs (fast Fourier transforms), digital filters, and other techniques to postprocess the data, you can integrate the phase-noise value over a band of frequencies to generate rms-phase-jitter values. Time-domain equipment is better than frequency-domain systems at measuring data-dependent jitter, making it useful for high-speed serial links that use SERDES (serializer/deserializer) technology.

Frequency-domain equipment cannot directly measure peak-to-peak, cycle-to-cycle, or period jitter; its native ability is to measure the rms power of a signal in a given frequency band. Frequency-domain equipment is also awkward for measuring data-dependent jitter. However, high-quality frequency-domain instruments have lower noise floors than their time-domain coun-

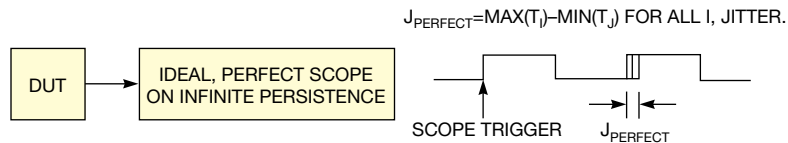


Figure 2 The peak-to-peak period jitter is the difference between the largest clock period and the smallest clock period for all clock periods within an observation window—typically 1000 or 10,000 cycles.

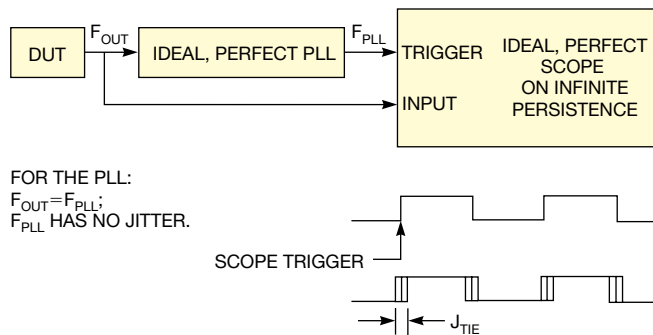


Figure 3 TIE jitter is the actual deviation from the ideal clock period over all clock periods.

terparts, making frequency-domain units the instruments of choice for ultra-low-phase-noise clock-signal measurements that are free of data-dependent jitter (**Table 1**).

Because this article focuses on the measurement of low-jitter clock signals, it omits further discussion of time-domain equipment except to mention that you can use various mathematical-estimation and -translation approaches to go from one type of jitter measurement to another. For example, it is possible to use a crest factor and a desired BER (bit-error rate) to go back and forth between peak-to-peak and rms jitter. Another example is using an FFT of time-domain data to provide frequency-domain information and filtering. However, most of these techniques rely on mathematical models, which may be good approximations in most situations but have limitations. As such, you should use them only carefully.

One issue that bears further investigation is the effect of clock, or carrier, frequency on the jitter measurement. It is intuitive that a clock signal divided down by an ideal divider will have the same clock edge jitter at both its input and output (**Figure 4**). In the **figure**, the top jittered signal with frequency F_0 is divided by two using a perfect divider to produce a clock frequency of $F_0/2$. Both clock signals have the same jitter, J_0 . Note that the jitter energy of the lower clock signal is half that of the higher clock signal because there are half as many edges in a given interval of time.

The intuition that J_0 is the same for the two clock signals is for the most part true, despite the fact that the phase noise of a clock signal that is divided by two will be 6 dB lower than the phase noise of the original clock signal. Note that, for division by two, $6\text{ dB} = 20 \times \log 2$ (**Reference 2**).

The following example illustrates the effect of division by powers of two for both phase noise and jitter. These measurements employ a Silicon Laboratories Si5324 PLL device (**Figure 5**). Note that the high-speed VCO resynchronizes the output clock, regardless of the final output frequency, meaning that the edge shape and placement should be the

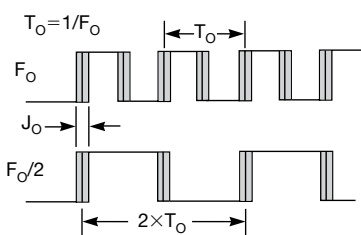


Figure 4 It is intuitive that an ideal divider divides down a clock signal that has the same clock-edge jitter after the divider as it has before the divider.

TABLE 1 DIFFERENCES IN TIME- VERSUS FREQUENCY-DOMAIN INSTRUMENTS

	Time domain	Frequency domain
Native measurements	Peak-to-peak, cycle-to-cycle, and period jitter	Phase noise, rms phase jitter, jitter-frequency information
Advantages	Good with low-frequency clocks and data-dependent jitter	Lower noise floor, easy detection of spurs versus random jitter

same for all possible divider values. The only difference should be that fewer clock edges occur during a given time interval. Although some retiming noise remains, the noise is the same for all of the divisor values (Figure 6).

The six curves in the figure are essentially the same but with a verti-

cal separation of 6 dBc/Hz. The 6-dB separation is relatively constant over all offset frequencies and divisor values, with one or two exceptions. On the right side of the plot, in which the offset from the clock, or carrier, is at its largest, the relative vertical offsets between the curves are compressed. The compres-

sion increases as the clock frequency decreases. This compression becomes more pronounced as the clock frequency and the phase-noise-curve values decrease. The compression occurs because the noise floor of the Agilent Technologies model E5052B signal-source analyzer nears the value of the phase noise, or jitter generation, of the Si5324 IC. The noise floor is an issue only because of the combined effect of the ultra-low jitter of the Si5324 and the low carrier frequency. Table 2 lists the corresponding jitter values for each of the six plots with the jitter integrated from 100 Hz to 20 MHz and all jitter values in femtoseconds rms.

Notice that the jitter increases slightly as the output frequency decreases—evidence that the output jitter is relatively constant despite the fact that 6 dB separates the phase-noise curves from one another. The rate at which the jitter increases becomes more pronounced at the lowest output frequencies. Let's examine the two sources of the increased rms-phase-noise values: instrument noise floor and aliasing.

NOISE FLOOR, PHASE NOISE

The instrument's noise floor can become the limiting factor of a measurement of phase noise of very-low-jitter clocks at low clock frequencies. At some point, you are measuring your equipment, not the DUT. Even though the phase-noise curves become monotonically smaller as the clock frequency decreases, the rms edge jitter remains almost constant because the phase-noise integration uses the clock period to scale the rms-jitter values.

To illustrate how this scenario occurs, consider the process of phase-noise integration to produce an rms-jitter value. Most modern phase-noise equipment produces a file that has two columns—typically, a CSV (comma-separated-value) file. One of the two columns lists the frequency offset from the clock, or carrier, frequency in hertz. The other column lists the phase-noise values at that offset frequency in decibels referenced to the carrier per hertz. Thus, the columns contain data-point pairs that describe the phase noise at a given offset from the clock frequency. Integration involves summing the area under the curve for all of the frequency-offset points after converting the

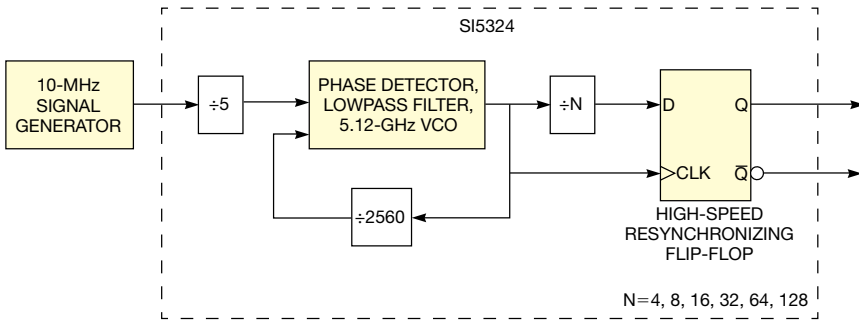


Figure 5 The measurements employ a Silicon Laboratories Si5324 PLL device.

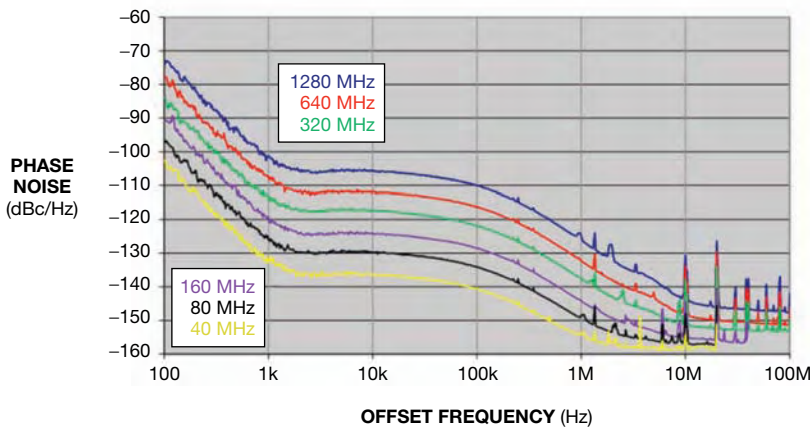


Figure 6 The high-speed VCO resynchronizes the output clock, regardless of the final output frequency, meaning that the edge shape and placement should be the same for all possible divisor values. The only difference should be that fewer clock edges occur during a given time interval.

TABLE 2 RMS-JITTER VALUES FOR DIFFERENT VALUES OF DIVISION

Color	Divisor	Output frequency (MHz)	Jitter (fsec rms)
Blue	Four	1280	441
Red	Eight	640	447
Green	16	320	461
Purple	32	160	463
Black	64	80	477
Yellow	128	40	523

decibels-referenced-to-the-carrier-per-hertz values to linear values using the following **equation**: Linear values = $10^{(\text{dBc/Hz})/10}$.

The equation for the area of a trapezoid in **Figure 7** is used to find the area described by two adjacent data-point pairs. You find the area under the curve by summing the area of all of the trapezoids. The final rms-jitter value is determined by scaling the result by two factors: The value $\sqrt{2}$ comes from the fact that the data was taken as one sideband; however, the rms jitter is assumed to be dual sideband. It is usually safe to assume that the two sidebands of the phase noise are symmetric about the clock frequency. In this case, it is even safer because a limiting amp suppresses AM (amplitude modulation) and passes FM (frequency modulation) to ensure symmetric sidebands (**Figure 8**).

The other scaling factor converts the area sum so that it is no longer in UIs (unit intervals) but in units of time. This factor keeps the rms edge jitter's values relatively constant, whereas the phase-noise values change. The equation for rms jitter is expressed as follows:

$$\text{rms jitter} = \frac{\sqrt{2}}{2\pi F_C} \sum_i \frac{(F_{i+1} - F_i) \times \left(10^{\frac{N_i+1}{10}} + 10^{\frac{N_i}{10}} \right)}{2},$$

where F_C is the clock frequency, N_i is the phase noise in decibels referenced to the carrier per hertz for the i th entry, and F_i is the offset frequency for the i th entry.

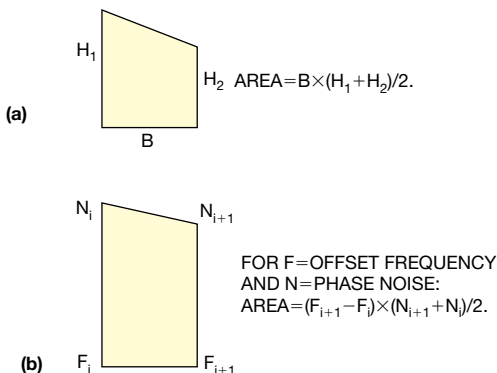


Figure 7 You find the area under the curve by summing the area of all of the trapezoids. You determine the final rms-jitter value by scaling the result by two factors.

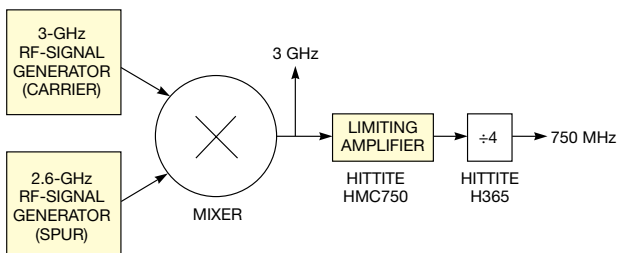


Figure 8 A limiting amp suppresses AM and passes FM to ensure symmetric sidebands.

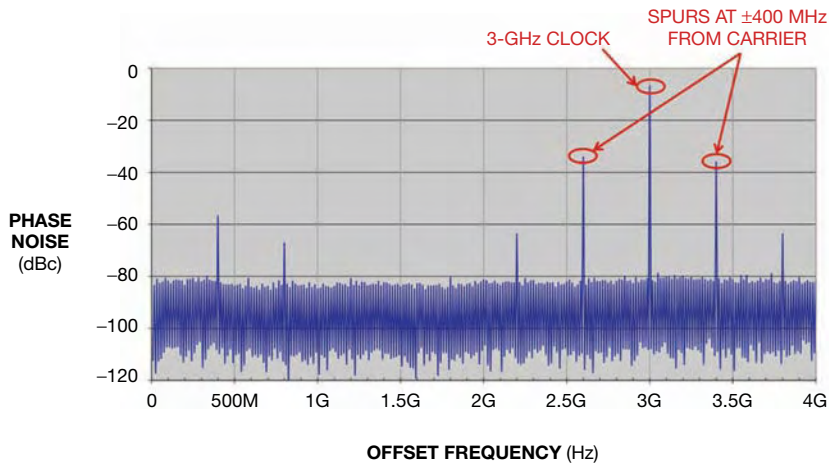


Figure 9 Symmetrical spurs occur at frequencies of 400 MHz above and below the 3-GHz clock frequency.

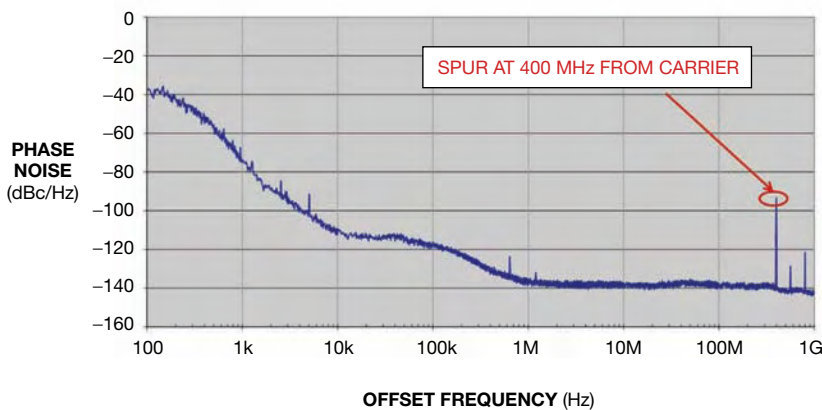


Figure 10 When the spectrum shows two equal sidebands, the phase-noise plot of the same signal combines their effect into one spur 400 MHz from the 3-GHz carrier. A divide-by-four circuit then divides down the 3-GHz signal to produce 750 MHz.

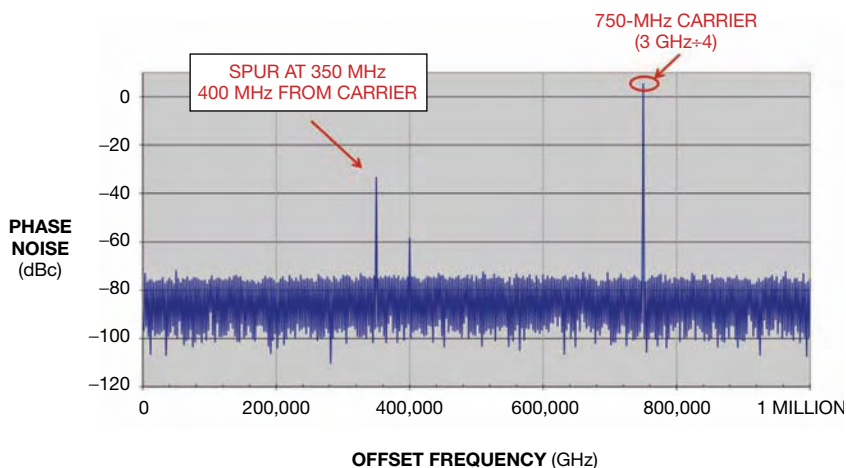


Figure 11 The spurs at 2.6 and 3.4 GHz alias down to a sideband spur at 350 MHz.

ALIASING

Aliasing is another cause of increasing rms-jitter values with decreasing clock frequency. For every division of two, the upper half of a phase-noise plot aliases down into the new lower-clock-frequency phase plot. Because phase noise is usually higher close to the clock or carrier frequency and drops off as the offset from the clock frequency increases, relatively little phase noise aliases down. However, when dividing by large numbers, the effect becomes cumulative and significant. For example, the difference between the 1280- and the 640-MHz curves in **Figure 1** is a constant 6 dB across the entire plot. As a result, you would expect that the increased rms-jitter values for the two curves in **Table 2** are due entirely to aliasing and not to the instrument's noise floor.

The spectra and phase-noise plots in **Figures 9** through **13** illustrate aliasing. The signals in these examples use AM to illustrate aliasing and are not what would be expected in a typical application. **Figures 9** and **10** show the spectra and phase-noise plots for the 3-GHz signal. The plots show symmetrical spurs at frequencies of 400 MHz above and below the 3-GHz clock frequency. When the spectrum shows two equal sidebands, the phase-noise plot of the same signal combines their effect into one spur 400 MHz from the 3-GHz carrier. A divide-by-four circuit then divides down the 3-GHz signal to produce 750 MHz.

Figures 11 and **12** show the spectra and phase-noise plots of the 750-MHz signal from the divide-by-four circuit. As a result of the division by four, the spurs at 2.6 and 3.4 GHz alias down to a sideband spur at 350 MHz. Note that 350 MHz is a frequency value that is the same 400 MHz from the 750-MHz carrier as 2.6 GHz is from the 3-GHz carrier. To further illustrate the aliasing, the 750-MHz signal is again divided down to 375 MHz. The 25-MHz spur in **Figure 13** is an alias of the spur at 350 MHz in **Figure 11**; that is, $25 \text{ MHz} = 375 \text{ MHz} - 350 \text{ MHz}$.

As you can see, the instrumentation's noise floor can become a limiting factor when measuring low-jitter clocks with low-frequency values. When a higher-frequency clock divides down the clock being measured, you can lower the value of the divider so that the measurement takes place at a higher frequency.

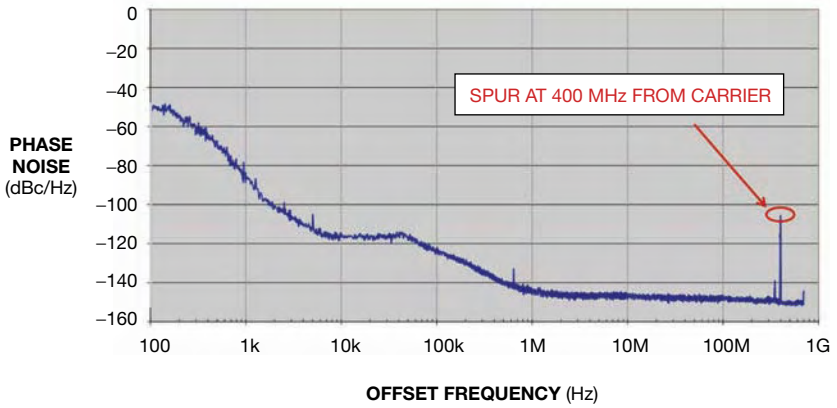


Figure 12 The 350-MHz frequency value is the same 400 MHz from the 750-MHz carrier as 2.6 GHz is from the 3-GHz carrier.

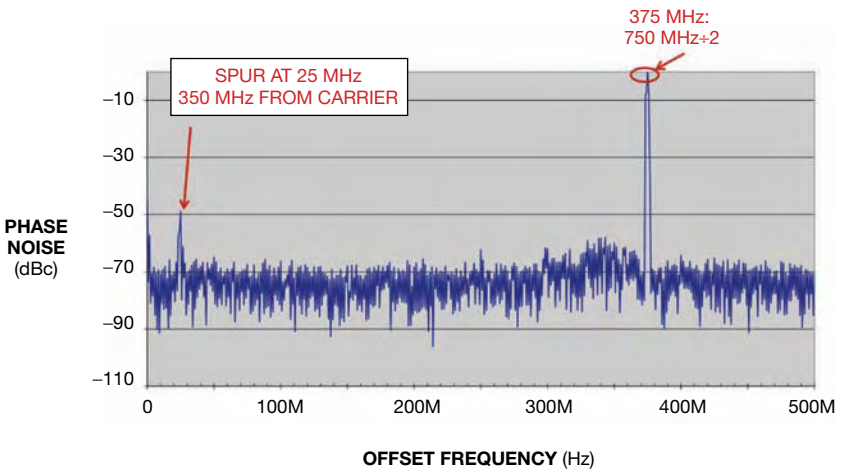


Figure 13 The 25-MHz spur is an alias of the spur at 350 MHz in Figure 11.

However, this commonly used technique removes the jitter contribution from higher-frequency jitter components that would have been aliased down by the division. Although the resulting rms-jitter values may be artificially lower, this approach is acceptable in applications in which the phase noise that is far off of the corner is relatively small. When measuring low-frequency clocks with appropriately high amounts of jitter, use time-domain equipment because the measurement can be made at the actual desired output frequency, no matter how low the clock frequency may be. **EDN**

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AUTHOR'S BIOGRAPHY



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