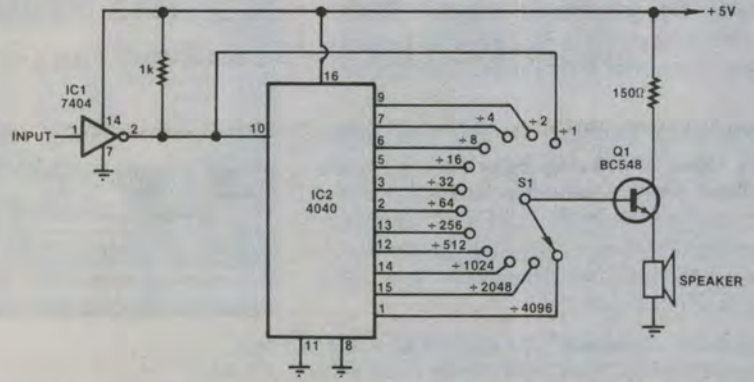
Digital clock monitor with audible output

When servicing digital equipment it is sometimes only necessary to know whether a clock or gate is producing an output. This can easily be determined by using the accompanying test circuit to "listen" to the suspect circuit.

The problem of listening to frequencies which are above audibility is overcome by selectable orders of frequency division. As shown it can divide by up to 4096 times, thus dividing a 5MHz signal to a mere 1220Hz.



The output under suspicion is fed into a 7404 TTL inverter (IC1). This ensures that the signal is within TTL levels and also provides some static protection for the following 4040 CMOS counter. The counter divides the signal, as already explained, and the upper limit is set by its speed (about 5MHz for the 4040).

This could be increased by adding a 7490, 7492, or 7493 TTL counter to the 4040 input to extend the limit to about 50MHz.

Output from the 4040 is fed to the base of a small transistor (BC549, etc) which drives a speaker. The level can be adjusted by varying the 150Ω resistor.

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