Adjustable TTL clock maintains 50% duty cycle

by Wilton Helm
Seventh-day Adventist Radio-TV-Film Center, Thousand Oaks, Calif.

The utility of the basic free-running transistor-transistor-logic clock can be greatly increased by adding a few components to provide a variable-frequency output over a 5:1 range or better, while still maintaining a 50% duty cycle of the square-wave output.

A common design of the free-running oscillator is shown in Fig. 1. Three inverters are connected as a three-stage inverting amplifier, with intermediate stages biased by the output of the previous stage, and the last stage pulled up to +5 volts by a bias resistor to provide a TTL-compatible output. Capacitor C, connected across the second amplifier stage, provides the necessary time delay to ensure positive feedback, and thus determines the frequency of oscillation.

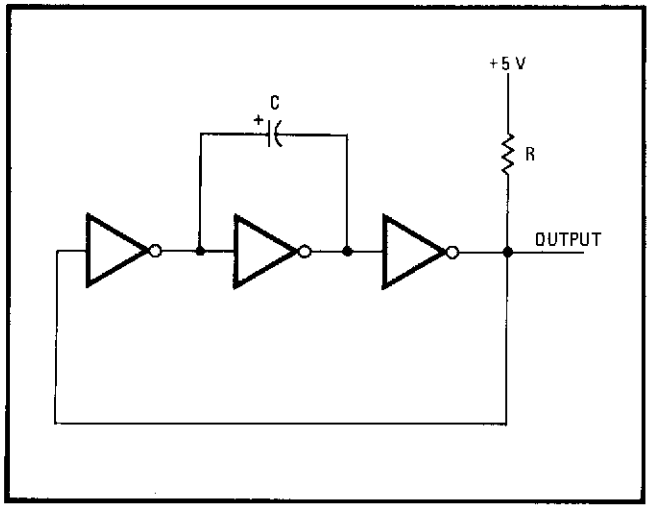
Adding a resistor, capacitor, and potentiomenter (R_2, C_2, and R_3), as in Fig. 2, enhances the versatility of the circuit. Capacitor C_1 performs the same time-delay function as C in the design of Fig. 1, but now serves to determine the upper limit of oscillation frequency, since it is paralleled by C_2.

The combination of C_2 and R_2 adds a time delay to the transitions of the second amplifier stage, additional to the delay of the upper-limit capacitor C_1. But the resistance in series with C_2 could tend to upset the symmetry of the square wave, as is usually the case when attempts are made to vary the frequency of the free-running-oscillator design of Fig. 1.

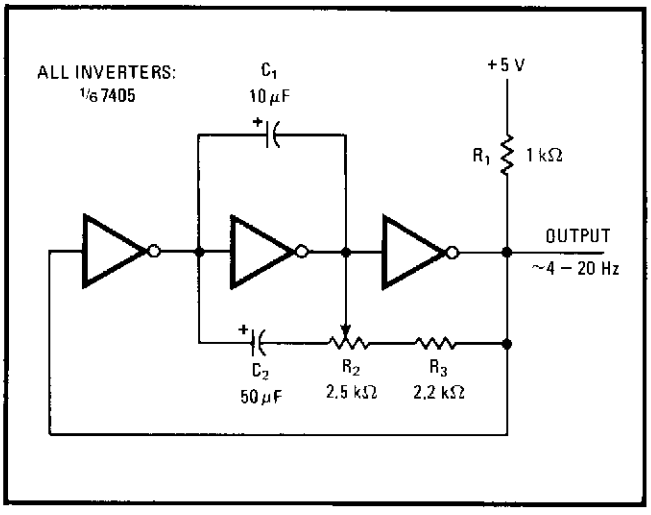
Symmetry of the square-wave output is maintained by connecting the right side of R_2 through resistor R_3 to the output of the third amplifier stage. This changes the charging current to the capacitors in proportion to the setting of frequency-adjusting potentiometer R_2. Thus, a duty cycle of 50% is constant over the entire range of oscillation.

The lower frequency limit is set by capacitor C_2. With the components shown, the frequency of oscillation can be varied by R_2 from about 4 to 20 hertz. Other frequency ranges can be obtained by changing the values of C_1 and R_3, which control the upper limit of oscillation, or C_2, which limits the low-frequency end.

Note that the inverters used in the adjustable oscillator are open-collector types, such as the 7405. The inherent low impedance of other types of inverters would swamp the effect of charging-current resistor R_3 and should not be used in this application. □



1. Free-running oscillator. Simple design of a TTL clock uses inverters. Frequency is determined by time constant of capacitor C with internal chip resistors. Low component count and good symmetry make it a natural for noncritical applications.



2. Adjustable counterpart. With the addition of three parts, the frequency of oscillation can be adjusted over a 5:1 range, while the attributes of the original design are maintained: the component count and cost is low, and the duty cycle is constant at 50%.