APPLICATION NOTE 975B

SPICE Computer Models for HEXFET® Power MOSFETs

(HEXFET is a trademark of International Rectifier)

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Introduction

The standard MOSFET models incorporated in SPICE (Simulation Program with Integrated Circuit Emphasis) were originally devised for lateral, low power structures. As such, they do not accurately simulate vertical MOSFETs. To enable SPICE modelling of circuits containing International Rectifier HEXFET power MOSFETs, SPICE model parameters are being added to HEXFET III third generation data sheets [1]. The performance of HEXFETs in a circuit may therefore be analysed without the need for expensive prototype construction. All the model parameters are specified on the data sheet so that the user does not have to extract any of the model elements from graphs or other data sheet parameters.

The type of model used allows accurate modelling of the HEXFET's switching performance while minimizing the computation time required. The model is suitable for use with most forms of SPICE.

Modelling Power MOSFETs in SPICE

The built-in MOSFET models in SPICE are more attuned to the modelling of low-voltage lateral MOSFETs such as might be encountered in integrated circuits rather than vertical DMOS power MOSFETs. The built in models are unable to simulate some of the features of a power MOSFET, such as the variable drain-gate capacitance and the body-drain diode.

In the absence of a suitable built-in model, the power MOSFET is usually simulated by combining further elements with the built-in MOSFET model to enable it to give a more faithful representation of such power MOSFET features as the variable drain-gate capacitance, the body-drain diode and parasitic inductances.

While the major test of a MOSFET model for small signal applications is its behavior in the linear regime, assessment of a power MOSFET model is usually based on its ability to accurately reproduce the switching of the device. The drain-gate (Miller) capacitance is a critical factor in determining the switching behavior of a power MOSFET. This capacitance varies with drain-gate voltage and therefore a successful power MOSFET model requires an accurate method of representing the variation in C_{gd}. However, this must be achieved without making excessive demands on the computational resources of the host machine.

The body-drain diode of the power MOSFET requires special attention. Ideally the model should be able to reproduce the reverse-recovery characteristics of the diode since diode recovery currents and the consequent losses can be significant in some circuit arrangements. However, this feature has been omitted in order to minimize computation times.

Other MOSFET features which are represented by the addition of further elements to the built-in model include the package inductances. These are important elements in determining power MOSFET switching due to the high values of di/dt involved. The source inductance in particular is a major factor in determining the maximum switching speed of the device.

The HEXFET Model

The new SPICE HEXFET model is shown in Figure 1. The built-in, level 3 MOSFET model is delineated by a

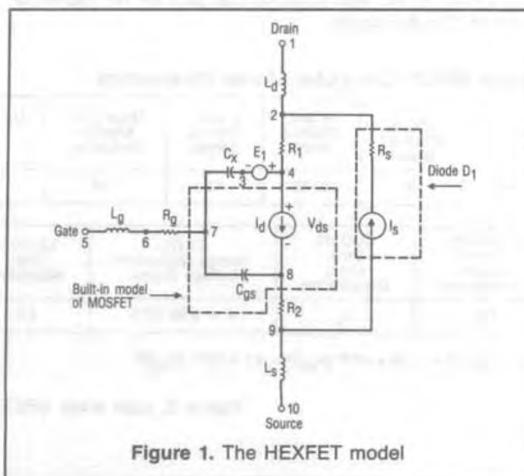

Figure 1. The HEXFET model

dotted line. The other elements of the model represent the following:

- L_g: The gate lead and bond wire inductance.
- R_g: The internal series gate resistance (principally the polysilicon gate resistance).
- L_d: The drain lead and bond wire inductance.
- R1: The epitaxial layer bulk resistance.
- R_S: The diode bulk resistance.
- I_S: A current source representing the relationship between diode current and diode voltage.
- R2: The source lead and bond wire resistance.
- L_S: The source lead and bond wire inductance.
- C_X: A scaled value of capacitance used to simulate the effect of C_{gd}. It is a polynomial capacitor whose coefficients are given in the individual datasheets as $(V_{GE})^n$ where n is the power of the polynomial.
- E1: A polynomial voltage dependent voltage source. This element has no physical reality, but is used to modify the voltage across C_X in such a way that the combination of C_X and E1 emulate the behavior of C_{gd} in the real device. Its coefficients are given in the individual datasheets as $(V_{DG})^n$.

The Miller capacitance, C_{gd}, is represented by a polynomial based on the drain-gate voltage. A high order of polynomial is used to model the rapid transition of C_{gd} from a high to a low value as V_{dg} increases. This is achieved by the use of a voltage dependent capacitor C_X connected in series with a voltage-controlled voltage source. This has the effect of causing the drain-gate capacitance to decrease with increasing drain-gate voltage. Although the value of C_X is far removed from the real value of C_{gd}, E1 is defined in such a manner that the charge which flows in and out of C_X as V_{dg} changes is identical to that which flows in and out of C_{gd} in the real device. A more detailed description of the operation of this part of the model is given in the Appendix.

Data Sheet SPICE Model Parameters

Figure 2 shows an example of the SPICE model data given on a HEXFET data sheet. The values shown are typical values. Model parameters are based on the physical properties and dimensions of the device with some adjustment to ensure a close fit with the measured electrical characteristics as given on the data sheet.

The following parameters constitute the built-in MOSFET model:

- Level of SPICE MOSFET model (LEVEL)
- Channel width (W)
- Channel length (L)
- Mobility modulation factor (THETA)
- Surface mobility (UO)
- Threshold voltage (VTO)
- Gate-source capacitance (CGSO)

The remaining parameters are elements that need to be added to the built-in model to give a model which more closely corresponds to a vertical, DMOS power MOSFET. These elements are listed in the previous section.

The element described as gate-drain capacitance is a voltage dependent capacitor. In some data sheets this has been referred to as C1, C2, C3 etc. depending on the device type. It is now designated as C_X for all device types. The name "Gate-Drain Capacitance" should not lead the user to expect that this value will be the same as that given for C_{gd} in the "Electrical Characteristics" section of the data sheet. As explained in the previous section, C_X is an artificial value used in conjunction with the voltage-controlled voltage source E1 to emulate the behavior of C_{gd}. As the equation for C_X shows, C_X is a polynomial function of V_{GE} which is the voltage between nodes 3 and 7 of the model (see Figure 1). The polynomial typically contains one or two components of different degrees. Examples of the performance of the C_{gd} model are

Typical SPICE Computer Model Parameters

Device	Level, SPICE MOSFET Model	W (m), Channel Width	L (μm), Channel Length	Theta (1/V), Mobility Modulation	UO (CM^2/V-S), Surface Mobility	VTO (V), Threshold Voltage	R1 (Ω), Drain Resistance	R2 (Ω), Source Resistance	RG (Ω), Gate Resistance
All	3	0.532	1.2	0.12	450	3.47	0.055	0.02	1

CGSO (pf), Gate-Source Capacitance	CGD (F) Gate-Drain Capacitance	E1 (V), Voltage Dependent Voltage Source	LD (nH), Drain Inductance	LS (nH), Source Inductance	LG (nH), Gate Inductance	IS (A), Diode Saturation Current	RS (Ω), Diode Bulk Resistance
730	C_X	4 + 0.95 VDG	4.5	7.5	7.5	1.4×10^{-13}	0.016

$C_X = 600\ pf + 2.38 \times 10^{-20} (V_{GE})^{20} - 1.1 \times 10^{-21} (V_{GE})^{22}$

Figure 2. Data sheet SPICE parameters for the IRF530

given in Figure 3 and Figure 4. While the curves yielded by the model do not exactly fit the curves of actual capacitance variation, in practice the resulting errors in the switching waveforms are small.

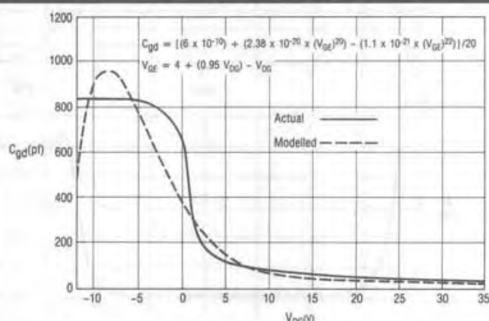

Figure 3. Gate-Drain Capacitance vs Drain-Gate Voltage (IRF530)

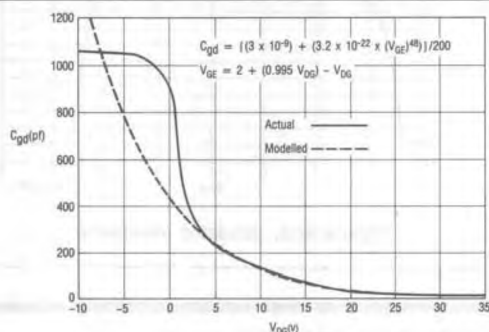

Figure 4. Gate-Drain Capacitance vs Drain-Gate Voltage (IRF730)

Loading the HEXFET Model

The following shows the HEXFET model listing for the IRF530. The data sheet SPICE parameters for this device are shown in Figure 2.

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******************************
*         IRF530             *
******************************
*
M530  4  7  8  8  IRF530  W=.532  L=1.2U
.MODEL IRF530 NMOS (LEVEL=3 THETA=.12
+UO=450 VTO=3.47 CGSO=730PF)
DI     9  2       DSD
.MODEL        DSD D IS=1.4E-12 RS=1.6E-2
LD     1  2       4.5NH
RI     2  4       .055
R2     8  9       .02
LS     9  10      7.5NH
EI     4  3  4  7  4  .95
Cx     7  3       POLY 600PF 0 0 0 0 0 0 0 0 0 0
+0 0 0 0 0 0 0 0 0 2.38E-20 0 -1.1E-21
RG     7  6       1.0
LG     6  5       7.5NH
*
```

Model Accuracy

The HEXFET model may be tested against reality on a simple test circuit such as that shown in Figure 5. The results of a test on this circuit are shown in Figure 6. As these waveforms show there is a degree of correspondence between the theoretical and actual waveforms which indicate that the model produces results in the switching regime that are sufficiently accurate for most purposes.

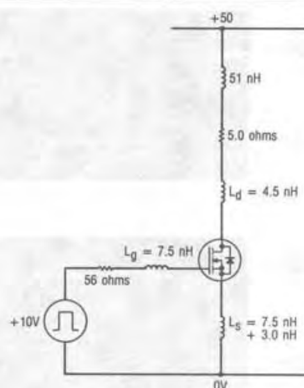

Figure 5. HEXFET power MOSFET test circuit

Model Constraints

Due to the manner in which C_{gd} is emulated by C_X and EI, the model suffers from one limitation. As can be seen from Figure 3 and Figure 4 the apparent value of C_{gd} becomes very large (either positive or negative) as V_{dg} reaches a value of approximately -10V. When the HEXFET is "on" this corresponds to a gate voltage of approximately +10V, since the drain will be approximately at source potential. A general failure of the model is likely to occur if the gate voltage is much above 12 volts.

It should also be noted that at some value of drain voltage beyond the breakdown voltage of the device the value of C_{gd} given by the model again becomes very large. However, this is not likely to be a serious limitation since the device cannot in practice be operated with a drain voltage beyond its breakdown voltage.

Summary

The new SPICE model for HEXFETs permits the SPICE user to model the performance of International Rectifier HEXFET power MOSFETs in the switching mode with a degree of accuracy that is acceptable for most applications. The model represents a compromise between a search for accuracy and the need to minimize computation times. As a consequence the gate-source voltage range is restricted to approximately 12 volts. A selection of HEXFET III data sheets carry the model data. Model information will progressively be made available for the whole HEXFET III range. □

REFERENCES

[1] International Rectifier "HEXFET III: a New Generation of Power MOSFETs" Application Note AN-966

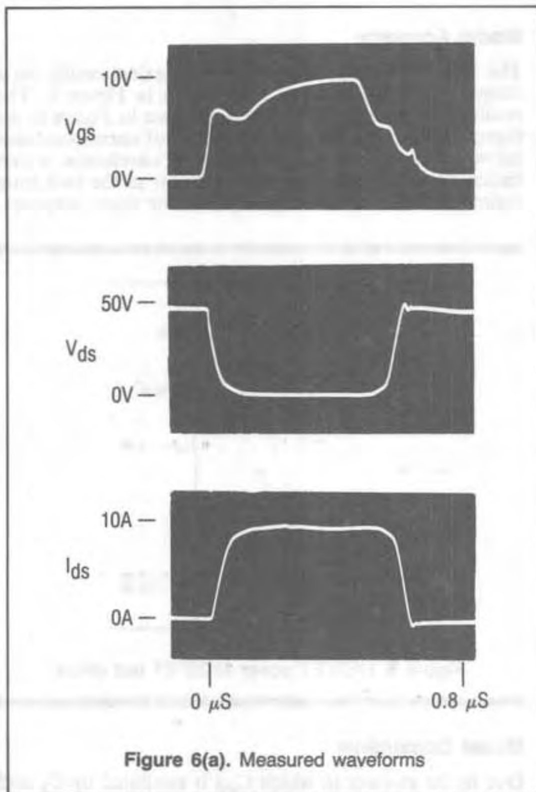

Figure 6(a). Measured waveforms

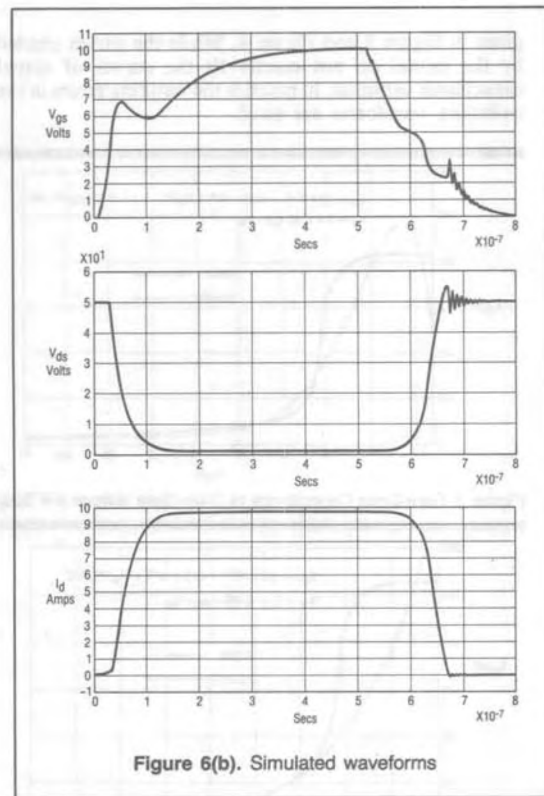

Figure 6(b). Simulated waveforms

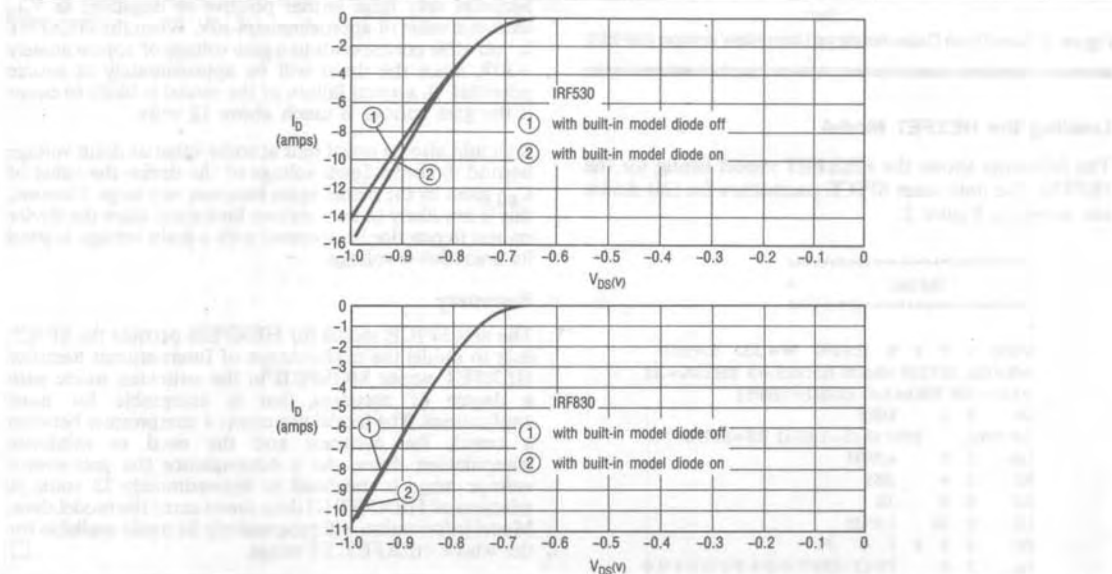

Figure 7. Error in modelled characteristics of body-drain diode due to conduction of bulk diode of built-in MOSFET

Appendix. Derivation of the HEXFET Model

Introduction

The model is shown in Figure 1. Components internal to the built-in MOSFET model are enclosed by dotted lines. The substrate of the built-in model is tied to its source, so that parameters associated with this junction are nullified.

The parameters of the model are calculated in the first place from the physical properties of the device, with adjustments where necessary to ensure a good fit with measured characteristics.

The Voltage-Controlled Current Source

In the ohmic region, the operation of the voltage dependent current source I_d is described by the following equation:

$$I_d = \frac{KP}{2} \cdot \frac{W}{L} \cdot V_{ds}\,[2(V_{gs} - V_{TO}) - V_{ds}] \qquad \textbf{(1)}$$

At saturation, I_d is described by:

$$I_d = \frac{KP}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_{TO})^2 \qquad \textbf{(2)}$$

Using the level-3 for N-MOS simulation and specifying KP in terms of its constituents, from **(2)** we have:

$$I_d = \frac{1}{2} \cdot \frac{E_{OX}}{T_{OX}} \cdot \frac{U_O}{[1 + THETA\ (V_{gs} - T_{TO})]} \qquad \textbf{(3)}$$

$$\cdot \frac{W}{L} \cdot (V_{gs} - V_{TO})^2$$

The default parameters pertinent to equation (3) are:

E_{OX} = 3.4E-8 (F/cm²) [oxide capacitance per unit area]

T_{OX} = 1E-7(m) [oxide thickness]

The input parameters are:

U_O: Surface mobility (cm²/V-S).

This is a process parameter dependent on the extent of the silicon doping. Typically U_O = 450 (cm²/V-S)

THETA: Mobility modulation factor (1/V).

This is the parameter which modulates surface mobility. As V_{gs} increases, effective surface mobility drops. It is found by adjusting THETA around a typical value of 0.1.

V_{TO}: Threshold voltage (V).

The model threshold voltage is typically 0.5 volts higher than the threshold as defined on the data sheet. It can be adjusted for a particular device.

W: Transistor channel region width (m).

This is determined from HEXFET die size measurements.

L: Transistor channel region length (m).
Typically L = 1.2 μm.

Resistances

R1: This represents the resistance encountered by the current flowing through the epitaxial drift region. R1 and R2 together with parameters for I_d determine the dc performance of the model. A value for R1 can be calculated from:

$$R1 = R_{ds(on)} - R_{CHANNEL} \qquad \textbf{(4)}$$

where $R_{ds(on)}$ = V/I, computed from a low V_{gs} and V_{ds} data point.

$$R_{CHANNEL} = \frac{1}{\left[\frac{KP}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_{TO})\right]} \qquad \textbf{(5)}$$

KP = 1.55E-5 for all models (computed by SPICE from the process parameter U_O).

The value for R1 is then adjusted to give best results in the ohmic region.

R2: This represents the parasitic resistance in the source. Its value for all devices in a TO-220AB package is 0.02 ohms.

R_g: HEXFET gate resistance is determined by putting an inductor in the gate of the device, applying a sinusoidal voltage to the gate and making current and voltage measurements at the resonance point. R_g can then be determined by calculating the damping factor of the circuit. The value of R_g varies from 0.5 to 3 ohms for different devices. R_g limits the rate at which junction capacitances can be charged and discharged and hence influences the switching performance.

Inductances

L_d: Parasitic drain inductance is calculated from lead wire measurements. For a TO-220AB package L_d = 4.5 nH.

L_S: The value of parasitic source inductance is 7.5 nH for a TO-220AB package.

L_g: Gate inductance is equal to the source inductance so that $L_g = 7.5$ nH for a TO-220AB package.

Stray inductances external to the HEXFET which arise from circuit wiring may also be taken into account. Their effect on circuit performance is the same as packaging inductances L_s, L_d and L_g.

Capacitances

C_{gd}: The HEXFET gate-to-drain capacitance is a function of drain-to gate voltage. Its value changes rapidly when V_{dg} is close to zero volts. The combination of the voltage source, E1, in series with the variable power-series capacitor C_x is used to model this capacitance. E1 is a voltage-controlled voltage source, controlled by V_{dg}, which serves two purposes. Firstly it offsets the voltage across the capacitor, thereby permitting C_{gd} to rise as V_{dg} falls and correctly locating the region in which the rapid change of capacitance takes place. Secondly, it decreases the voltage change across the capacitor by a factor of 200 for high-voltage devices and by a factor of 20 for low voltage devices. This is done so as not to go over the SPICE exponent limit ($E_{min} = -35$), when deriving polynomial coefficients. C_x is a voltage dependent power series capacitor.

The coefficients for the polynomial describing C_{gd} are found by curve fitting. Procedures for coefficient extraction are complicated since close approximations to the actual C_{gd} graphs are made. However, a procedure for deriving coefficients for a rough estimate of C_{rss} is given in [2]. Since the voltage change across C_x has been suppressed by a factor of 200 (factor of 20 for low voltage devices), the capacitance value is increased by a factor of 200 (factor of 20 for low voltage devices) above the actual value of C_{gd} in order to give the correct apparent value of gate-drain capacitance.

C_{gs}: The gate-to-source capacitance is essentially independent of voltage and current variations. It is given by:

$$C_{gs} = C_{iss} - C_{rss} \quad (6)$$

The value of C_{gs} is then entered as per unit channel width capacitance C_{gso} as follows:

$$C_{gso} = \frac{[C_{gs} - (C_{ox} \cdot W \cdot L)]}{W} \quad (7)$$

C_{ds}: The drain-to-source capacitance is also a decreasing function of the voltage. In the switching regime the effect of C_{gd} swamps that of C_{ds}. C_{ds} has therefore been omitted to minimize computation time.

DI: The HEXFET source-to-drain integral diode is modelled by diode D1. The bulk-to-drain diode of the built-in MOSFET model cannot be used for this purpose because its corresponding resistance R1 has been adjusted to give satisfactory simulation of the MOSFET output characteristics in the linear region. As a result, the bulk-to-drain diode has to be shut off by specifying $I_s = 0$ and a separate diode used to model the HEXFET body-drain diode. The saturation current for D1 is found from:

$$I_s = \exp\left[\ln(I_{d1}) - \frac{V_{d1}}{V_t}\right] \quad (8)$$

where $V_t = 26$ mV (thermal voltage). I_{d1} and V_{d1} represent a low current data point. Diode bulk resistance can then be determined from:

$$R_s = \frac{\left[V_{d2} - V_t \cdot \ln\left(\frac{I_{d2}}{I_s}\right)\right]}{I_{d2}} \quad (9)$$

where I_{d2} and V_{d2} represent a high current data point.

A difficulty arises in some versions of SPICE in that the bulk-to-drain diode of the built-in model does not stop conducting when I_s is set to zero. Fortunately the amount of current carried by this diode is small compared with the current which flows in the diode model D1. The reason for this is that R1 is usually large compared with R_s. This is particularly true of high-voltage devices. Figure 7 shows the error produced with versions of SPICE in which the bulk-drain diode of the built-in MOSFET model is not shut off for two devices. The IRF530 is rated at 100V and the IRF830 at 500V. □

REFERENCES

[2] P.O. Lauritzen, F. Shi "Computer simulation of power MOSFETs at high switching frequencies" Proc. Power Conversion International, October, (1985)