Reliability Section

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The Approach to HEXFET Reliability

The purpose of International Rectifier's HEXFET Reliability Program has been, from its very beginning in 1982, to provide design engineers with all the information required to determine the failure rate of their design in its operating environment.

It was felt that the traditional "statistical approach" to equipment reliability calculation, which relied on the historic information of MIL-HDBK-217 and a formula composed of factors that are wide open to subjective evaluation, was not useful nor appropriate for state-of-the-art devices in a scenario of rapid technological change.

As an alternative we proposed the "technological approach," which relied on the design engineer, who is intimately familiar with electrical and thermal stresses in the circuit, to perform a reliability analysis based on the effects of those stresses on the life of the devices.

The two key elements that would allow the designers to perform this task are the following:

1. The *Characterization* of the dominant failure mechanisms of the devices.
2. The *statistical sampling* of each and every production wafer lot to insure that the product conforms to the values identified in the characterization.

The concept of characterization is not new in the semiconductor industry; reliability studies have been around for a good many years. Their value was mainly academic, however, since no company would guarantee that its production conformed to any specific report. What is significantly new in International Rectifier's approach is its commitment to deliver semiconductors with a specific failure behavior.

There is a third element in our reliability program: The *Qualification*. A new product cannot be released to production until it has passed the Reliability Qualification tests. This insures that the design is sound from a reliability point of view. For this reason, a product would go through a requalification if the design were to change significantly.

The following Sections I-III describe in more detail the programs outlined above. The results of the Reliability Characterization are updated on a quarterly basis by the HEXFET Quarterly Reliability Report which is available upon request. In addition, Section IV describes the failure analysis and customer return procedures at International Rectifier.

1.1 Using HEXFET Reliability Information

In this section the user will find three principal sets of graphs for each package type: the gate-oxide lifetime (Fig. 1), the High Temperature Reverse bias failure rate (Fig. 2), and the effects of power cycling (Fig. 3). These graphs show the effect of operating conditions on device lifetime. (The graphs shown here are examples only and the relevant information for a particular device should be obtained from this current quarterly reliability report). These graphs can be used by the circuit designer to arrange the operating conditions of the HEXFET so that optimum reliability is achieved. This information allows the designer to avoid expensive over-design while being confident that the necessary level of reliability has been achieved.

Appropriate Information

Traditionally, reliability results have been presented in terms of Mean-Time-To-Failure or Median-Time-To-Failure. While these results have their value, they do not necessarily tell the designer what he most needs to know. For example, the Median-Time-To-Failure tells the engineer how long it will take for half a particular lot of devices to fail. Clearly no designer wishes to have a 50% failure rate within a reasonable equipment lifetime. Of greater interest, therefore, is the time to failure of a much smaller percentage of devices — say, 1% or 0.1%. For example, if it has been decided that one failure per hundred units over five years is an acceptable failure rate for the equipment, and each unit contains one critical component, the designer knows that the time to accumulate 1% failure of that component must be at least five years. If there are ten such components per unit, then no more than 0.1% of the components may fail in five years. Therefore, the HEXFET reliability or operating-life data is presented in terms of the time it will take to produce a prescribed number of failures under the given operating conditions.

Sample Calculations

The use of graphical reliability information is best illustrated by the following sample calculations.

Example 1: Use of gate oxide lifetime graph

A gate voltage of 10 or 12 volts is adequate to ensure that a HEXFET stays fully turned-on in most applications. However, in applications where high peak currents are encountered, a greater gate voltage may be required to ensure that device does not go into the pinch-off region with a consequent increase in drain to source voltage. This is particularly true of low voltage devices which have high current ratings compared with their low voltage counterparts. The channel region is called upon to carry higher peak currents and a greater gate voltage is required. Under such circumstances, it can be the gate oxide lifetime which limits the allowable peak drain current.

A circuit uses on IRF130 to switch a current of 35 amps with a duty cycle of 10%. The designer wants to know how long it will take to accumulate 1% failures under these conditions. The supply voltage is low with respect to the voltage rating of the device so that the HTRB failure rate is not significant. The device is to be operated at a maximum junction temperature of 140°C.

Fig. 4 shows the relationship between $R_{DS}(on)$, the drain current I_D and the gate voltage V_{GS} for an IRF130 at T_J = 25°C. From this it can be seen that a practical minimum for the gate voltage, taking into consideration device dissipation and the possible spread in threshold and transconductance characteristics, is 16V.

The gate-oxide lifetime data given in Fig. 1 is a worst case condition for all N-channel HEXFETs and may therefore be used for the IRF130. Therefore:

From the gate lifetime curves in Fig. 1,

Time to accumulated 1% failures at T_J = 140°C and V_{GS} = 16V	= 6 × 10^8 hours
Duty cycle	= 0.1
Time to acquire 10^4 hours of exposure to a gate voltage of 16V	= 6 × 10^8/ 0.1 hours = 68,446 years

If this time to 1% failure is unacceptable, then a device with a lower $R_{DS}(on)$ must be used so that the required drain current can be obtained with a lower gate-source voltage. A lower $R_{DS}(on)$ will also result in less dissipation and a lower junction temperature with the same heatsink, thereby extending the life of the device. However, as will be seen from Fig. 1, gate voltage is the most significant factor in determining gate-oxide lifetime.

Example 2: Use of HTRB Graph

A power supply is to be designed that will provide a continuous output of 250W to a dedicated load, twenty four hours per day. The circuit employs two HEXFETs as the power switching elements. The HEXFETs and their heatsinks are to be chosen so that there are no more than 0.1% accumulated failures over 5 years.

First, gate-oxide lifetime is checked. The maximum applied gate voltage has been set at 10 volts. This is quite adequate to ensure full enhancement of the channel of the HEXFET when the drain current is at its maximum value. The junction temperature is as yet unknown but is estimated as no greater than 90°C. From Fig. 1 the time to 0.1% accumulated failures under these conditions is found to be 102 years. Clearly gate failure rates are low enough to be ignored.

Next, the maximum allowable junction temperature is obtained from the HTRB failure graph as follows:

Number of hours in 5 years	= 43,830
Percentage of time that HEXFET is under blocking voltage	= 0.55
Effective number of device operating hours per 1000 units in 5 years	= 43,830 × 2 × 0.55 × 1000 = 4.82 × 10^7 hrs
Failure rate in FITs (failures in 10^9 hours)	= 10^9/(4.82 × 10^7) = 21 FITs

From the HTRB failure rate graph (Fig. 2):

Maximum allowable junction temperature = 72°C. Assuming a half-bridge circuit operating from 220V minus 15% (low line condition) and an efficiency of 80%, the peak current in each device will be 2.7 amps at a duty cycle of 45% (assuming a rectangular waveform).

There are two devices suitable for this application:

(a) The IRF430.

$R_{DS}(on)$ max at 84°C	= 2.4 ohms
Thermal resistance junction to case	= 1.8 °C/W

(b) The IRF440.

$R_{DS}(on)$ max at 84°C	= 1.36 ohms
Thermal resistance junction to case	= 1.1 °C/W

Both devices are in a TO-3 package. The IRF440 employes a larger area die. Hence its lower $R_{DS}(on)$ and lower thermal resistance.

The next stage of the design is to chose a heatsink for each device that will ensure that the peak junction temperature does not exceed 84°C.

(a) For the IRF430.

Conduction losses $= (2.7)^2 \times 2.4 \times 0.45 = 7.9$ W

Assuming an ambient temperature of 45°C,

Temperature rise junction to ambient $= 72 - 45 = 23$°C

Thermal resistance required, junction to ambient $= 23/7.9 = 2.9$°C/W

Thermal resistance required, sink to ambient $= 2.9 - 1.8 = 1.1$°C/W

(b) For the IRF440:

Conduction losses $= (2.7)^2 \times 1.36 \times 0.45 = 4.46$ W

Assuming an ambient temperature of 45°C,

Temperature rise junction to ambient $= 68 - 45 = 23$°C

Thermal resistance required, junction to ambient $= 23/4.46 = 5.2$°C/W

Thermal resistance required, sink to ambient $= 5.2 - 1.1 = 4.1$°C/W

Clearly, the designer's reliability objectives can be achieved either by employing a low resistance device on a small heatsink or a higher resistance device on a large heatsink. Considerations such as size, cost and efficiency will determine which is most suitable.

Example 3: Use of Power Cycling graph

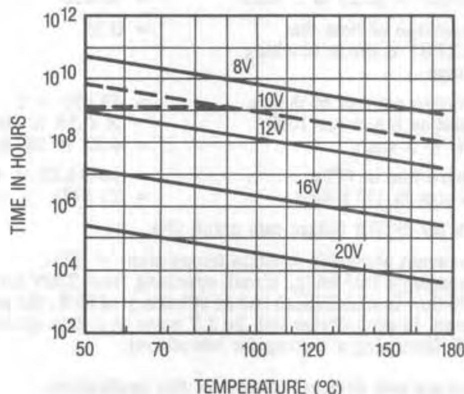
The die bond in any power semiconductor eventually fatigues if submitted to a sufficient number of thermal cycles. This is due mainly to differential expansion between the silicon and the solder or metal surface to which it is attached. The failure rate is dependent on the temperature excursion in each power cycle. Fig. 3 shows the relationships between accumulated failures, the number of power cycles and the temperature excursion for a HEXFET with a die size of 6.5mm × 6.5mm. Since failure rates are generally greater for the larger die, this information is valid for this die size and smaller dice mounted in the same manner.

As an example of the use of these curves, consider the reliability of a piece of equipment which is turned on and off once a day. The equipment contains one HEXFET transistor operating at a temperature of 100°C. The designer wishes to know the time to accumulate 0.1% failures.

From Fig. 3 it can be seen that, for a delta T of 100°C,

the number of cycles to accumulate 0.1% failures = 10,000

time to accumulate 0.1% failures = 10,000/365 = 27 years



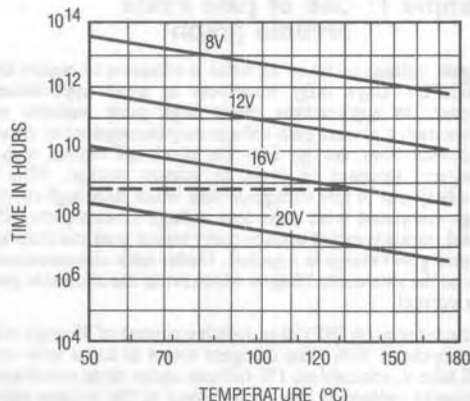


Figure 1. Gate oxide life data

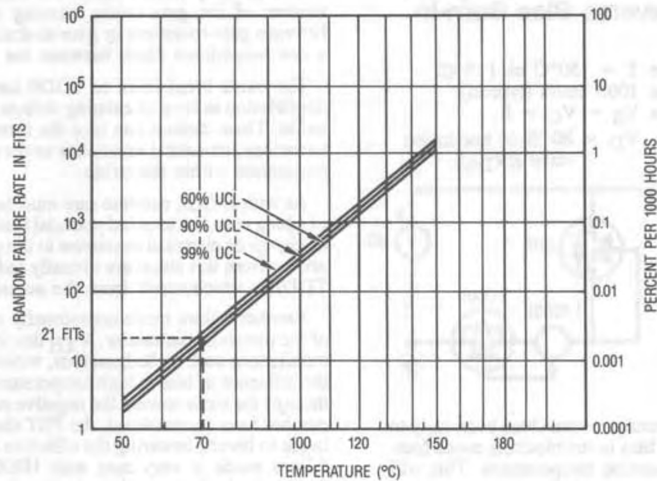


Figure 2. HTRB life data

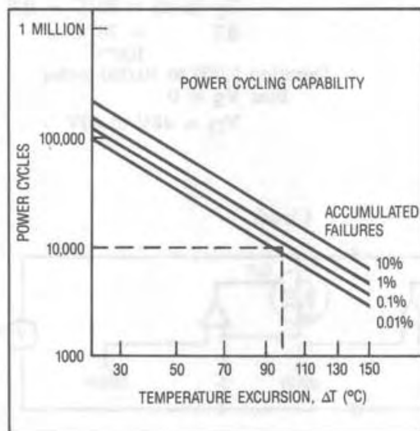


Figure 3. Power cycling data

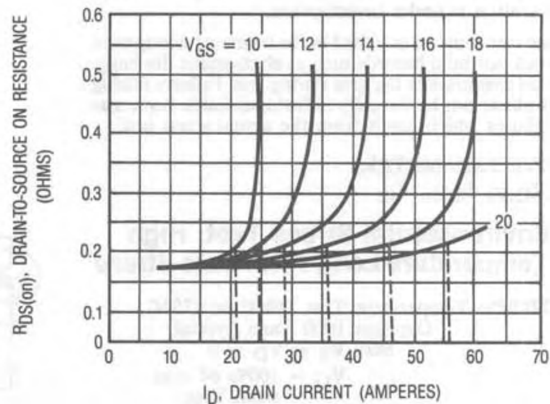
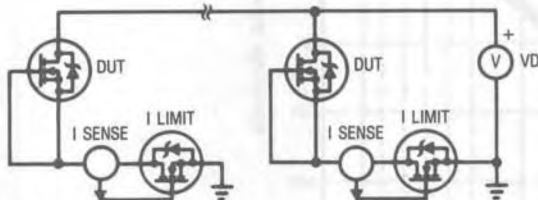


Figure 4. Relationship between $R_{DS(on)}$, I_D, and V_{GS} of IRF130

1.2 Environmental Stress and Failure Mode

1.2.1 Environmental Stress Test: High Temperature Reverse Bias Burn-In (HTRB)

CONDITIONS: Temperature T = 150°C or 175°C
Duration 1000 hours (typical)
Bias $V_S = V_G = 0$
V_D = 80 % of maximum rated BV_{DSS}



PURPOSE
The purpose of high temperature reverse bias burn-in is to stress the devices with applied bias in the blocking mode (cut-off mode) while at elevated junction temperatures. This will accelerate any blocking voltage degradation process.

FAILURE MODES
The primary failure mode for HTRB stress is a gradual degradation of the breakdown characteristics or BV_{DSS}. This degradation has been attributed to the presence of foreign materials and polar/ionic contaminants. These materials, migrating under the application of electric field at high temperature, can perturb the electric field termination structure.

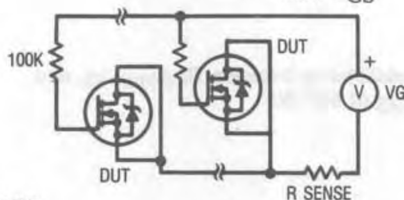
A secondary failure mode, threshold voltage degradation has been present in HTRB stress with less frequency than the primary failure mode. The mechanism responsible for this degradation is under investigation.

Extreme care must be exercised in the course of a long term test to avoid potential hazards such as electrostatic discharge or electrical overstress to the gate during test. Failures arising from this abuse can be virtually indistinguishable from true HTRB failures which result from the actual stress test.

SENSITIVE PARAMETERS
BV_{DSS}, I_{DSS}, I_{GSS}, V_{th}

1.2.2 Environmental Stress Test: High Temperature Long Term Gate Stress

CONDITIONS: Temperature T = 150°C or 175°C
Duration 1000 hours (typical)
Bias $V_S = V_D = 0$
V_G = 100% of max. rated V_{GS}



PURPOSE
The purpose of long term high temperature gate stress is to stress the devices with applied bias to the gate of the device while at elevated junction temperatures. This will accelerate what is known as time-dependant dielectric breakdown (TDDB) of the gate structure.

FAILURE MODES
The primary failure mode for long term gate stress is a rupture of the gate oxide, casuing either a resistive short between gate-to-source or gate-to-drain or what appears to be a low breakdown diode between the gate and source.

The oxide breakdown or TDDB has been attributed to the degradation in time of existing defects in the thermally grown oxide. These defects can take the form of localized thickness variations, structural anomalies or the presence of sub-micron particulate within the oxide.

As with HTRB, extreme care must be exercised in the course of a long term test to avoid potential hazards such as electrostatic discharge or electrical overstress to the gate during test. Failures arising from this abuse are virtually indistinguishable from true TDDB's which result from the actual stress test.

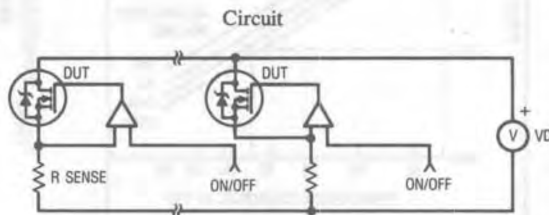
Another failure mode occasionally observed is degradation of the threshold parameter, V_{TH} due to the presence of highly mobile ions such as Sodium ions, within the gate oxide. Under the influence of bias at high temperatures, these ions will move through the oxide toward the negative surface. Once a sufficient number have accumulated, the FET channel in the vicinity can begin to invert, lowering the effective threshold voltage. This failure mode is very rare with HEXFETs due to inherent features in the design and due to cleanliness of wafer fabrication.

SENSITIVE PARAMETERS
I_{GSS}, V_{TH}.

1.2.3 Environmental Stress Test: Power Cycling

CONDITIONS: Temperature T_C (min) = 30°C
T_C (max) = 30°C + ΔT
ΔT = 70°C or 100°C
Duration 5,000 to 10,000 cycles
Bias $V_S = 0$
V_D = 48V to 80V

Circuit



PURPOSE
The purpose of power cycling is to simulate the thermal and current pulsing stresses which devices will encounter in actual circuit applications when either the equipment is turned on and off or the power is applied to the device in short bursts interspersed with quiescent, low power periods. The simulation is achieved by the on/off application of power to each device while they are in the active linear region.

FAILURE MODES
The primary failure mode for power cycling is a thermal fatigue of the silicon/metal interfaces and metal/metal interfaces. The fatigue, due to the thermomechanical stresses

from the heating and cooling, will cause electrical or thermal performance to degrade.

If the degradation occurs at the header/die interface, then the thermal impedance, θ_{JC}, will begin to increase well before any electrical effect is seen. If the degradation occurs at the wire bond/die interface or the wire bond/post interface, then on resistance, $R_{DS(on)}$, will slowly increase or become unstable with time. The thermal impedance, when measured during this time may appear to decrease or change erratically.

The mechanical stresses from the application of power can also propagate fractures in the silicon when the die is thermally mismatched to the solder/heat sink system. These fractures will manifest themselves in the form of shorted gates or degraded breakdown characteristics (BV_{DSS}).

SENSITIVE PARAMETERS
I_{GSS}, BV_{DSS}, Θ_{JC}, $R_{DS(on)}$.

1.2.4 Environmental Stress Test: Tempeature Cycling

CONDITIONS: Temperature T_C (min) = -55°C
T_C (max) = +150°C
ΔT = 205°C
Duration 1000 cycle (typical)
Bias No bias applied during test
Circuit none

PURPOSE
The purpose of temperature cycling is to simulate thermal stresses which devices will encounter in the actual circuit applications (as with power cycling) in combination with potentially extreme operating ambient temperatures. Some equipment is destined to be used in extreme environments, and subject to daily temperature cycles.

FAILURE MODES
The primary failure mode for temperature cycling is a thermal fatigue of the silicon/metal interfaces and metal/metal interfaces. The fatigue, as in the case of power cycling in section 1.2.3, results from thermomechanical stresses due to heating and cooling and will cause electrical or thermal performance to degrade.

If the degradation occurs at the header/die interface, then the thermal impedance, θ_{JC}, will begin to increase well before any electrical effect is seen.

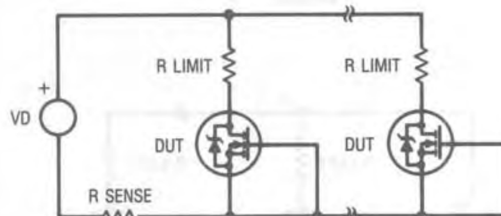
If the degradation occurs at the wire bond/die interface or the wire bond/bond post interface, then on resistance, $R_{DS(on)}$, will slowly increase or become unstable with time. The thermal impedance, when measured during this time, may appear to decrease or change erratically.

The mechanical stresses from the temperature can also propagate fractures in the silicon when the die is thermally mismatched to the solder/heat sink system. These fractures will manifest themselves in the form of shorted gates or degraded breakdown characteristics (BV_{DSS}).

SENSITIVE PARAMETERS
I_{GSS}, BV_{DSS}, Θ_{JC}, $R_{DS(on)}$.

1.2.5 Environmental Stress Test: Temperature-Humidity-Bias (85/85)

CONDITIONS: Temperature T = +85°C
Humidity Relative Humidity = 85% or 81%
Pressure P = 0 psig
Duration 1,000 hours (typical)
Bias $V_G = V_S = 0V$
V_D = full bias (typical)
Circuit



PURPOSE
The purpose of temperature-humidity-bias testing is to subject non-hermetic encapsulated devices to temperature and humidity extremes with bias on the drain. This test is a method of examining the ability of a non-hermetic package to withstand the deleterious effects of a humid environment. The devices are placed in a temperature and humidity chamber at ambient pressure and are biased in a cut-off mode.

FAILURE MODES
There are two primary failure modes which have been observed. The first failure mode comes about as a result of the ingression of water molecules into the active area on the surface of the die. Once sufficient water has accumulated in the region of the electric field termination structure on the HEXFET, the perturbation of that field begins to degrade the breakdown characteristics of the device.

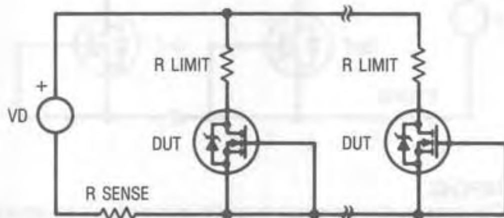
The second failure mode that has been observed is due to cathodic corrosion of the Aluminum source bonding pad. As with the first failure mode, water will ingress to the top of the die. There, in the presence of applied bias, an electric current through the few monolayers of water will begin to cause the bond pad to dissolve. Eventually, the corrosion will proceed to the point where the current capability of the device is impaired and parameters such as $R_{DS(on)}$ and V_{SD} begin to increase and become unstable.

The dominance of either of these failure modes is basically determined by the amount of bias present during the test. Under low bias conditions, the corrosion proceeds slowly, so the first failure mode will dominate. Alternatively, if a high bias is applied to the drain, the corrosion will proceed very rapidly, and the device will fail due to on-resistance before the breakdown characteristic can degrade.

SENSITIVE PARAMETERS
BV_{DSS}, $R_{DS\ (on)}$, V_{DS}.

1.2.6 Environmental Stress Test: Highly Accelerated Temperature and Humidity Stress Test (HAST)

CONDITIONS: Temperature
Dry Bulb T_a = +100 - 175 °C
Wet Bulb T_a = +100 - 158 °C
Humidity Relative Humidity = 50% - 100%
Pressure P = 0 - 70 psig
Duration Variable
Bias V_{DS} = 10 volts (typical)
Circuit



PURPOSE

The purpose of Highly Accelerated temperature and humidity Stress Test (HAST) is to subject non-hermetic encapsulated devices to temperature and humidity extremes while under pressure in a nonsaturated environment. The HAST test has now supplanted the pressure cooker test as a method of choice. The HAST test serves as a method of quick evaluation of the relative hermeticity of epoxy encapsulated packages. The devices, placed in a pressurized vessel with bias at a preselected temperature and humidity for several tens or hundreds of hours, are then read out and examined for any degradation.

FAILURE MODES

Like the sister test, 85/85 (see section 1.2.5), there are two failure modes which have been observed. The first mode, degradation of the breakdown characteristics of the devices, can occur in the same fashion as noted in the 85/85 test. Biasing the devices at a much higher temperature than in 85/85 conditions while in a non-saturated atmosphere imparts a much higher diffusion of water into the bulk of the epoxy encapsulation. Once water arrives at the surface of the die blocking voltage capability degrades much faster than in 85/85 exposure.

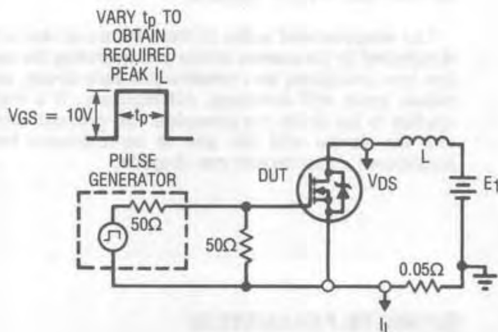
The second failure mode that has been observed is due to cathodic corrosion. This occurs in the same way as described in section 1.2.5. It is possible for contaminants to work their way into the active area of the device while under pressure in the presence of water. For that reason, the devices and test board are cleaned prior to use. Then, throughout the course of the testing, the parts and the test boards are never brought into contact with human contaminant.

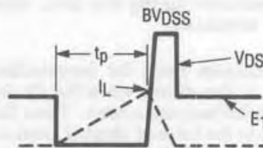
SENSITIVE PARAMETERS

BV_{DSS}, R_{DS} (on).

1.2.7 Environmental Stress Test: Inductive Load Life Test

CONDITIONS: Temperature $T_{HEAT\ SINK}$ = 45°C
T_j Max. Rated T_j
Duration 1000 hours
Bias V_S = 0
V_G = 12V (on) or 0V (off)
V_D = 15V to 50V
Frequency = 0.77 Hz to 40 KHz
Circuit





PURPOSE

The purpose is to simulated highly repetitive avalanche breakdown stress, and to detect any uneven distribution of avalanche current throughout the die. Devices are subject to this type of stress in actual circuit application. And, it is not known whether this use will lead to some unknown failure mechanism.

FAILURE MODES

No failure has been detected.

1.3 Reliability Theory

Reliability can be defined as a probability of failure-free performance of a required function, under a specified environment, for a given period of time. The reliability of semiconductors has been extensively studied and the data generated from these works is widely used in industry to estimate the probabilities of system lifetimes. The reliability of a specific semiconductor devices is unique to the technology process used in fabrication and to the external stress applied to the device.

In order to understand the reliability of a specific product like the HEXFET®, it's useful to determine the failure rate associated with each environmental stress that HEXFET® s encounter. The failure rate, f, of a collection of N devices can be expressed as:

$$f = \frac{r}{N\Delta t} \quad (1)$$

where r is the number of failures that occur in a span of time Δt. This equation can be modified to express the statistical reliability by specifying the upper confidence limit (UCL) as

$$f = \frac{X\ (1 - UCL);\ (2r + 2)}{2\ N\ \Delta t} \quad (2)$$

where X is the CHI squared function

The values reported in this report are at a 60% upper confidence limit. It has been shown (Ref. 3) that the failure rate of semiconductors in general, when followed for a long period of time, exhibits what has been called a "bathtub curve" when plotted against time (see figure 5) for a given set of environmental conditions.

Three specific epochs of a device's lifetime can be present: Infant region, Random region, and the Wearout region. The Infant region consists of an initially high failure which falls rapidly in the first few tens of hours of operation. After this period of infant failures, there follows a long period of time with a very low, almost constant failure rate. This period is referred to as the Random region where the few devices that fail in this period do so as a result of random causes. Following the Random region period (which can last for tens of millions of hours under low stress conditions) the failure rate will begin to rise, reach a maximum, and slowly fall again as the number of survivors decrease. This is the third epoch, the Wearout region, which signals the end of useful life. The failures that occur at this time are often due to processes whose rates are affected by temperature or humidity stresses.

Failure Rate Models

The bathtub curve for HEXFETs® is determined for each environmental stress by testing production units and evaluating the results. The accelerated-life stress tests result in an accelerated number of failures that occur during one of the three failure rate regions of the bathtub curve in Figure 5. The data from each test is evaluated by or modeled according to an appropriate probability theory, depending on the failure rate region involved.

One such theory, the Exponential probability theory, assumes the failure rate is constant and the accumulation of failures in time is exponential. These conditions apply to the Random region of the failure rate curve because the failure rate decreases very slowly. The 1000-hour HTRB burn-in test failures are from the Random region. The failure rate from these tests is estimated by equation (2). The Arrhenius model allows the failure rate to be estimated for other temperatures as well.

The second probability theory, Lognormal Probability, assumes a non-constant failure rate which follows the lognormal probability density function (ref 4). It has been shown (ref. 3, 4) that accelerated-life stress test failure rates follow the lognormal probability function as follows:

$$f = \frac{1}{\sigma t \sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{\ln t - \mu}{\sigma}\right)^2\right] \quad (3)$$

where t is time, μ represents the median lifetime (actually e^{μ}) and σ is the lognormal standard deviation. The instantaneous failure rate at a time t is expressed as:

$$\lambda\ (t) = \frac{f(t)}{\int_t f(x)\ dx} \quad (4)$$

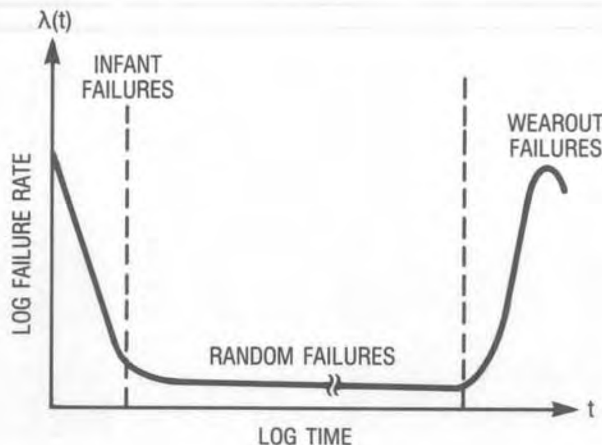


Figure 5. Classic bathtub curve for failure rate of solid state devices (Ref. 1)

2.0 Statistical Reliability Sampling Program

The Statistical Reliability Sampling program consists of conducting a series of stress tests on a 20 piece sample from each wafer lot (See Tables below). The stress tests are designed to detect any process shifts that could cause potential reliability problems.

Failure analysis is performed on each rejected sample in order to determine the failure mechanism. Once this has been established, the failure mechanism is then associated with a particular phase of the assembly process. When new failure mechanisms are discovered, design or assembly processes are changed accordingly.

Table I: SRS Program — Accelerated Tests

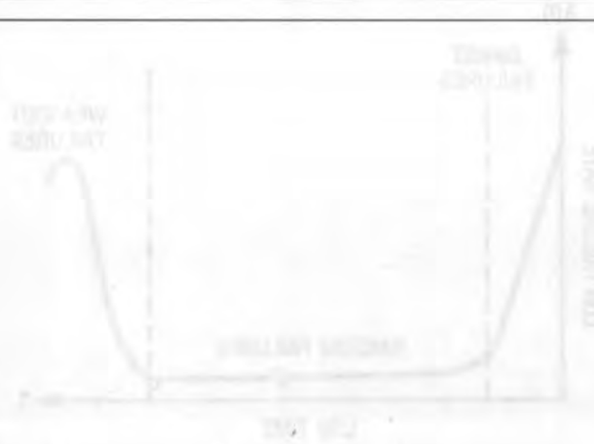
Test	Sample Size	Duration	Purpose
HTRB $T_j = 150°C$	5	12 hrs	Detect temperature dependent failure modes and any change in performance parameters with temperature.
Gate Stress	5	12 hrs	Check the reliability of the gate oxide and oxide/silicon interface.

Table II: SRS Program — Non-destructive Test

Test	Sample Size	Purpose
Thermal Resistance	10	Check integrity of header/ solder/die interface.

Table III: SRS Program — Destructive Test

Test	Sample Size	Purpose
Inductive Load (Avalanche Energy)	10	Check ability of part to handle inductive overloads.



3.0 Reliability Qualification

A new product or a redesign of an old product cannot be released to production until it is "qualified". This program serves different purposes depending on whether it is applied to a new design or to a design modification.

In a new design it uncovers potential latent defects and provides the initial data points of the long term reliability characterization.

In a new design modification it identifies the impact of the modification on the reliability of the device, thereby providing very valuable design feedback. As in the previous case, it also provides the statistical information for the long term reliability characterization.

The enclosed table lists the "core" tests for a qualification. The introduction of a new device, e.g. a new HEXFET die, designed according to well established design rules, would not require all the tests listed in the table. A radically new device may, on the other hand, require some additional tests, as appropriate to the technology employed.

Long Term Qualification Testing

TEST	CONDITIONS	DURATION	PURPOSE
HTRB	100% BV_{DSS} T_J=150°C or 175°C	1000 Hours	Stress Reverse Blocking Capabilities
Gate Stress	100% V_{GS}; V_{DS} = 0V T_J=150°C or 175°C	1000 Hours	Stress Time-Dependent Gate-Dielectric Breakdown
85/85 (Non-Hermetic Package)	V_{DS} = full bias (typ.); V_{GS} = 0, T_J = 85°C Humidity=85% RH	1000 Hours	Stress Moisture Withstanding Capabilities
Temperature Cycling	No Bias ΔT=205°C	1000 Cycles	Stress Die Attach & Wire Bond For Fatigue Degradation
Power Cycling	V_{DS} = 48V-80V; ΔT = 70°C	10,000 Cycles	Stress Wire Bond And Die Attach For Fatique Degradation

4.1 Customer Request For Failure Analysis

International Rectifier provides free failure analysis and applications consultation to its HEXFET customers. Our years of experience in performing in-depth analysis of HEXFETs and working closely with our customers on problem solving has been highly beneficial, both for our customers and for International Rectifier. We therefore encourage our customers to contact their sales representative for any support in device analysis or application involving HEXFETs should a problem arise.

Zener diode protection to prevent transient overvoltage or Electrostatic Discharge (ESD) damage is always recommended. Of equal importance in decreasing failures is an initial gate check immediately preceding and after any incoming Quality Assurance electrical tests.

Summary of the Failure Modes and Corrective Action References

This table summarizes the failure modes and typical causes associated with the customer requests for failure analysis. The causes were determined through follow-up investigation. The key failure parameters are the electrical measurements most likely to show degradation. The corrective actions, as well as a complete description of the failure modes, are covered in the indicated application notes.

FAILURE MODE	KEY FAILURE PARAMETER	TYPICAL CAUSE	APPLICATION NOTES FOR CORRECTIVE ACTION
Gate Short	IGSS	1. Excessive voltage applied to the gate	AN 936 AN 955 AN 937 AN 944
Safe Operating Area (SOA)	IGSS, BVDSS	1. Excessive thermal transient(s). 2. Improper heatsinking.	AN 936 AN 949
Avalanche (IL)	BVDSS	1. Excessive avalanche current from an inductor	AN 936 AN 934
Fused Leads	RDS(on)	1. Excessive transient current overload.	AN 936

References

1. HEXFET RELIABILITY QUARTERLY REPORT NO. 1; JANUARY 1983 (This report can be obtained by contacting the Applications Department at (213) 772-2000).
2. HEXFET RELIABILITY QUARTERLY REPORT NO. 2; 2ND QUARTER 1983 (This report can be obtained by contacting the Applications Department at (213) 772-2000).
3. Glaser, A. B. and Subak-Sharpe, G. E., *Integrated Circuit Engineering*: Reading, Massachusettes: Addison-Wesley Publishing Co., 1979.
4. Goldthwaite, L. R., "Failure Rate Study for the Lognormal Lifetime Model," *1961 Proceedings of the National Symposium on Reliability and Quality Control* pp. 208-213.