TDN: Temperature-Drift Nonlinearity— A New Dual-FET Specification

GETTING PREDICTABLE 5μV/°C MAXIMUM DRIFT FROM 50μV/°C TRAK-FET's

The most common application for dual FET's is as high-impedance inputs for instrument circuits. Quite often, they are used with IC op amps, functioning as an external high-impedance input stage (Figure 1). In such applications, the FET's picoampere-level bias current greatly reduces the drift that would be caused by the flow of the basic amplifier's bias current through high resistance paths. FET's can add substantial amounts of voltage drift, because — conventionally — they have been hard to match (or if well-matched, they are expensive or have some other problem.) This is unfortunate, because the basic amplifier is often capable of quite low voltage drift.

We discuss here briefly the devices resulting from a new FET process that not only provides excellent yields of low-leakage devices with low drift, but also allows the drift to be further reduced, in a predictable way, because of the linearity of offset with temperature.

More than a year ago, we introduced, in these pages* two families of monolithic matched-dual-FET's: the medium-geometry AD3954-8, with maximum gate current of 50pA, maximum offsets from 25-50mV, and maximum drifts from 5 to 100μV/°C; and the small-geometry AD5905-9, with maximum gate currents of 1pA, maximum offsets of 20-75mV, and maximum drifts from 5 to 75μV/°C.†

We also discussed the advantages they had over both two-chip hybrid assemblies (better tracking, better thermal transient rejection, lower cost), and interdigitated monolithics with common back gates (virtual elimination of bulk bias problems and gate-to-gate breakdowns). And we showed a number of examples of applications of dual FET's, including their use as input stages with low cost general-purpose op amps, such as the AD741.

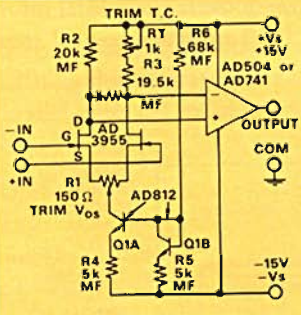


Figure 1. TRAK-FET Used in Differential Op Amp for < 5μV/°C Drift, 5pA Typ. I_b

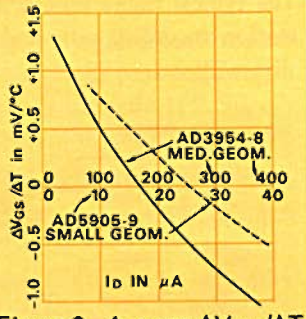


Figure 2. Average $\Delta V_{GS}/\Delta T$ vs Drain Current for Single FET Unit

Since then, a new process has been developed for manufacturing these FETs, using silicon nitride and low-dislocation diffusion techniques. The result is: better yields, lower leakage current (0.1pA *max* is routine for the AD830), less drift with temperature, and — of great importance — highly-linear drift with temperature, due to their superior tracking. The new devices bear the same type numbers and specifications as their earlier namesakes, are now available from stock (completely replacing the earlier devices), and they cost no more. In addition, they bear a new specification, *Temperature-Drift Nonlinearity (TDN)*, of 5μV/°C maximum (typically 1μV/°C), which allows the user the option of purchasing low-cost, moderate-drift (e.g., 50μV/°C) units and, with a modicum of "tweaking," obtaining 10:1 improvement routinely. We call these new FET's TRAK-FETs™.

OFFSET, DRIFT, AND TDN

Since single FET's have V_{GS} of 0.5 to 4 volts and $\Delta V_{GS}/\Delta T$ ranging from 0 to ±1mV/°C or worse (Figure 2), they are generally unsatisfactory for low-drift dc amplifier applications, even when great pains are taken to operate them at their "zero-drift" drain current. (Typical sensitivity of ½-AD3954 types to drain current is about 6.1μV/°C/μA, or 12.2μV/°C/% ΔI_D, and for ½-AD5909, 33μV/°C/μA, or 10μV/°C/% ΔI_D). When used in matched pairs, the initial dc offset $V_{GS\,1\text{-}2}$) is less than 50mV, typically 5mV, thermal drift ($\Delta V_{GS1\text{-}2}/\Delta T$, is less than 100μV/°C (Figure 3), typically 5μV/°C, and it is independent of small variations in drain current for equal drain currents.

Since the T.C. is a function of drain current, it ought to be possible to reduce temperature drift by unbalancing the drain currents. For example, if temperature drift for the pair, with equal currents, is 24μV/°C, then, in view of the typical 6.1μV/°C/μA sensitivity to drain current, a 4μA current unbalance should result in near-cancellation of drift . . . *if* the offset vs temperature curve is linear. (In fact, 3 different FET's, connected in the circuit of Figure 1, with initial drift rates of 50, 30, and 18μV/°C, turned up with 4.5, 2.5, and 1.5μV/°C when the *calculated* value of R_T required to furnish the current unbalance appropriate to each FET was used.)

This technique can obviously result in economies, since a user may purchase a less-tightly-selected FET, at considerably lower expense, and yet obtain premium performance, at the cost of obtaining initial drift data. In order to ensure that the FET's purchased by a user have adequate temperature-drift nonlinearity, (see Figure 4 for a qualitative comparison of essentially-linear monolithic TRAK-FET's and nonlinear hybrid

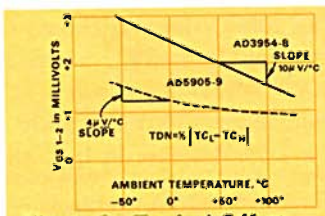


Figure 3. Typical Offset vs Temperature for Dual TRAK-FETS. Note Linearity (TDN's < 1μV/°C)

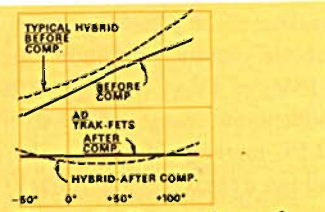


Figure 4. Comparison of Typical TRAK-FET's vs Hybrid FET's, With and Without Drift Compensation

*Analog Dialogue, Vol. 4, No. 2

†For complete technical data on Analog Devices' TRAK-FETs, use the reply card. Circle F18. For a more-detailed version of this design discussion, Circle F19

dual FET's) we define a *temperature-drift nonlinearity (TDN)* specification as follows:

$$TDN = \tfrac{1}{2} \mid TC_L - TC_H \mid$$

where TC_L is the average temperature coefficient from -55° to +25°C, and TC_H is the average temperature coefficient from +25° to +125°C. If it were possible precisely to null out the average temperature sensitivity over the entire range, the TDN would represent the remaining irreducible thermal drift. For nearly all grades of TRAK-FET's, the TDN specification is ±5μV/°C maximum, ±1μV/°C typical. *Maximum* TC is determined by the larger of TC_L or TC_H; *average* TC is one-half the sum of their magnitudes, with the polarity of the larger.

To enable the reader to grasp the full meaning of the TDN specification, the table indicates the limiting effect of the TDN specification on FET selection. The table lists a number of maximum TC's and TDN's for FET's that meet a ±50μV/°C specification. The units outlined in the unshaded area also meet a TDN specification of ±5μV/°C, and are therefore capable of being trimmed to within ±5μV/°C. To be sure of obtaining this kind of performance without the TDN specification, the user would have to specify the severely-restricted class of expensive units lying within the dashed lines.

TC_L or TC_H ↓	T_{CH} or T_{CL} → / PARAMETER	-50	-25	-10	-5	0	+5	+10	+25	+50
+50	TC	50	50	50	50	50	50	50	50	50
	TDN	50	37.5	30	27.5	25	22.5	20	12.5	0
+40	TC	50	40	40	40	40	40	40	40	50
	TDN	45	32.5	25	22.5	20	17.5	15	7.5	5
+30	TC	50	30	30	30	30	30	30	30	50
	TDN	40	27.5	20	17.5	15	12.5	10	2.5	10
+20	TC	50	25	20	20	20	20	20	25	50
	TDN	35	22.5	15	12.5	10	7.5	5	2.5	15
+10	TC	50	25	10	10	10	10	10	25	50
	TDN	30	17.5	10	7.5	5	2.5	0	7.5	20
+5	TC	50	25	10	5	5	5	10	25	50
	TDN	27.5	15	7.5	5	2.5	0	2.5	10	22.5
0	TC	50	25	10	5	0	5	10	25	50
	TDN	25	12.5	5	2.5	0	2.5	5	12.5	25
-5	TC	50	25	10	5	5	5	10	25	50
	TDN	22.5	10	2.5	0	2.5	5	7.5	15	27.5
-10	TC	50	25	10	10	10	10	10	25	50
	TDN	20	7.5	0	2.5	5	7.5	10	17.5	30
-20	TC	50	25	20	20	20	20	20	25	50
	TDN	15	2.5	5	7.5	10	12.5	15	22.5	35
-30	TC	50	30	30	30	30	30	30	30	50
	TDN	10	2.5	10	12.5	15	17.5	20	27.5	40
-40	TC	50	40	40	40	40	40	40	40	50
	TDN	5	7.5	15	17.5	20	22.5	25	32.5	45
-50	TC	50	50	50	50	50	50	50	50	50
	TDN	0	12.5	20	22.5	25	27.5	30	37.5	50

For the circuit of Figure 1, total drain current of 400μA is maintained constant by the current source, Q1, Q2. Since the op amp maintains the drains at very nearly equal voltage, the distribution of current between the two FET's depends on the resistances R_2 and $R_3 + R_T$. The 20kΩ value was chosen to obtain input common-mode swing of +5V minimum ($15V_S - 4V_{GS} - 2V_{DS} - 200\mu A \times 20k\Omega$). R_T allows a TC adjustment range of ±2.5%I_D, or about ±30μV/°C. Since a 2.5% increase of I_{D1} results in a 2.5% decrease in I_{D2}, this allows a total range of ±60μV/°C.

Adjust R1 for zero offset at 25°C, measure $\Delta V_{OS}/\Delta T$ over the desired temperature range, set R_T to the appropriate value, readjust R1 at room temperature, and confirm by measurement that the drift is within the predicted range.

EBR Uses 16-Bit DAC

4096 SCAN LINES WITH 5% SPACING-ERROR ALLOWS HIGH-RESOLUTION, HIGH-SPEED ELECTRON-BEAM RECORDINGS ON FILM

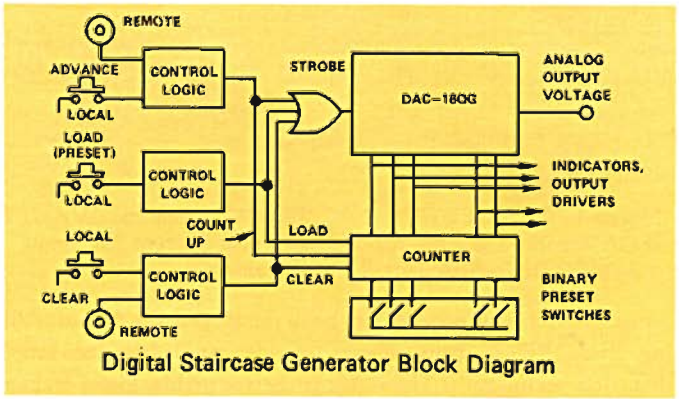
At CBS Laboratories, high-resolution electron-beam recording is accomplished by directing a controlled stream of electrons at a sensitive film in a vacuum. The electron beam is scanned horizontally, with stepwise vertical displacement of successive sweeps, and intensity modulation of the beam. The result is a latent image on film, which is subsequently developed. Thus, in this application, the EBR operates in much the same manner as the familiar TV raster, except that, in a typical system, there are 4,096 lines, with 8,192 data points/line, and 128 distinct "gray" levels. The image is formed on 70mm film with, typically, 2-micron line widths and 4μ interlinear spacing.

Since the developed film may be examined quite closely, and with considerable magnification, the spacing of the lines must be maintained within quite close tolerances, to avoid "gaps" and "banding," and to facilitate interpolation. A typical specification for line spacing tolerance is within ±5%.

The maximum tolerable vertical error is thus ±5% of 1/4096, or 1/82,000. If the vertical line-spacing is generated digitally, a 16-bit DAC with ±½LSB nonlinearity would have a maximum linearity error of 1/131,072, which is quite adequate. (½LSB of 15 bits would be 1/65,536, which is inadequate, and an ordinary "12-bit" converter, which might be implied by 4,096 lines, is out of the question.) Translated into actual voltage, for a ±5V range, the maximum allowable error is ±122μV.

The vertical scan is a 4,096-step voltage staircase, generated by a counter and the 12-most-significant bits of a DAC-16QG.* (For some projects, more steps are used, with tighter line-to-line spacing.) The counter may be advanced either manually (for test) or by a digital clock pulse; it may be cleared either manually or automatically; it may be preset to a desired initial value by a set of manual switches. The analog output scale factor and position are both adjustable.

The typical frame time is 2 minutes: 300kHz horizontal information recording rate, and 30ms dwell time per vertical step.



Digital Staircase Generator Block Diagram

Our thanks for this Application Note go to Marvin H. Gold, Senior Electronic Engineer at CBS Laboratories, Stamford, Connecticut.

*For information on Model DAC-16QG, use the reply card. Circle F8