

Design of Gate-Protected MOS Field-Effect Transistors

by L. A. Jacobus and S. Reich

MOS (metal-oxide-semiconductor) field-effect transistors are in demand for rf-amplifier applications because their transfer characteristics make possible significantly better performance than that experienced with other solid-state devices.^{1,2} Unless equipped with gate protection, however, MOS transistors require careful handling to prevent static discharges from rupturing the dielectric material that separates the gate from the channel. This Note describes the design of dual-gate MOS field-effect transistors that use a built-in signal-limiting diode structure to provide an effective short circuit to static discharge and limit high potential build-up across the gate insulation.

Breakdown Mechanism

Before the techniques of gate protection can be applied, the breakdown mechanism associated with gate destruction must be understood. For the sake of simplicity in exploring the breakdown mechanism, a single-gate structure is used. Fig. 1 shows this single-gate structure (a), its electrical symbol (b), and a much simplified equivalent circuit (c) that explains the possible static discharge paths within the device. The substrate diode is formed by the p-n junction integrated over the entire junction area, i.e., the source and drain diffusions connected by the inversion layer or n-type channel. Fig. 1 (c) lumps the diffuse diode into one equivalent diode terminating at the center of the channel.

C_{IN} in Fig. 1(c) represents the gate-to-channel capacitance, and R_1 and R_2 represent the channel resistance. R_3 is the leakage resistance associated with the substrate-to-channel equivalent diode D_1 . Leakage resistance across C_{IN} was intentionally deleted because it is more than a thousand orders of magnitude higher than R_3 . In a typical RCA MOS field-effect transistor (e.g., 3N128), C_{IN} is less than 5 picofarads. The channel resistance $R_1 + R_2$, which is a function of the applied bias, can range from 10^2 to 10^{10} ohms. R_3 is also subject to variations determined by operating conditions, but can be assumed to be in the order of 10^9 ohms. Thus, the application of a dc potential between the gate and any other element results in practically all of this potential being applied across C_{IN} .

In a dual-gate MOS field-effect transistor, the oxide thickness of the C_{IN} dielectric is about 600 angstroms. The dielectric material is SiO_2 , which has a breakdown constant of 5×10^6 volts per centimeter. The gate voltage-handling capability is therefore 30 volts. A cross-

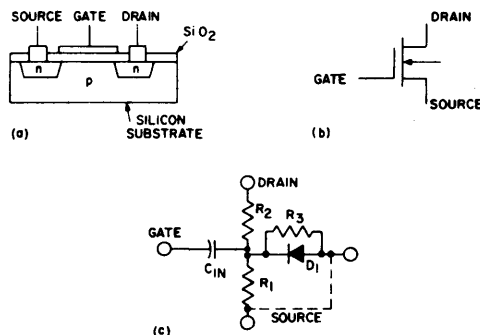


Fig. 1 - Single-gate MOS field-effect transistor: (a) structure; (b) electrical symbol; (c) simplified equivalent circuit.

section of a typical RCA dual-gate device is shown in Fig. 2 (a), and its schematic symbol in Fig. 2(b). The substrate in this structure is internally tied to the source; this connection is also shown schematically by the dotted line in Fig. 1 (c).

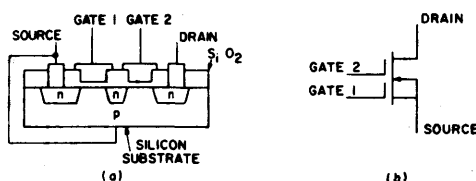


Fig. 2 - Dual-gate MOS field-effect transistor: (a) structure; (b) electrical symbol.

Static Discharge

If the potential applied to an MOS transistor were entirely within the control of the circuit designer, there would be no need for gate protection. Unfortunately, designers do not have complete control of the MOS field-effect transistor environment and static potentials do accumulate. These high potentials can inadvertently be discharged through the device when it is handled

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during the equipment manufacturing cycle or by a receiving antenna associated with the end product in which the transistor is used. The more severe of these conditions, in terms of percentage of units that suffer damage, is probably the initial handling phase.

Fig. 3 shows a simple equivalent circuit of a static discharge generator as it appears at the input of an MOS transistor. E_S represents the static potential stored in the static generator capacitor C_D . This voltage must be discharged through internal generator resistance R_S . Laboratory experiments have determined that a human body acts as a static (storage) generator with a capacitance C_D ranging from 100 to 200 picofarads and a resistance R_S greater than 1000 ohms. Although there is

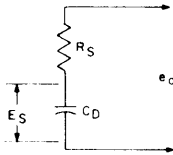


Fig. 3 - Equivalent circuit of a static discharge generator.

virtually no upper limit to the amount of static voltage that can be accumulated, repeated measurements suggest that the amount of potential stored is usually less than 1000 volts. Experience has also indicated that the potential from a static discharge is more severe during transistor handling than when the device is installed in a typical application. In an rf application, for example, a static potential picked up by the antenna would traverse an input circuit that normally provides a large degree of attenuation to the static surge before it appears at the input of the rf amplifier. For this reason, the development of gate-protected MOS transistors concentrated on the requirement that the devices be capable of withstanding the static discharges likely to occur during handling operations.

Gate-Protection Methods

It has been established above that in terms of a static discharge potential it is reasonable to represent the MOS transistor as a capacitor, such as C_{IN} in Fig. 4. The ideal situation in gate protection is to provide a signal-limiting configuration that allows for a signal such as that shown in Fig. 4(a) to be handled without clipping or distortion. The signal-limiting devices should limit all transient responses that exceed the gate breakdown voltage, as shown in Fig. 4(b). One possible means of securing proper limiting is to place a diode in parallel with C_{IN} , as shown in Fig. 4(c). Unfortunately, this arrangement causes several undesirable consequences. In terms of signal handling, the single diode clips the positive peaks of a sine wave such as that in Fig. 3(a) when the transistor is operated in the vicinity of zero bias. The 3N140 dual-gate MOS transistor, for example, is frequently operated with the rf signal superimposed on a slightly positive "bias" potential on gate No. 1. Furthermore, gate No. 2 of the 3N140 is designed to handle large positive and negative dc voltage swings from the agc loop. A single-diode arrangement would render this device useless for this type of circuit. It is important, therefore, that the limiting device be an effective open circuit to any incoming signals through the amplitude range of such signals. The best available method for accom-

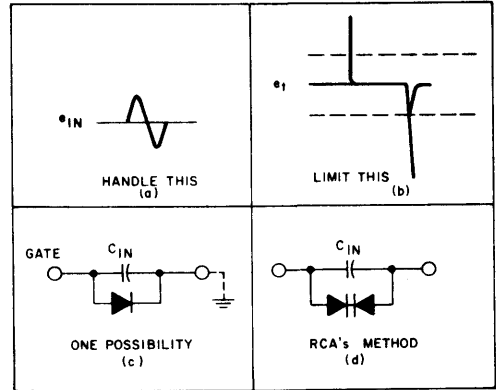


Fig. 4 - Gate-protection requirements and two solutions.

plishing this effective open circuit is the back-to-back diode arrangement pioneered by RCA and shown in Fig. 3(d).

Ideally, the transfer characteristic of the protective signal-limiting diodes has an infinite slope at limiting, as shown in Fig. 5(a). Under these conditions, the static potential generator in Fig. 5(b) discharges through its internal impedance R_S into the load represented by the signal-limiting diodes. The ideal signal-limiting diodes, with an infinite transfer slope ($R_S = 0$), would then limit the voltage presented to the gates to its knee value, e_d . The difference voltage $E - e_d = e_s$ (where E is the static potential in the static generator, e_d is the diode voltage drop, and e_s is the voltage drop across the generator internal resistance) appears as an IR drop across R_S , the internal impedance of the generator. The instantaneous value of the diode current is then equal to e_s/R_S . During handling, the practical range of this discharge varies from several milliamperes to several hundred milliamperes.

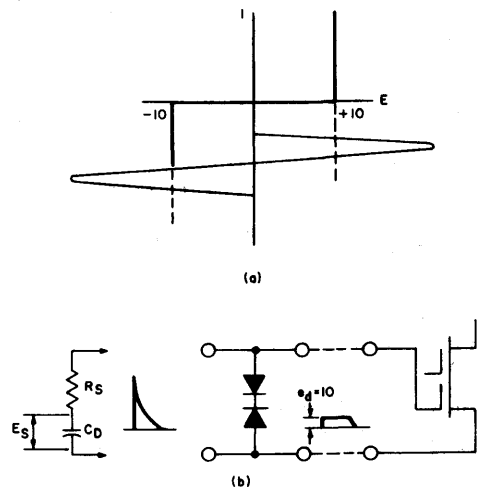


Fig. 5 - Transfer characteristic of protective diodes (a), and resulting waveforms in equivalent circuit (b).

Electrical Requirements

The previous discussion points out that optimum protection is afforded to the gate with a signal-limiting diode that exhibits zero resistance (i.e., an infinite transfer slope and fast turn-on time) to all high-level transients. In addition, the diode ideally adds no capacitance or loading to the rf input circuit.

The first phase in the development of gate-protected MOS field-effect transistors was, quite naturally, their construction in hybrid form. This form was used for initial measurements because it effectively enabled the physical separation of the diodes from the MOS pellet. This separation made it possible to measure the performance of the active device apart from the combined structure and thus obtain a more precise assessment of the loading effect of the diodes. The hybrid phase has now been followed by the development of monolithic gate-protected MOS field-effect transistors such as the RCA-40673. In this transistor, the diodes are an integral part of the MOS device and are internally connected as shown in Fig. 6.

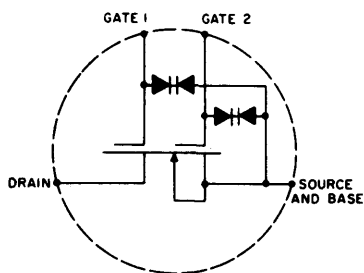


Fig. 6 - Connection of integral protective diodes in dual-gate MOS transistor.

Monolithic Gate-Protected MOS Transistors

In the design of a monolithic diode-protected MOS transistor, several factors must be taken into account. (1) The high-frequency performance of the device must be comparable to that of available unprotected units. (2) The device must be designed so that no additional assembly cost is incurred. (3) The silicon area must be used efficiently to provide the maximum number of devices per semiconductor wafer. (4) The diodes must provide adequate protection against the transients experienced primarily in handling but also when the transistor is finally installed in some piece of equipment.

One approach to integrating protective diodes into an MOS transistor structure on one chip is shown in Fig. 7. In this approach, the silicon substrate required for an n-channel depletion-type MOS device is the

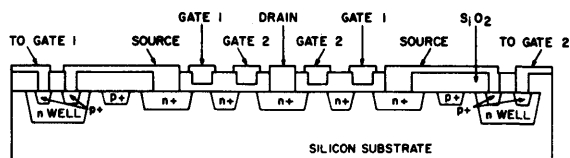


Fig. 7 - Structure of MOS transistor chip including protective diodes.

starting material. The n-type wells are diffused into the silicon to provide pockets for the protective devices. The surface concentration and depth of these wells are carefully controlled because both of these factors are important in determining diode characteristics.

The p⁺-type regions are diffused into the n-type wells to form the diodes and around the periphery to isolate the diode structure from the surface of the MOS device and to provide a region into which the channels may be terminated. The size of the diodes is determined by the desired current-handling capability and the amount of capacitance that can be tolerated across the gate of the MOS transistor. The spacing of the diodes is determined by the area available and the desired amount of control of transistor action from diode to diode. After the diode structures are formed, they are covered by a protective oxide. The MOS device is then fabricated by conventional means.

Fig. 8 shows a photograph of a completed monolithic diode-protected dual-gate MOS transistor. In this structure,

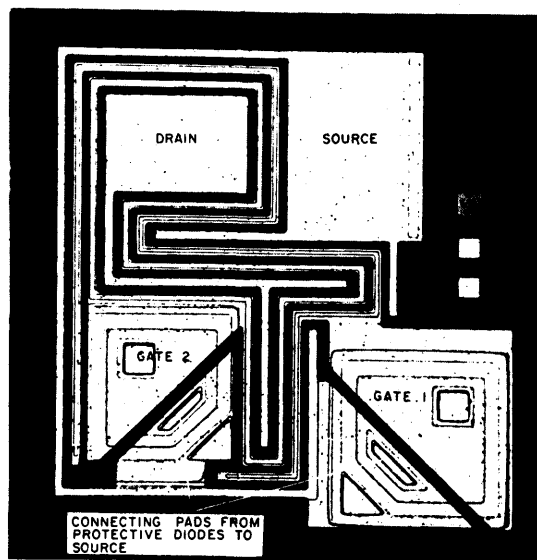


Fig. 8 - Completed monolithic diode-protected dual-gate MOS transistor.

one of the diodes of each pair has been located under the gate bonding pads. The small triangular metal pads

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make contact with the second diode of each pair and connect it to the source metalization. In assembly, the source is shorted to the substrate so that a low-resistance path to ground is provided for the diodes. To ground the diodes under the second gate properly, it is necessary to break the metal of the first gate and terminate the first channel on the p⁺-type guard band surrounding the diode structure of the second gate. This technique prevents spurious source-to-drain current which could result from the open nature of the structure.

Current-Handling Capability

Fig. 9 shows a typical diode transfer characteristic measured with a one-microsecond pulse width at a 4×10^{-3} duty cycle. The purpose of the protective diode is to limit the amplitude of the transient to a value that is below the gate breakdown voltage. Typically, a dual-gate transistor has a gate-to-source breakdown voltage rating of 20 volts. The curves in Fig. 9 show that the transfer characteristic of the signal-limiting diodes will constrain a transient impulse to potential values well below this 20-volt limit even when the input surge is capable of delivering hundreds of milliamperes.

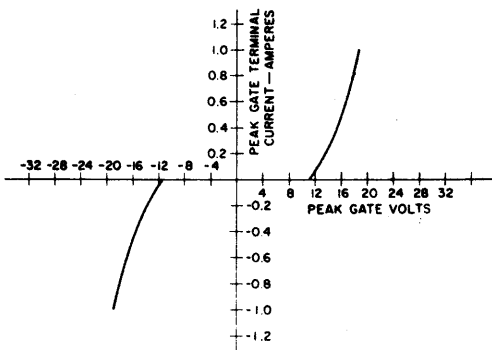


Fig. 9 - Typical diode transfer characteristic measured with 1-microsecond pulse width at 4×10^{-3} duty cycle.

The protection offered by the MOS signal-limiting diodes is more dramatically demonstrated when a gate-protected MOS transistor is compared to a high-frequency bipolar device. A laboratory experiment in which a static charge was accumulated in a capacitor and discharged through a circuit configuration like the one shown in Fig. 3 demonstrated that the special signal-limiting diodes made the protected-gate MOS field-effect transistor less vulnerable to static discharge damage than the bipolar transistor by a factor greater than two.

Input Capacitance and Resistance

The curves of input capacitance and input resistance as a function of drain current in Fig. 10 represent average readings taken from ten hybrid devices with diodes first connected and then disconnected (the readings for all ten devices were remarkably close to the averages). The curves indicate that the diodes increase input capacitance by about 2.5 picofarads and decrease input resistance by about 200 ohms.

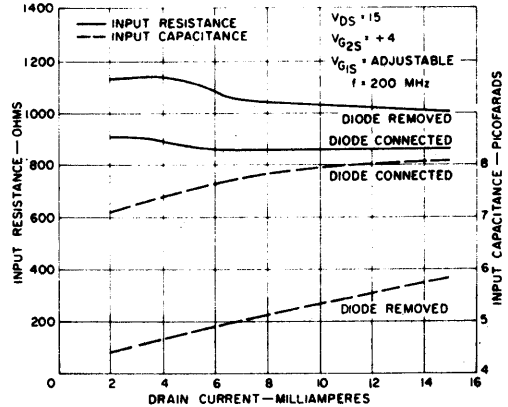


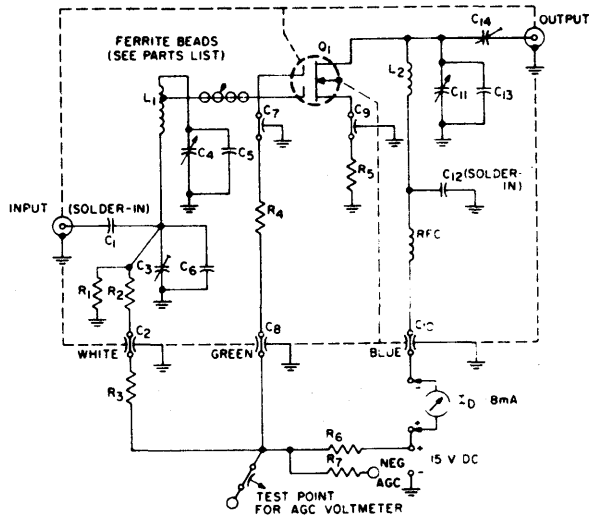
Fig. 10 - Input resistance and capacitances as a function of drain current for hybrid structures with and without diodes.

Power Gain and Noise Factor

In the final analysis, the question that must be answered is how the addition of the protective signal-limiting diodes affects circuit power gain and noise factor. Performance data taken on the ten units described above in the typical rf test circuit shown in Fig. 11 are given in Table 1. Noise-factor values show an average degradation of 0.25 dB when the diodes are connected. The power-gain values show that the change in this characteristic is insignificant.

Table 1 - Power Gain and Noise Factor at 200 MHz.

HYBRID UNIT	POWER GAIN (dB)		NOISE FACTOR (dB)	
	DIODES IN	DIODES REMOVED	DIODES IN	DIODES REMOVED
1	16.3	16.4	3.7	3.4
2	18.8	18.5	2.4	2.2
3	16.5	16.2	3.3	3.0
4	16.3	15.7	3.9	3.4
5	17.7	17.8	2.6	2.4
6	17.2	17.5	2.8	2.5
7	17.1	17.0	3.3	3.2
8	17.9	18.0	2.9	2.6
9	18.5	18.5	2.4	2.3
10	17.3	17.3	3.2	3.0



- C₁**: 100 picofarads, ceramic disc
C₂ C₇ C₈ C₉ C₁₀: 1000 picofarads, feed-through type
C₃: 1 to 10 picofarads, variable air (piston);
 JFD VAM-010, Johnson Co. No. 4335 or equivalent
C₄: 1.8 to 8.7 picofarads, variable air;
 Johnson Co. No. 160-104 or equivalent
C₅: 3 picofarads, tubular ceramic
C₆: 22 picofarads, ceramic disc
C₁₁: 1.5 to 5 picofarads, variable air;
 Johnson Co. No. 160-102 or equivalent
C₁₂: 100 picofarads, ceramic disc
C₁₃: 1.5 picofarads, tubular ceramic
C₁₄: 0.8 to 4.5 picofarads, variable air (piston);
 Erie 560-013 or equivalent

- Ferrite**: 4 beads on No. 24 wire between L₁ and socket; beads
 beads: are Pyroferrio Co. "Carbonyl J" or equivalent;
 0.093-inch OD, 0.03-inch ID, 0.063 inch thick
L₁: 4 turns 0.020-inch copper ribbon, silver-plated, 0.075 to
 0.085 inch wide, 0.25-inch inside diameter, coil
 approximately 0.80 inch long
L₂: 4.5 turns 0.020-inch copper ribbon, silver-plated, 0.085 to
 0.095 inch wide, 0.3125-inch inside diameter, coil approxi-
 mately 0.90 inch long
Q₁: MOS transistor under test
RFC: Ohmite part No. Z235
 or equivalent
R₁: 27,000 ohms
R₂: 47,000 ohms
R₃: 36,000 ohms
R₄: 1800 ohms
R₅: 275 ohms, ½ watt, 1%
R₆: 120,000 ohms
R₇: 1000 ohms

Fig. 11 - RF test circuit for dual-gate MOS transistors.

Conclusions

Gate-protected dual-gate MOS field-effect transistors such as the RCA-40673 make available to the circuit designer a device capable of good rf performance without the hazards previously associated with the handling and installation of MOS devices. Moreover, the gate protection is provided by signal-limiting diodes that do not significantly compromise dynamic range, noise factor, or power gain.

Acknowledgment

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