Depletion-Mode MOSFET: The Forgotten FET

*By Bill Chen, Field Application Engineer*

I. Introduction

For most practicing electrical engineers, the last time that they had contact with the Depletion mode MOSFET is in their undergraduate junior year. It is mentioned in class as another version of MOSFET that exists, but often there is no further mention of it. Here is a refresher on its properties and where it can be uniquely useful.

The Depletion-mode MOSFET is a cousin of the more familiar Enhancement-mode MOSFET.

The symbols for these devices are shown below:

DRAIN

GATE

SOURCE
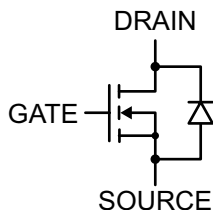
Enhancement-Mode FET

DRAIN

GATE

SOURCE
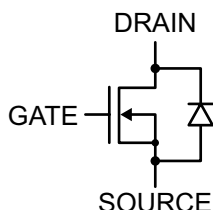
Depletion-Mode FET

Note that the Enhancement-mode FET symbol shows a broken (normally non-conducting) channel at zero gate bias, while the Depletion-mode FET symbol shows a normally conducting channel at zero gate bias.

Common properties:

- Majority carrier devices, therefore fast switching.
- Insulated gates, thus no bias current.
- Body diode that points from source to drain.
- Behave resistive when V_{DS} is near zero volts, with positive temperature coefficient.

Differentiating Properties:

- Enhancement FET does not conduct when $V_{GS} = 0$. Conduction starts when $V_{GS} = V_{GS(th)}$. Current increases as V_{GS} is increased beyond $V_{GS(th)}$.

- Depletion FET is conducting when $V_{GS} = 0$. The current decreases when $V_{GS} < 0$ until $V_{GS} = V_{GS(th)}$, when conduction stops. Current increases when $V_{GS} > 0$.

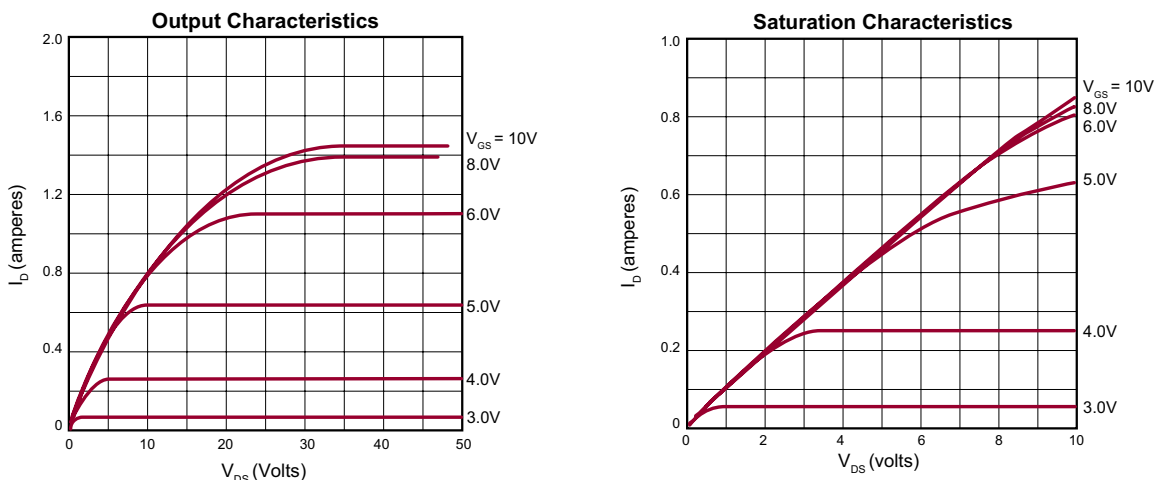These differences and similarities are visible in Figures 1 and 2.

Figure 1. Enhancement FET: TN2540 Output and Saturation Characteristics
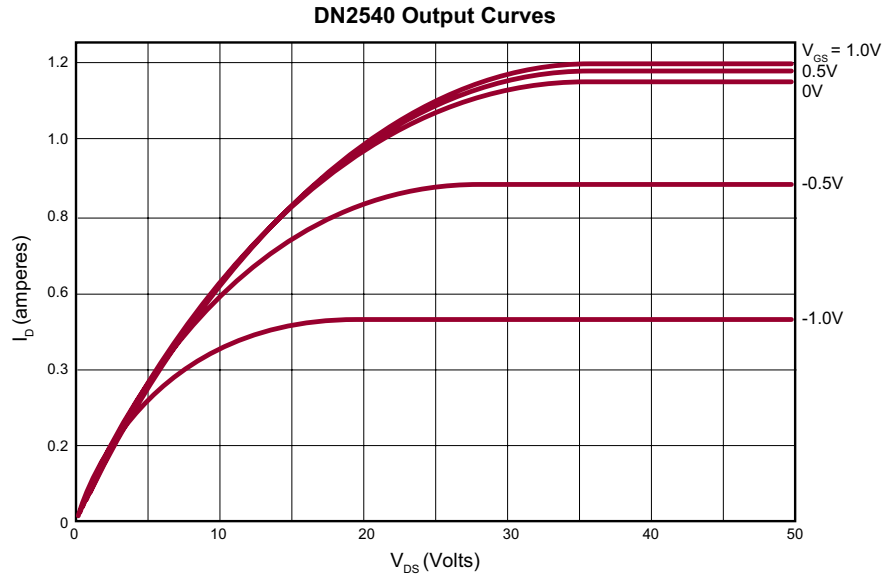
DN2540 Output Curves

Figure 2. Depletion FET: DN2540 Output Characteristics

Because of the "normally on" property of Depletion FET, there are some interesting and unique applications for it.

II. Unique Applications of Depletion Mode FETs

Figure 3. Constant Current Source

Figure 3 shows a constant current source using a Depletion FET and a resistor.

The current in the circuit is approximately $|V_{GS(th)}|$ / R1. The value of V_{GS}(th) is typically in the range of (-1.5V to -3.5V), thus the current is in the range of (1.5mA to 3.5mA). A variable resistor can be used to set the current to a specific value.

Applications:

1. The constant current source is useful to generate a bias current that is independent of the voltage across it.

2. It can be used to charge a capacitor at a constant rate, generating a linear ramp for timing purposes.

3. It can be used as a trickle charger to maintain battery charge state.

4. The constant current circuit can be used as a Current Limiter. When the current is below the current limit, the circuit shown in Figure 3 also behaves like a resistor with value of 1.01kΩ.
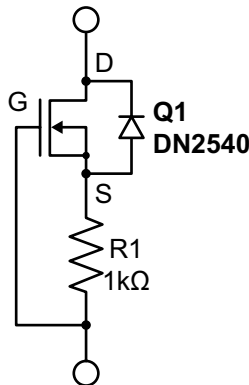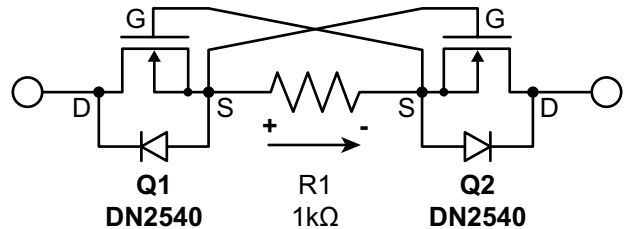

Figure 4. Bi-Directional Current Limiter

Figure 4 shows a Bi-directional current limiter. When the current is flowing from left to right as shown, the voltage across the R1 renders V_{GS} of Q1 negative. When the VR1 reaches $V_{GS(th)}$, Q1 goes into current limiting mode. In the meantime, the V_{GS} of Q2 is positive and Q2 behaves as a resistor of less than 10Ω.

When the current is flowing from right to left, the reverse of the above situation occurs and Q2 becomes the current limiting FET. This circuit is commonly used to protect test sensitive instruments that can be accidentally exposed to high voltage sources.
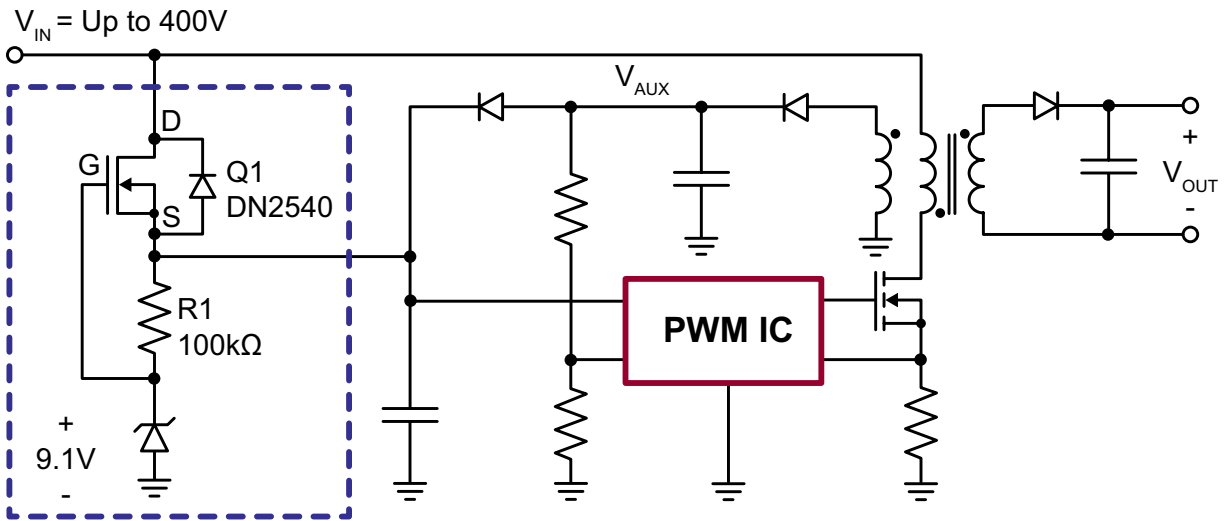
Figure 5. Starting Circuit for SMPS

Applications:

1. Portable testers / Volt meters input over-current protection.

2. Bed-of-nail In-circuit testers input over-current protection.

Many popular SMPS (switch-mode power supply) controller ICs require a local power supply of 10V to 16V to get started. Once the SMPS is up and running, the auxiliary winding will generate the 16V rail to keep the IC running. The Starting circuit will then go into dormant state to conserve power.

Figure 5 shows a starting circuit using a Depletion FET, a resistor and a Zener diode.

The Depletion FET and resistor circuit functions as a current limiter for the current in the Zener diode. The voltage at the source of the Depletion FET is at $V_Z + V_{GS(th)}$, approximately 10.5V. Once the SMPS is up and running, the V_{AUX} will be at 16V. The voltage at the source of the Depletion FET will be at 16V, while the voltage at the gate is 9.1V. Thus, the Depletion FET will be negatively biased by more than the gate threshold voltage and the FET will stop conducting. The starting circuit goes into the required dormant state, consuming almost no power. DN2540, as shown in Figure 5, is a 400V Depletion FET. Thus, the starting circuit can work up to 400V. If the power source is higher than 400V, the DN2540 can be replaced with a higher voltage rated FET.

All Supertex's PWM controllers and some LED drivers use high voltage depletion mode FET as the pass transistor for their internal linear regulator as shown on Figure 6.
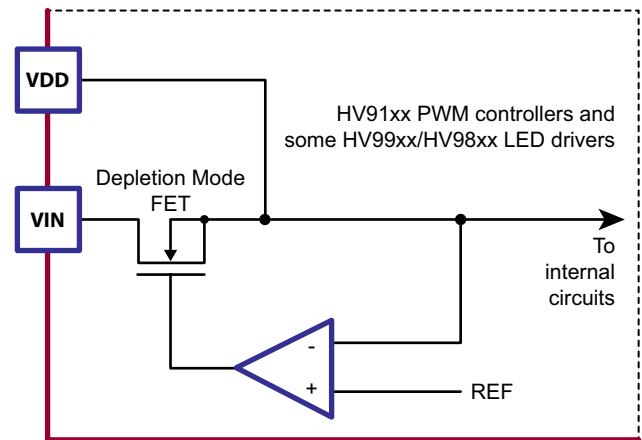

Figure 6. Internal Linear Regulator using Depletion Mode FET

Supertex's HV91xx PWM Controllers and some HV99xx/ HV98xx LED drivers can be powered directly from its VIN pin and can work from a high voltage input up to 450V (for some devices) at its VIN pin. When a voltage is applied at the VIN pin, the HV91xx and some of the HV99xx/HV98xx maintains a constant voltage at the VDD pin. The VDD voltage is set by the internal REF voltage. The voltage at the VDD pin is used to power the IC and any external, low current circuit, needed to control the IC.

An external voltage source that is greater than the internally regulated voltage can also be connected to the VDD pin to operate the HV91xx and some HV99xx/HV98xx. This will turn off the internal regulator of the IC and then the IC will operate directly off of the voltage supplied at the VDD pin. Please note that this external voltage at the VDD pin should not exceed the absolute maximum rating of the respective VDD pin.

Being able to turn off the internal regulator by applying an external voltage or boot-strap winding that is higher than the VDD is beneficial, especially for line powered application, as this minimizes the power dissipation of the IC.
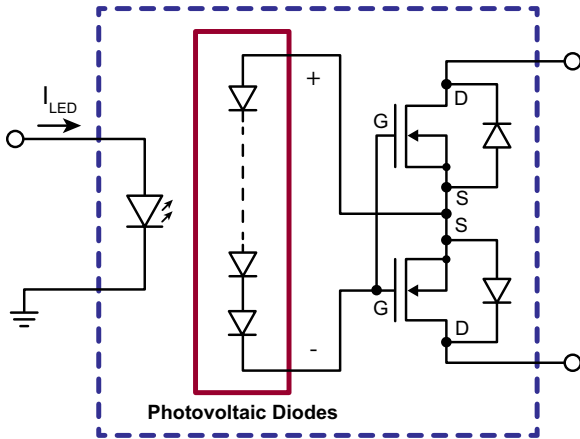

Figure 7. Normally-On Solid State Relay

A normally-on solid state relay can be constructed using Depletion FETs as the contact elements, as shown in Figure 7. The Depletion FETs are connected back-to-back, with their sources and gates tied together. The gate and source terminals are driven by the photo voltaic diode string, which in turn is driven by the LED diode.

When ILED is off, there is no photo voltaic voltage generated. V_{GS} = 0. The Depletion FETs are in the conducting state and the relay is in the on state..

When ILED is on, a photo voltaic voltage is generated with sufficient magnitude to turn the depletion FETs off, rendering the relay in the off-state.
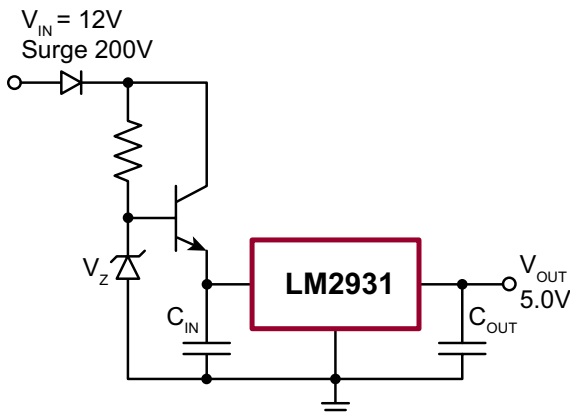

Figure 8. Linear Regulator, Surge Protected to 200V V$_{IN}$ using Transistor/Zener/Resistor Clamp

Low Drop-Out (LDO) linear regulators are often used to provide a stable low voltage, say 5V, to power electronic

circuits. The power source is often nominally 14V but can vary, from 8V to 100V, for a short duration.

Most LDO will function properly up to an upper limit of 30V. Beyond that, LDO will self-protect by shutting down. In situations that require the LDO to provide continuous output, an input protection circuit will be needed.

Figure 8 shows a typical voltage clamp circuit. The circuit consists of a power resistor, a Zener diode and a bipolar transistor. The bipolar transistor is used as an emitter follower. When the input is below the clamp Zener voltage, the resistor biases the transistor on, and the transistor operates in saturation. Approximately 0.2V is dropped across the transistor. When the input voltage surges up beyond the Zener voltage, the Zener clamps the base of the transistor at Vz, and the emitter of the transistor is clamped at one diode voltage below the Vz. Thus, the LDO never sees any voltage beyond the Zener voltage.

For the duration of the clamp action, the transistor absorbs the surge voltage and carries the output current, and power is dissipated in the transistor. The transistor must be sized to withstand the power dissipation for the duration of the voltage surge.
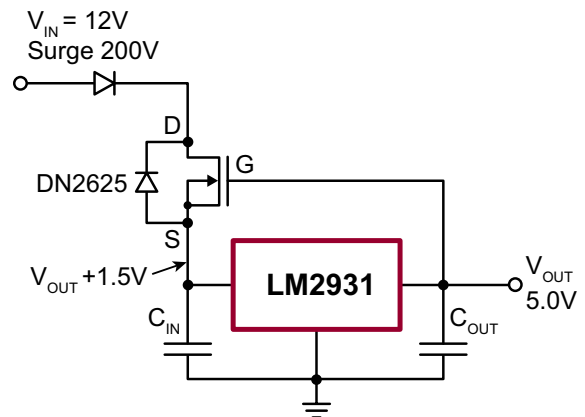

Figure 9. Linear Regulator, Surge Protected to 200V V$_{IN}$ using Depletion Mode MOSFET

A much simpler solution is to use a Depletion-mode MOSFET, as shown in Figure 9. The gate of the depletion FET, a DN2625, is connected to V$_{OUT}$. The source is connected to the input of the LDO, LM2931. The load current flows from V$_{IN}$ through the DN2625 and the LDO to the load. At I$_{OUT}$ = 100mA, the DN2625 is operating at V$_{GS}$ of -1.5V. Thus, V$_{SOURCE}$ is at V$_{OUT}$ +1.5V, well above the LDO drop out requirement. Since there is voltage across and current through the FET, power is being dissipated in the FET. An appropriate package must be chosen to dissipate the power.

III. References:

The applications shown above are example circuits making use of the unique properties of the Depletion FETs. More examples can be found in the references below.

Supertex Application Notes:

AN-D10:   Off-Line Compact Universal Linear Regulator.

AN-D11:   +/- 500V Protection Circuit.

AN-D12:   High Voltage Ramp Generator.

AN-D16:   High Voltage Regulators and Linear Circuits using LND1.

AN-D17:   High Voltage Off-Line Linear Regulator.

AN-D18:   High Voltage Regulators and Linear Circuits using DN25.

AN-D25:   Efficient Switch-mode Power Supply Start-Up Circuit.

AN-D26:   High Voltage Isolated MOSFET driver.

AN-D30:   Off-Line 5.0V Output Non-Isolated Linear Regulator

These documents can be found at the Supertex website:

www.supertex.com

Supertex inc.

1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com