AN-3193

Application Considerations for the RCA 3N128 VHF MOS Field-Effect Transistor

by

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Early MOS field-effect transistors were intended primarily for low-frequency applications in which their extremely high input impedance is advantageous,* and were not designed to be useful in the vhf range (30 to 300 MHz). Recently, however, RCA has developed high-frequency MOS transistors that exhibit high gain and low noise at vhf, together with very low feedback capacitance and cross-modulation distortion that approaches the low levels of electron tubes. The low level of cross-modulation distortion is a particularly important characteristic in view of the increasing congestion of the communications frequency bands.

This note describes applications and vhf circuit considerations for a new high-frequency n-channel MOS field-effect transistor, the RCA 3N128. Biasing requirements and basic circuit configurations are discussed, and selection of the optimum operating point and methods of automatic gain control are explained. The cross-modulation and intermodulation distortion characteristics of the 3N128 MOS transistor are compared to those of bipolar transistors, and procedures are given for the design of a practical vhf amplifier that uses the 3N128.

Biasing Requirements and Circuit Configurations

The biasing requirements and operating characteristics of an n-channel MOS transistor such as the 3N128 are similar to those of an electron tube. For example, the 3N128 uses positive drain voltages and usually negative gate voltages which are analogous to the plate and grid voltages, respectively, of electron tubes. In addition, the current-voltage characteristics of the 3N128, shown in Fig.1, are similar to those of a pentode tube. An electron-tube analogy, therefore, can be useful in the analysis of the n-channel 3N128 MOS transistor.†

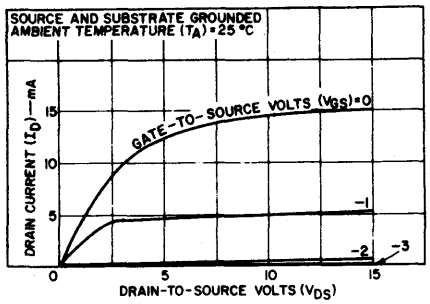


Fig.1 - Transfer characteristics for the RCA 3N128 vhf MOS transistor.

Although their characteristics are similar, MOS transistors have several important advantages over electron tubes. They can be operated at the low voltages typical of bipolar transistors. The dc gate current of MOS transistors is substantially less than the

* The basic theory of MOS transistors and equivalent circuits for these devices are discussed in RCA Application Note AN-201, "Application Considerations for RCA 3N98 and 3N99 Silicon MOS Transistors," by D. M. Griswold.

† The electron-tube analogy does not apply to p-channel MOS transistors or to enhancement types.

grid current of most electron tubes. In addition, the MOS transistor requires no heat-generating filament.

MOS transistors are most often used in the common-source type of circuit configuration. Fig.2 shows three basic methods of dc-biasing an MOS transistor in a common-source circuit. MOS transistors may also be used in common-gate or common-drain (source-follower) configurations.[2] These circuits are not widely used in vhf applications, however, because their gain is low at high frequencies.

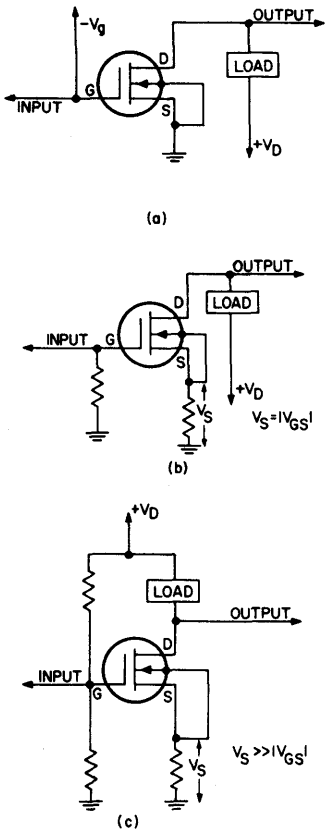
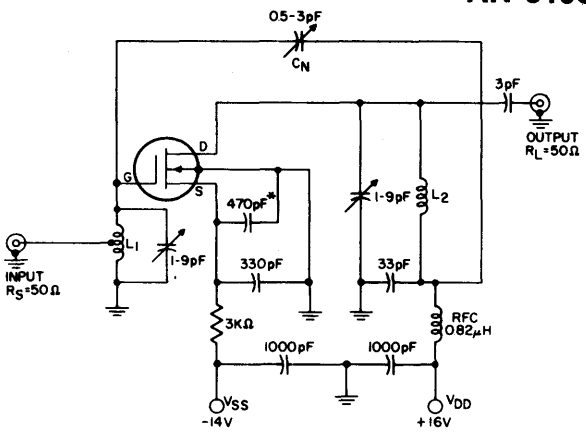


Fig.2 - Bias methods for common-source MOS transistor stages: (a) fixed bias; (b) source-resistor bias; (c) constant-current bias.

Fig.3 shows a 200-MHz common-source amplifier used to measure the rf power gain of the MOS transistor. This amplifier uses a modified form of the constant-current biasing arrangement shown in Fig.2(c). With this modified biasing arrangement, both the insulated gate and the case of the MOS transistor are operated at dc ground potential. The insulated gate should always have a dc path to ground even if the path is through a multimegohm resistor. If the gate is allowed to float, the resultant dc bias conditions may be unpredictable and possibly harmful.



L_1 = 4-1/2 turns of No.20 wire, 3/16 inch in dia., 1/2 inch long, tapped at 1 turn

L_2 = 3-1/2 turns of No.20 wire, 3/8 inch in dia., 1/2 inch long

* Leadless disc capacitor

Fig.3 - 200-MHz common-source amplifier.

Fig.4 illustrates the effect of the leakage resistances R_{L1} and R_{L2} when the insulated gate is floating. When these resistances ($\approx 10^{14}$ ohms) are approximately equal, they form a voltage divider which biases the insulated gate at $+V_{DD}/2$. This value of bias voltage may exceed the maximum rating for positive gate voltage and, in addition, may cause an excessive flow of drain current.

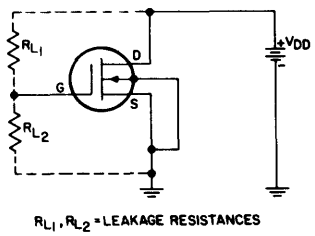


Fig.4 - Bias conditions for an MOS transistor when the insulated gate is floating.

The cascode configuration represents a useful variation of common-source circuit. In this configuration, a common-source-connected MOS transistor is used in the lower section of the cascode, and a common-gate-connected MOS transistor is used in the upper section. Fig.5 shows the use of MOS transistors in a 200-MHz cascode amplifier. This circuit normally requires a negative voltage on the gate of Q_1, a positive voltage on the gate of Q_2, and approximately equal drain-to-source voltages for each transistor. Although the gate of Q_2 may require a positive voltage of 5 to 10 volts, the net gate-to-source voltage for this transistor should be approximately 0 to -1 volt.

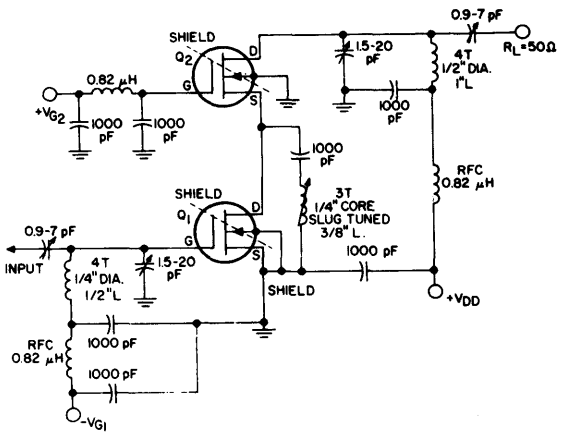


Fig.5 - 200-MHz cascode amplifier.

Selection of Operating Point

The operating point selected determines the power gain, noise figure, power dissipation, and, where applicable, battery life. In many applications, a compromise between gain and available supply voltages or battery lifetime is necessary. Knowledge of the variation in gain and noise figure as functions of voltage and current is essential, therefore, before an operating point can be selected.

The 3N128 provides maximum rf power gain at a drain-to-source voltage V_{DS} of approximately 20 volts and a drain current I_D of about 5 milliamperes. The transistor also exhibits a minimum noise figure at a V_{DS} of 20 volts for a drain current of about 2 milliamperes. The difference in the noise figures obtained at 2 milliamperes and at 5 milliamperes, however, is very small (usually between 0 and 0.2 dB) and generally is not a significant factor in the selection of the operating point. Although a V_{DS} of 20 volts represents the optimum value for the 3N128 in terms of both rf power gain and noise figure, this value is also the maximum V_{DS} rating for the transistor. Greater long-term reliability is achieved, therefore, by operation of the 3N128 at a V_{DS} of 12 to 15 volts rather than at 20 volts.

For a V_{DS} of 15 volts and an I_D of 5 milliamperes, the 3N128 typically provides a power gain of 18 dB and a noise figure of 4 dB at 200 MHz. Operation of the 3N128 at considerably lower drain currents, such as those normally employed in battery-powered equipment, does not seriously affect system performance. For example, when the transistor is operated at a V_{DS} of 15 volts and an I_D of only 1 milliampere, the power gain and noise figure at 200 MHz are typically 15.5 dB and 4.5 dB, respectively. Because the MOS transistor is a voltage-controlled device, its performance for a given power dissipation can often be improved by operation at high voltage and low current levels. At a power dissipation of 30 milliwatts, for example, the 3N128 typically provides a power gain of 17.3 dB and a noise figure of 3.9 dB when operated at 15 volts and 2 milliamperes. At the same dissipation level, however, the power gain is reduced to 14.6 dB and the noise figure is increased to 4.7 dB when the 3N128 is operated at 6 volts and 5 milliamperes. Fig.6 shows the variations in power gain and noise figure of the 3N128 as functions of the drain current and voltage.

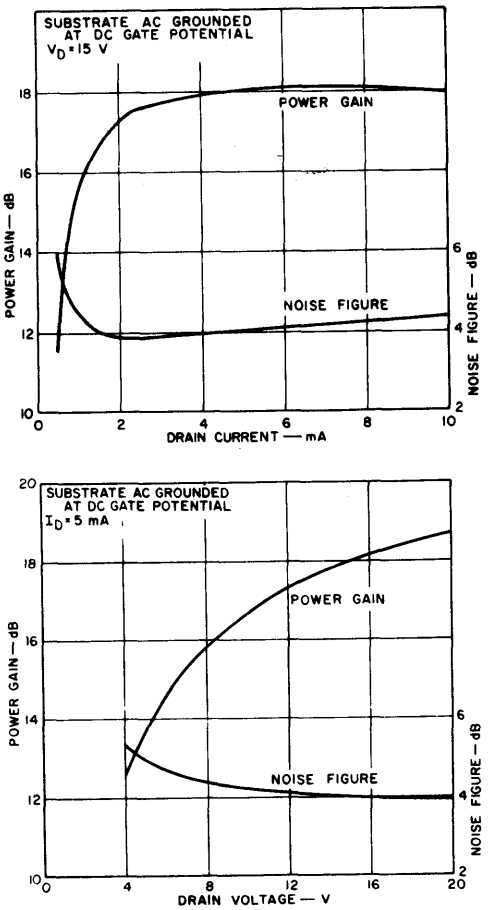


Fig.6 - Power gain and noise figure of the RCA 3N128 at 200 MHz as functions of drain current and voltage.

A gate voltage V_G of between -0.5 and -2 volts is normally required to bias a 3N128 for operation at a drain voltage V_D of 15 volts and a drain current I_D of 5 milliamperes. If a fixed-bias circuit, as shown in Fig.2(a), is used, the value of the gate voltage must be adjustable to compensate for variations among individual transistors. For the source-resistance bias circuit shown in Fig.2(b) the value of the biasing resistor should be 200 ohms (5 mA x 200 ohms = 1 volt). The source-resistance circuit will limit the variations in current among the different transistors to approximately

50 per cent. With the constant-current bias circuit shown in Fig.2(c), variations in current from one transistor to another can easily be limited to less than 10 per cent. Regardless of the bias circuit or the bias point selected, there is no danger of thermal runaway with the 3N128 because this transistor has a negative temperature coefficient at the zero-gate-bias point. In the selection of the bias circuit for an MOS transistor stage in which automatic gain control is employed, consideration should be given to the following principle: The more restrictive the tolerance imposed on quiescent operating-point current, the more difficult automatic gain control of the stage becomes because the self-compensating action of the constant-current bias circuit also resists current changes that result from the agc action.

AGC Methods

When it is necessary to employ agc in an MOS transistor stage, either of two methods may be used to reduce transistor gain. In one method, referred to as reverse agc, the reduction in gain is accomplished by an increase in negative gate bias. In the other method, the gain is decreased by reduction of the drain-to-source voltage.

In the reverse agc method, the application of higher negative voltage to the gate reduces the drain current and the transconductance of the transistor. The low feedthrough capacitance of the 3N128 (typically about 0.13 picofarad) usually permits more than 30 dB of gain reduction at frequencies up to 200 MHz. Substantially greater gain reduction can be achieved at lower frequencies or in neutralized amplifier circuits.

Gain reduction achieved by the decrease of drain-to-source voltage is usually controlled by a variable impedance in series, or in shunt, with the MOS transistor. The variable impedance may be another MOS transistor or a bipolar transistor. A major disadvantage of this method is that the MOS feedback capacitance rises by a factor of 4 or 6 times as V_D approaches zero. This increase in capacitance reduces the agc range obtainable and decreases the effectiveness of a fixed neutralization network. In addition, the output impedance of the 3N128 decreases with a reduction in the drain voltage.

In the cascode circuit, agc is accomplished most effectively by application of a negative voltage to the gate of the upper (common-gate) section. A wide agc range can be obtained in this circuit. Gain reductions greater than 45 dB at 200 MHz or 65 dB at 60 MHz are realizable in an unneutralized cascode circuit.

RF Considerations

One of the prime advantages of the 3N128 MOS transistor over bipolar transistors is its superior cross-modulation, intermodulation, and modulation distortion performance. The 3N128 has considerably lower feedback capacitance than junction-gate field-effect transistors. In addition, the 3N128 maintains a high input resistance at frequencies well into the vhf range (the real part of the input admittance, $Re(y_{11}) = 0.15$ mmho at 100 MHz).

At maximum gain, the cross-modulation distortion of the 3N128 is approximately one-tenth that of most bipolar transistors, or roughly comparable to the cross-modulation performance of vacuum tubes (at 200 MHz, an interfering signal of approximately 80 millivolts is required to produce cross-modulation distortion of 1 per cent). However, cross-modulation susceptibility changes as the gain of the stage is changed. For a single 3N128, the cross-modulation distortion increases when reverse agc is applied; the distortion is also increased, but to a lesser extent, if agc action is achieved by reduction of the drain-to-source voltage. A deterioration in cross-modulation performance at high attenuation results from the fact that the MOS triode is a sharp-cutoff device; as a result, large non-linearities occur near "pinch-off." Beyond "pinch-off," the transadmittance depends primarily upon the capacitive feedthrough, which does not have large third-order non-linearities. Cross-modulation performance at the extreme limits of attenuation, therefore, is very good.[1] In cascode stages, the effect of reverse agc on cross-modulation distortion is reduced when the agc is applied to the gate of the common-gate stage; application of reverse bias to the gate of the common-source stage results in cross-modulation performance similar to that of a single triode-connected stage. Figs.7 and 8 show the variation in cross-modulation susceptibility as a function of agc. The test circuits used to measure cross-modulation distortion of MOS transistors are shown in Fig.9.

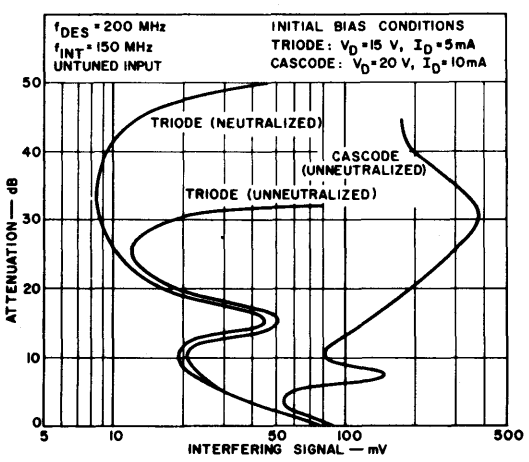


Fig.7 - Cross-modulation distortion as a function of the attenuation produced by reverse agc.

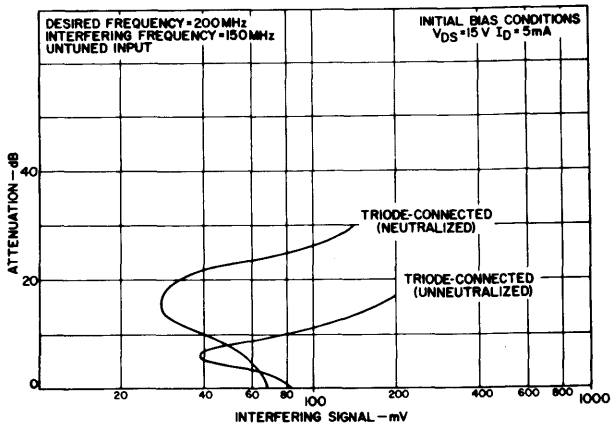


Fig.8 - Cross-modulation distortion as a function of the attenuation produced when agc is accomplished by a reduction of drain-to-source voltage.

The test circuit shown in Fig. 10 is used to measure the intermodulation distortion of MOS transistors. In such measurements, the receiver is tuned to 150 MHz. The MOS is then inserted, and bias voltages are applied. When no signals are applied (i.e., the amplitudes of the signals f_1 and f_2 are both 0 volts), the rf indicator of the receiver indicates an equivalent input noise level of approximately 2.4 microvolts. The signals f_1 and f_2 are gradually increased in amplitude until the reading on the rf indicator is 1 microvolt above the noise level (3.4 microvolts total). This reading indicates that 2.4 microvolts of 150-MHz signal is being produced by the interaction of f_1 and f_2 (i.e., $2f_1 - f_2 = 150$ MHz). Table I lists the dc bias levels used for the 3N128 MOS transistor and the amplitude of the f_1 and f_2 signals required to produce an output, at 150 MHz, of 2.4 microvolts, which corresponds to 1 microvolt above the input noise level. The amplitudes of f_1 and f_2 were measured by an rf vacuum-tube voltmeter; the f_1 generator was turned down for measurement of f_2, and vice versa.

Table I

INTERMODULATION DISTORTION DATA FOR THE 3N128 MOS TRANSISTOR

		Interfering Voltages Required to Produce 2.4 microvolts at 150 MHz	
V_D volts	I_D mA	f_1 (175 MHz) mV	f_2 (200 MHz) mV
16.5	10	18	18
16.5	10	7	150
16.5	5	15	15
16.5	5	3.5	150
16.5	5	30	3.5
16.5	2.5	19	21

When the same test methods were used to measure the intermodulation distortion of bipolar transistors, distortion levels were found to be two to five times greater than those of the 3N128 MOS transistor.

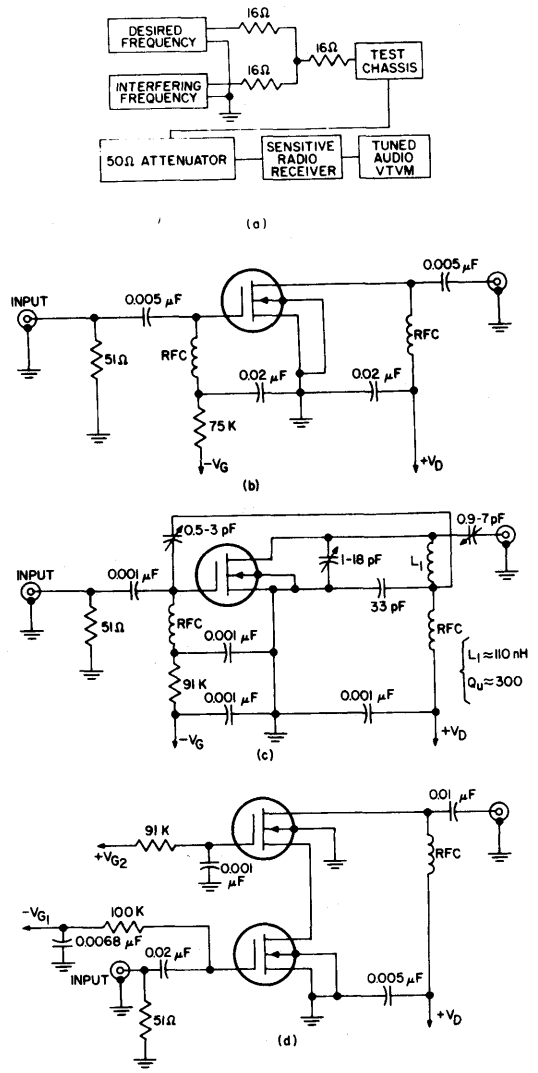


Fig.9 - Test circuits used to measure cross-modulation distortion in MOS transistors: (a) block diagram; (b) unneutralized-stage test circuit; (c) neutralized-stage test circuit; (d) cascode-stage test circuit.

Designing VHF MOS Amplifier Circuits

A complete set of graphs of typical y parameters, both as a function of frequency at constant bias and as as a function of bias at constant frequency, are given in the published data for the 3N128 MOS transistor. The application of these y parameters in the design of the 200-MHz amplifier shown in Fig.3 is discussed in following paragraphs.

For operation at a frequency of 200 MHz, an I_D of

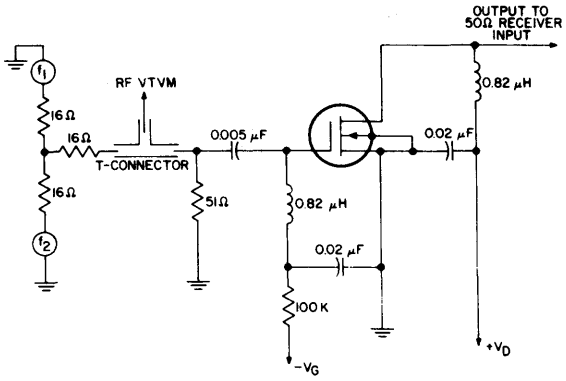


Fig.10 - Test circuit used to measure intermodulation distortion in MOS transistors.

5 milliamperes, and a V_D of 15 volts, the y parameters of the 3N128 are typically as follows:

y_{11} (input admittance with output short-circuited) = 0.45 + j7.2 mmhos

y_{22} (output admittance with input short-circuited) = 0.28 + j1.75 mmhos

y_{21} (forward transfer admittance with output short-circuited) = 7.0 - j1.9 mmhos

y_{12} (reverse transfer admittance with input short-circuited) = 0 - j0.16 mmhos

If y_{12} is assumed to be zero, the maximum available power gain (MAG) under conjugately matched conditions,* may be computed. MAG serves as a useful figure of merit for comparison of the vhf power gain of various MOS transistors. The MAG for the 3N128 is determined as follows:

$$MAG = \frac{|y_{21}|^2}{4Re(y_{11})Re(y_{22})} = \frac{|7.0-j1.9|^2}{4(0.45)(0.28)} = 104 = 20.2\,dB \quad (1)$$

where Re means "the real part of."

All MOS transistors have a small, but measurable, feedback component (y_{12}); it is possible, therefore, that some of them will oscillate under certain circuit conditions. This possibility may be checked by use of methods given by Linvill[2,4] and by Stern.[3,4] If the transistor is unconditionally stable for any combination of passive source and load admittances, then Linvill's critical stability factor C, as determined from the following equation, is less than |1|:

$$C = \frac{|y_{21}y_{12}|}{2Re(y_{11})Re(y_{22}) - Re(y_{21}y_{12})} \quad (2)$$

The critical stability factor for the 3N128 is calculated as follows:

$$C = \frac{|(7.0-j1.9)(0-j0.16)|}{2(0.45)(0.28) - Re(7.0-j1.9)(-j0.16)} = 2.08$$

Stern has derived a similar expression for stability C_S that includes the effect of the generator and load conductances, y_g and y_L, respectively, as follows:

$$C_S = \frac{|y_{21}y_{12}|}{2\,Re(y_{11}+y_g)Re(y_{22}+y_L) - Re(y_{21}y_{12})} < |1| \quad (3)$$

If a conjugate match is assumed at both the input and the output, then $Re(y_g) = Re(y_{11})$, and $Re(y_L) = Re(y_{22})$. For this condition, the stability factor is calculated as follows:

$$C_S = \frac{|(7.0-j1.9)(-j0.16)|}{2(0.45+0.45)(0.28+0.28) - Re(7.0-j1.9)(-j0.16)} = \frac{1.16}{1.31} = 0.885$$

These calculations show that the transistor itself is not unconditionally stable, but that it is stable when placed in a conjugately matched circuit. Therefore, neutralization is not required, although it may be used if a more symmetrical pass-band characteristic is desired. All unneutralized amplifiers have a certain amount of skew in the selectivity characteristic; if this skewness becomes objectionable for the required application, then neutralization (or mis-matching) is necessary.

When neutralization is desired, there are two common methods of obtaining the required feedback. The first, and more common method, is the capacitance-bridge technique shown in Fig.11(a). The capacitance bridge becomes more apparent when the circuit is redrawn as shown in Fig.11(b). The condition for neutral-

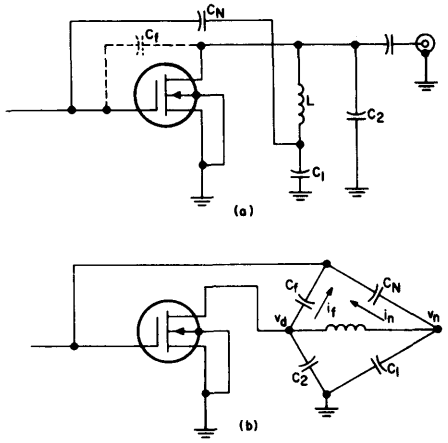


Fig.11 - Capacitance-bridge neutralization circuit: (a) actual circuit configuration; (b) circuit redrawn to emphasize capacitance-bridge network.

* Conjugate match means that the transistor input and the generator and the transistor output and load are matched resistively and that all reactance is tuned out.

ization is that $i_f = i_n$. This condition implies the following relationship:

$$\frac{v_d}{jX_f} = \frac{-v_n}{jX_n}, \text{ or } C_f v_d = -C_n v_n \quad (4)$$

The voltage v_n is defined by the following equation:

$$v_n = \left(\frac{v_d}{jX_L + jX_1}\right) jX_1 = \left(\frac{v_d}{\frac{-\omega^2 LC_1 + 1}{j\omega C_1}}\right) \frac{1}{j\omega C_1} = \frac{v_d}{-\omega^2 LC_1 + 1} \quad (5)$$

If this relationship for v_n is substituted in Eq.(4), the following result is obtained:

$$C_f v_d = -C_n \left(\frac{v_d}{-\omega^2 LC_1 + 1}\right), \text{ or } C_n = -C_f(-\omega^2 LC_1 + 1) \quad (6)$$

At resonance, the equation for the neutralization capacitance C_n may be rewritten as follows:

$$C_n = -C_f\left[\left(\frac{-1}{\omega C_2}\right)\omega C_1 + 1\right] = C_f\left(\frac{C_1}{C_2} - 1\right) \quad (7)$$

If $C_1 >> C_2$, Eq.(7) may be rewritten as follows:

$$C_n \approx C_f\left(\frac{C_1}{C_2}\right) \quad (8)$$

The other common method of neutralization is the transformer-coupled method shown in Fig.12. Again, the condition for neutralization is that $i_f = i_n$. The requirements for this condition are expressed by the following equation:

$$\frac{v_d}{X_f} = \frac{-v_n}{X_n}, \text{ or } C_f v_d = -C_n v_n \quad (9)$$

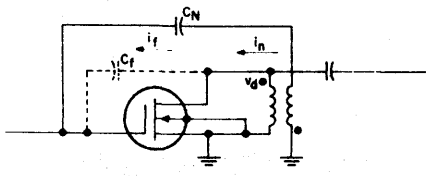


Fig.12 - Transformer-coupled neutralization circuit.

Eq.(9) may be rewritten in the following form:

$$\left|\frac{v_d}{v_n}\right| = \frac{C_n}{C_f} \quad (10)$$

The required turns ratio for the coupling transformer can be determined from Eq.(10).

The generator and load impedances must be matched to the transistor input and output impedances, respectively, to obtain maximum gain. For the 200-MHz amplifier shown in Fig.3, the generator resistance at the input is 50 ohms. For a conjugately matched input, the generator admittance y_g and the real part of the transistor input admittance must appear to be equal. Because the generator admittance y_g is 20 mmhos and the real part of the input admittance $Re(y_{11})$ is 0.45 mmho, the coupling transformer must provide a transformation ratio of 44 to obtain the desired impedance match. The turns ratio required is determined as follows:

$$\frac{N_2}{N_1} = \sqrt{44} = 6.6$$

Experimentally, a turns ratio of 4 was found to be approximately the optimum value. This difference results, in part, from the fact that the parallel resistance of the tank coil was not considered in the calculation. At the output of the 200-MHz amplifier, the load is also 50 ohms. Because the dc drain voltage must be blocked from the load, a series matching capacitor was selected which performs both dc blocking and resistive matching simultaneously.

In the actual load-circuit network shown in Fig.13(a), the value of capacitor C_S must be chosen so that the load admittance, $y_L = 20$ millimhos, is apparently equal to the real part of the transistor output admittance, $Re(y_{22}) = 0.28$ millimhos. Fig.13(b) shows the equivalent circuit of the load-circuit network for this condition.

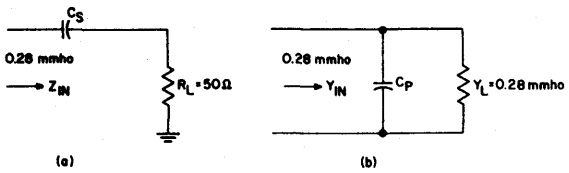


Fig.13 - Output network in which series coupling capacitance is used for dc-voltage blocking and resistive matching: (a) actual network; (b) electrical equivalent.

The following equation gives the input impedance Z_{IN} for the network shown in Fig.13:

$$Z_{IN} = R_S + \frac{1}{j\omega C_S} \quad (11)$$

The input admittance y_{IN}, therefore, may be expressed as follows:

$$y_{IN} = \frac{1}{R_p} + j\omega C_p = \frac{1}{Z_{IN}} = \frac{1}{R_S + \frac{1}{j\omega C_S}} \quad (12)$$

The terms in Eq.(12) are rearranged to obtain the following result:

$$\frac{R_S}{R_p} + j\omega C_p R_S + \frac{1}{j\omega C_S R_p} + \frac{j\omega C_p}{j\omega C_S} = 1 \quad (13)$$

The real and imaginary terms in Eq.(13) are equated to obtain the following relationships:

$$\frac{R_S}{R_p} + \frac{C_p}{C_S} = 1 \qquad (14)$$

$$\omega C_p R_S - \frac{1}{\omega C_S R_p} = 0 \qquad (15)$$

$$C_p = \frac{1}{(\omega C_S R_p)(\omega R_S)} \qquad (16)$$

Eq.(16) is substituted into Eq.(14) to obtain the following equation for the matching capacitance C_S:

$$C_S = \frac{1}{\omega}\sqrt{\frac{1}{(R_p - R_S)R_S}} \qquad (17)$$

Substitution of numerical values for the parameters in Eq.(17) yields the following value for C_S:

$$C_S = \frac{1}{2\pi(2 \times 10^8)}\sqrt{\frac{1}{(3600-50)50}} = 1.9 \text{ pF}$$

Experimentally, a 3-picofarad capacitor was found to perform very satisfactorily in the amplifier. If $R_p >> R_S$, then $C_p \approx C_S$. Therefore, a 3-picofarad capacitance appears in parallel with the 1.4-picofarad capacitance of the MOS transistor. A small 1-to-9-picofarad variable air capacitor was selected for the tank tuning capacitor to compensate for variations among transistors. For a nominal value of 2 picofarads for the air capacitor, the total output capacitance is 6.4 picofarads. The inductance required to resonate with 6.4 picofarads at 200 MHz is 0.1 microhenry. When the total output capacitance is known, the required neutralization capacitor can be calculated. If C_1 is arbitrarily selected as 33 picofarads, the neutralization is determined from Eq.(8), as follows:

$$C_n \approx C_f\left(\frac{C_1}{C_2}\right) = 0.2\left(\frac{33}{6.4}\right) = 1.0 \text{ pF}$$

The optimum value for the neutralization capacitor was determined experimentally by use of a small (0.5-to-3-picofarad) variable capacitor. This capacitor was adjusted to the optimum value for a typical unit (C_{rss} = 0.13 pF) and then fixed. The required input inductance was found to be 0.06 microhenry. The completed amplifier is shown schematically in Fig.3. The bandwidth of the amplifier is typically 8 MHz and shows negligible skew.

The y parameters may also be used to design a cascode vhf amplifier such as the one shown in Fig.5. This circuit had typical power gain and noise figure of 17 dB and 4.2 dB, respectively. The amplifier has a bandwidth of 10 MHz with negligible skew. The capacitance of the $source_2$-$drain_1$ interconnection must be tuned out to achieve a good vhf noise figure. The noise figure of the cascode amplifier is 2 to 3 dB higher if this capacitance is not tuned out.

References

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