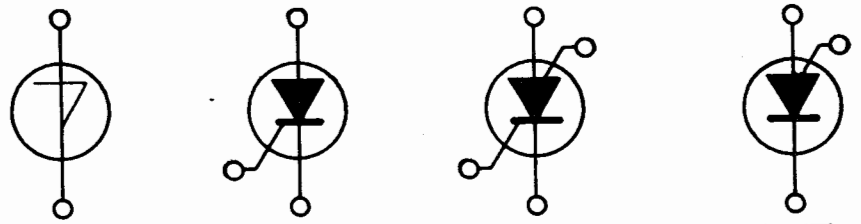
How To Putter With The Put



The PUT or complementary SCR is new solid-state device. Here is how it works and how to use it.

by R. W. FOX

About three years ago, the General Electric Company introduced the fourth member of the pnpn structure. This device has been called both a Programmable Unijunction Transistor (PUT), since it may be used in place of the unijunction transitor, and a complementary SCR. The former name is to show a major use of the device while the latter is a more descriptive name. General Electric has at present two devices on the market, the C13 Complementary SCR and the D13T PUT. These two devices are specified for their respective tasks, but to a degree may be interchanged. This article is devoted mainly to the D13T PUT. Several of the applications and much of the theory can apply equally to both devices. Included are theory, UJT replacement, switching circuits and many examples of their use.

Theory of the PUT

In Fig. 1, the equivalent circuit shows the two transistor analogue of a pnpn structure. For an SCR, the gate is the base of the npn transistor, but for the PUT the gate is the base of the pnp transistor. This is the difference between a PUT (and/or a complementary SCR) and an SCR. The theory follows normal thyristor theory for turn-on, turn-off and latching, etc.

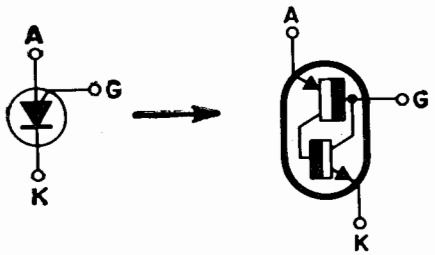


Fig. 1—PROGRAMMABLE UNIJUNCTION transistor and its equivalent circuit.

The device is turned on by making the gate negative with respect to the anode by a little more than the diode offset voltage so that enough anode current exists through the first pn junction (i.e., the anode-anode gate junction) to cause regeneration to occur. This current can be considered base current for the pnp transistor. The current required to trigger is typically on the order of a microampere. The current at which regeneration takes place is defined as the peak-point current (1_p). As the regeneration causes the anode-cathode voltage to collapse the device switches to the conducting state. The time for device turn-on is about 50 to 100 nanoseconds. (This turn-on, it should be noted, is an order of magnitude faster than the conventional unijunction transistor.) This results in a steep pulse for high di/dt SCR trigger applications. The device is now in the on-state, and in this region there are two parameters of great interest. These parameters (shown in Fig. 2) are I_V or valley current and I_H or

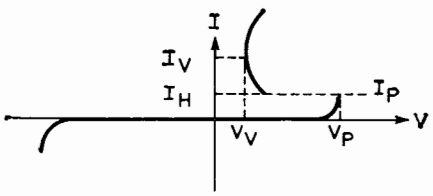


Fig. 2—ANODE-CATHODE CHARACTERISTICS based on the I_V and I_H parameters.

holding current. Valley current is the point at which the PUT starts out of saturation, however, because of the beta shifts in the two transistors, the device will remain in conduction until the holding current is reached. The device at this point returns to a non-conducting state.

The PUT in relaxation oscillators

Figure 3 shows a typical PUT relaxation oscillator. This circuit has two allowable states. State 1 will be for the PUT in the off or non-conducting state and state 2 will be for the PUT in the on-state.

First let's analyze the steady state conditions. Assume that the PUT is in state 1. After sufficient time the capacitor will be charged to $(V_{AA} - R_A I_{CL})$, where I_{CL} is capacitor leakage current. The anode-cathode voltage would be $(V_{AA} - R_A I_{CL} - R_L I_L)$, where I_L is the cathode leakage current

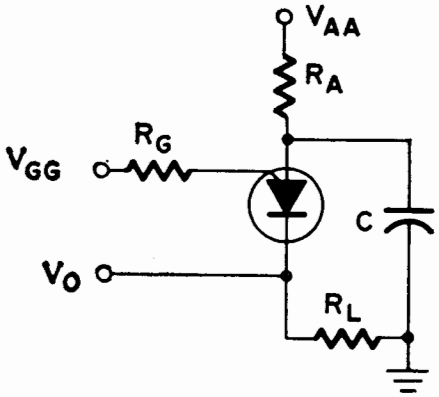


Fig. 3—A PUT RELAXATION OSCILLATOR. Like most circuits of this type, the active element is either on or off.

(which usually may be neglected). The voltage would be $(V_{GG} - R_G I_{GO})$, where I_{GO} would be the gate current with device off. (At room temperature I_{GO} will be less than 10 nanoamperes). If this state is allowed then:

$$V_{AA} - R_A (I_L + I_{CL}) < V_{GG} - R_G I_{GO} + V_T \quad \text{Eq. 1}$$

Where V_T is the gate offset voltage to trigger.

If this equation is satisfied then this state is a permissible state, and the output voltage (V_O) is $I_L R_L$. Assuming that I_L, I_{CL} and I_{GO} are negligible, Equation I reduces to:

$$V_{AA} \leq (V_{GG} + V_T) \quad \text{Eq. 2}$$

Equation 2 points out vividly that as long as the anode supply voltage is less than the effective gate source voltage ($V_{GE} \triangleq V_{GG} - V_T$) the PUT will remain non-conducting.

If the PUT is initially in state 2, then the following relationships will hold:

$$V_{GG} = (R_G + R_L) I_G + R_L I_{AR} \quad \text{Eq. 3}$$

$$V_{AA} = (R_A + R_L) I_G + R_L I_G \quad \text{Eq. 4}$$

$$V_O = R_L (I_G + I_{AK}) \quad \text{Eq. 5}$$

Where I_{AK} is anode-cathode current and V_F is the forward voltage drop.

If

$$I_{AK} > I_H \quad \text{Eq. 6}$$

then the PUT will remain in conduction.

If V_{GG} is applied to the circuit of Fig. 3 and then V_{AA} is applied, capacitor C will charge exponentially toward V_{AA}. If Equation 2 is satisfied then the PUT

does not turn-on. If, on the other hand $V_{AA} > (V_{GG} + V_T)$ then it may be possible for the PUT to turn on. As the capacitor charges the current through R_A decays exponentially. When $V_C = (V_{GG} + V_T)$ the current through R_A is:

$$I_A = (V_{AA} - V_C)/R_A \qquad \text{Eq. 7}$$

It is at this point the PUT will trigger, if at all. For the PUT to be triggered

$$I_A \geq I_P \qquad \text{Eq. 8}$$

For if I_A is less than I_P then regeneration cannot occur and the device remains in State 1.

If regeneration occurs then the anode-cathode voltage collapses and V_C appears across R_L. Voltage V_O will now follow V_C on an exponential decay less the forward drop of the PUT to one of two end points. The first is the case where equation 6 holds; the second where it does not. It can be seen, if the capacitor has been discharged, and Equation 6 still holds, then, as a consequence the PUT will remain conducting. In the other case, as the capacitor discharges, there will be a point in the discharge at which the anode current has dropped below the holding current. At this point the PUT returns to State 1 and the capacitor is recharged through R_A. This is the free-running relaxation oscillator.

PUT fudge factors

In the above discussion, I_P, I_V, V_T and V_{GG} were assumed. The parameters, though, are not just single numbers that are merely plugged into equations. Each of these may be varied over a considerable range.

Factor No. 1—**Stand-Off Ratio** (η)

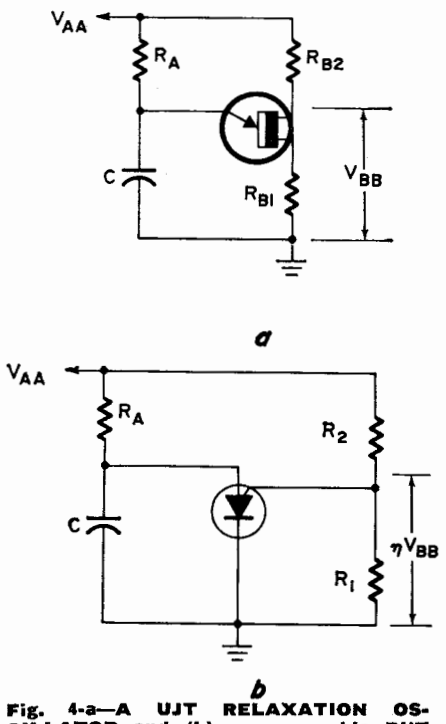


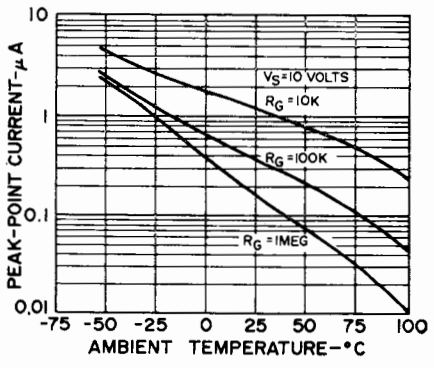
Fig. 4-a—A UJT RELAXATION OSCILLATOR and (b) a comparable PUT circuit.

In the above example two power supplies were used for the relaxation oscillator. In a conventional unijunction circuit (Fig. 4-a) only one supply is used and the peak capacitor voltage at turn-on is expressed as a function of the inter base voltage (V_{BB}). However, between UJT's of the same type this function, the stand-off ratio (η), varies by 10 to 20%. With the PUT each and every peak-point will be essentially the same and the designer may pick his peak-point over the range from 0.1 to 0.9. The stand-off ratio is merely the ratio of resistors in divider R1–R2 in Fig. 4-b. Thus, for the PUT, the stand-off ratio is:

$$\eta = R_1/(R_1 + R_2) \qquad \text{Eq. 9}$$

Factor No. 2—Peak Point Current (I_P)

Peak-point current is a function of gate source impedance and temperature, one is an advantage but one a disadvantage. As gate source impedance and temperature are raised the peak-point current decreases. Temperature compensation will be discussed in a later section. Figure 5-a and 5-b show



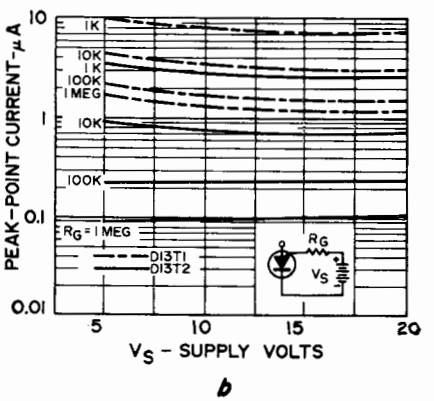
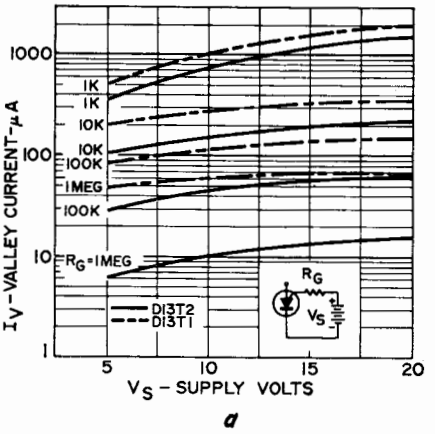


Fig. 5—PEAK-POINT CURRENT is a function of gate source impedance and of temperature. Chart (a) plots peak-point current against temperature and chart (b) against supply voltage (V_S) for different values of gate source impedance R_G.

the typical variations of peak-point current with changes in temperature and V_S (gate supply volts) for different values of gate series resistance (R_G).

Factor No. 3—Valley Current (I_V)

Valley current can be varied the same way the peak-point current is



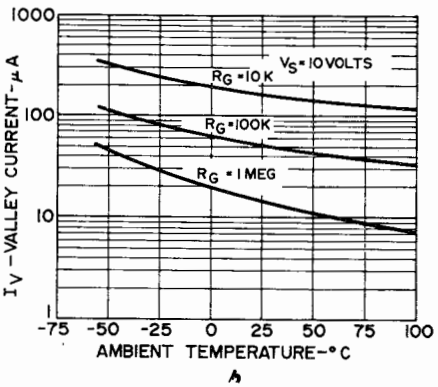


Fig. 6—VALLEY CURRENT characteristics, for given gate impedance, varies with V_G (chart a) and temperature (b).

varied. Figures 6-a and 6-b show this variation.

Factor No. 4—Offset Voltage (V_T)

Since the PUT, like most thyristors, is current triggered, the offset voltage is a function of gate source impedance. In reality this offset is due to the diode voltage drop between anode and gate, hence it is a function of temperature. Figure 7 shows the

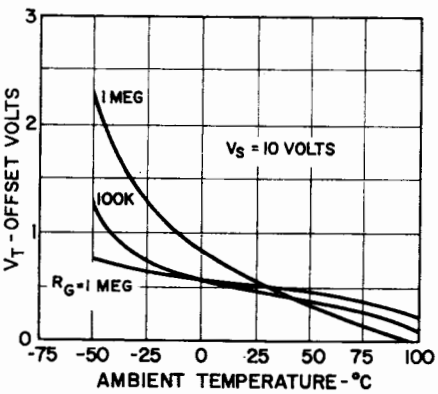


Fig. 7—TRIGGER OFFSET VOLTAGE for a programmable unijunction transistor varies with ambient temperature level and with the series impedance at the gate.

typical variation of V_T with gate source impedance and temperature.

Replacing UJT's with PUT's

In many cases a designer will wish to replace a UJT with a PUT to obtain a cost or performance advantage. Using the PUT (D13T) in a cir-

cuit in place of an unijunction is easily understood. Figure 8-a shows a basic unijunction circuit. Figure 9-a shows the identically same circuit except the unijunction transistor is replaced by the D13T plus the resistors R1 and R2. Comparing the equivalent circuits of Figs. 8-b and 9-b, it can be seen that both circuits have a diode connected to a voltage divider. When this diode is forward biased in the unijunction transistor, R1 becomes strongly modulated to a lower resistance value. This action generates a negative resistance characteristic between the emitter (E) and base one (B1). For D13T, resistors R1 and R2 control the voltage at which the anode-gate diode becomes forward biased. After the diode conducts, the regeneration inherent in a thyristor causes the PUT to switch on. This generates a negative resistance characteristic from anode to cathode simulating the modulation of R_1 in the conventional unijunction.

Resistors R_{B2} and R_{B1} (Figure 8-a) are generally unnecessary when the D13T replaces a conventional UJT. This is illustrated in Fig. 9-c. Resistor R_{B1} is often used to bypass the interbase current of the unijunction which would otherwise trigger the SCR. Since R1 in the case of the PUT (D13T), can be returned directly to ground there is only the peak-point current of the PUT (about 1μA) to bypass. Resistor R_{B2} is used for temperature compensation and for limiting the dissipation in the UJT during capacitor discharge. Since R2 (Fig. 9) is not modulated, R_{B2} can be absorbed into it. The result is the circuit of Fig. 9-b which contains the same number of components as the UJT circuit but at a lower cost and with better performance.

Resistors R1 and R2 have been removed from the pulse circuit, there is no reason why they cannot be changed in impedance to change the peak-point and valley currents as required by the application.

Applications of the PUT

The PUT with its flexibility can be tailored to fit many places where a UJT would not be acceptable: but before proceeding to some examples of this type of circuitry, there is a need to examine some final UJT applications of the PUT.

It was noted above and shown in Fig. 5 and 6 that peak and valley current were functions of gate source impedance. Since they both decrease with increase in gate source impedance there could be a problem if we wish to vary them independently. Figure 10 shows some variations on the gate circuitry.

In normal UJT circuitry the interbase resistance is normally about 10,000 ohms, with the PUT impedance level as a design factor. Figure 10-a shows a high-impedance divider which gives low I_P and low I_V. If you want characteristics closer to the UJT's, use the circuit in Fig. 10-b. Remembering that at the peak-point the anode (point E) of the PUT (D13T) is above the gate potential by V_T. Thus the diode is reversed biased and the gate source impedance is high (1-megohm in this case). But at the valley-point the gate is near cathode potential (point B1), so that the diode is forward biased and the gate source impedance is low (about 1000 ohms).

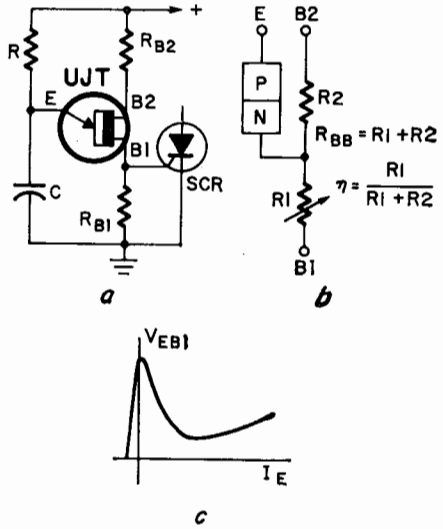


Fig. 8-a—A TYPICAL UNIJUNCTION driving an SCR. b—UJT equivalent circuit and (c) negative-resistance characteristic.

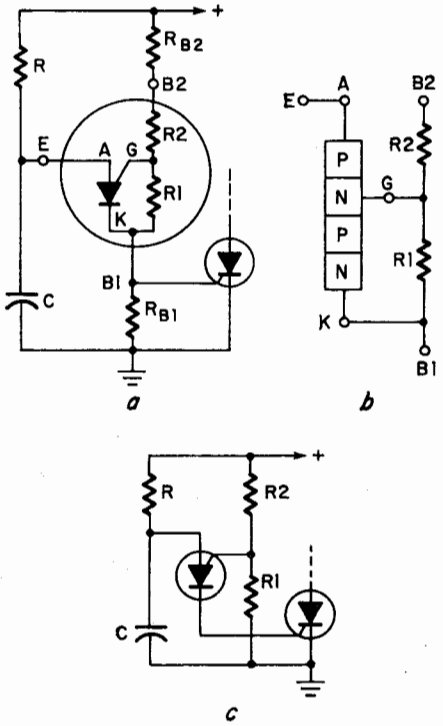


Fig. 9—HOW A PUT REPLACES UJT in circuit in Fig. 8-a. b—UJT equivalent circuit using programmable unijunction. c—The simplified PUT version of Fig. 8-a.

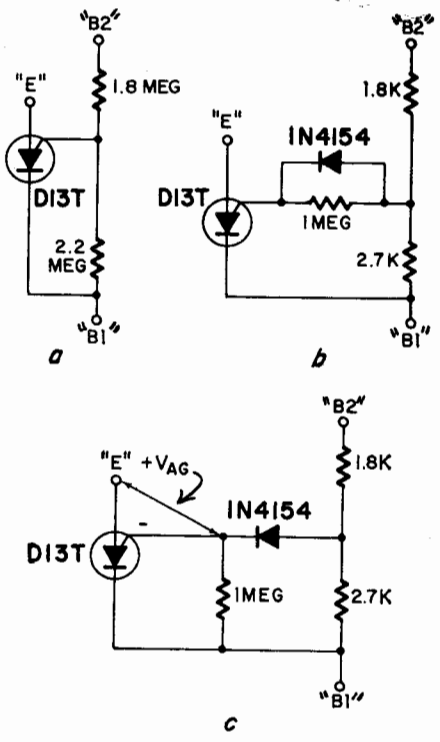


Fig. 10—TYPICAL UNIJUNCTION circuit configurations. a—For low I_P and low I_V. b—Use paralleled diode and resistor for low I_P-high I_V and (c) for low I_P and high I_V with temperature compensation.

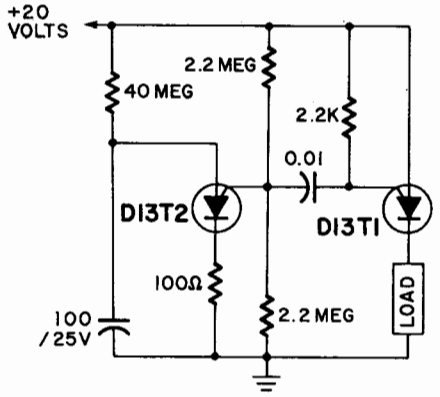


Fig. 11—A ONE HOUR TIMER using a pair of PUT's. The first does the timing; the second one triggers the load circuit.

This circuit has a low I_P and relatively high I_V.

Figure 10-c shows a similar diode network that provides temperature compensation of $V_T(V_{AG})$. When the peak-point is approached, the trigger point is when

$$(V_E - V_T) = (V_{GG} - V_D) \quad \text{Eq. 10}$$

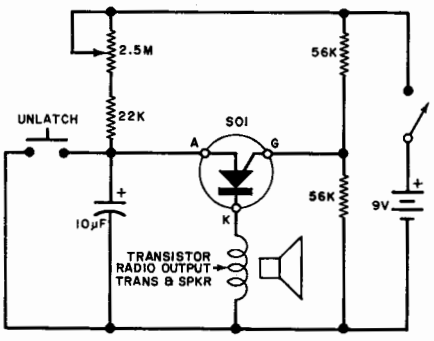
where V_{GG} is the effective gate source voltage; V_E is the emitter of the equivalent UJT and V_D is the diode forward drop. Equation 10 shows that temperature compensation is obtained when the diode's temperature coefficient is the same as V_T.

In Fig. 11 there is shown a one-hour timer using a single D13T2 PUT for timing and to develop a trigger pulse for the D13T1 at the end of the delay.

(continued next month)

IF you have some programmable unijunction transistors (PUT's) whose condition you are not quite sure of, you will want to build this simple test circuit. It will quickly sort good PUT's from bad ones. With a PUT plugged into the socket and the power turned on, the potentiometer is slowly adjusted from maximum to minimum. If the PUT is good, the speaker will emit a series of clicks or pops over some portion of the potentiometer's range.

You can also sort PUT's into grades and determine the correct anode re-



The PUT will oscillate at certain input currents.

sistor for reliable operation. To do this, use a dial plate and indicator knob to record the resistance of the potentiometer. With the PUT oscillating, a high resistance setting indicates the lowest allowable value of input current, while the lowest resistance setting indicates the maximum input current. To use that particular PUT in a circuit, the anode resistor must be within the indicated resistance range. If the resistance is too high, the PUT will not turn on; with too low a resistance the input will cause the PUT to latch in. To unlatch the circuit, the power must be removed or the capacitor must be discharged (using the switch shown).

PUT's that operate with a wide range of permissible input current can be used in variable oscillators, while those with a narrow range can be used in less demanding circuits where the anode resistor can be tailored for the application. ◈

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THEORY, CHARACTERISTICS AND APPLICATIONS OF THE PROGRAMMABLE UNIJUNCTION TRANSISTOR

This note discusses the characteristics of a programmable unijunction transistor (PUT) and offers comparisons with the annular unijunction. Also included are several circuits showing the versatility of the PUT.

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THEORY, CHARACTERISTICS AND APPLICATIONS OF THE PROGRAMMABLE UNIJUNCTION TRANSISTOR

INTRODUCTION

The programmable unijunction transistor (PUT) is a four layer device similar to an SCR except that the anode gate rather than the cathode gate is brought out. It is normally used in conventional unijunction transistor (UJT) circuits. The characteristics of both devices are similar, but the triggering voltage of the PUT is programmable and can be set by an external resistive voltage divider network. The PUT is faster and more sensitive than the UJT. It finds limited application as a phase control element and is most often used in long duration timer circuits. In general, the PUT is more versatile and is a more economical device than the UJT and will replace it in many applications.

OPERATION OF THE PUT

The PUT has three terminals, an anode (A), gate (G), and cathode (K). The symbol and a transistor equivalent circuit are shown in Figure 1. As can be seen from the equivalent circuit, the device is actually an anode-gated SCR. This means that if the gate is made negative with respect to the anode, the device will switch from a blocking state to its on state.

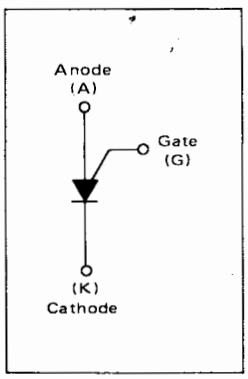

FIGURE 1a – PUT Symbol

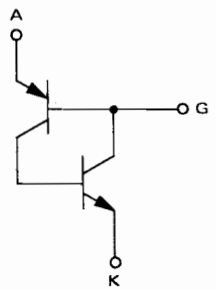

FIGURE 1b – Transistor Equivalent

Since the PUT is normally used as a unijunction transistor (UJT), the UJT terminology is used to describe its parameters. In order to operate this device as a UJT, an external reference voltage must be maintained at the gate terminal. A typical relaxation type oscillator circuit is shown in Figure 2a. The voltage divider shown is a typical way of obtaining the gate reference. In this circuit,

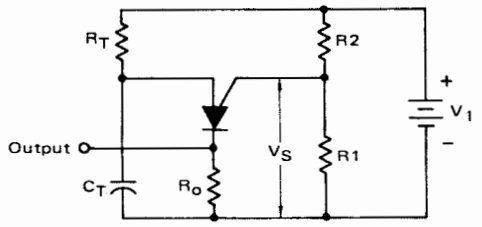

FIGURE 2a – Typical Oscillator Circuit

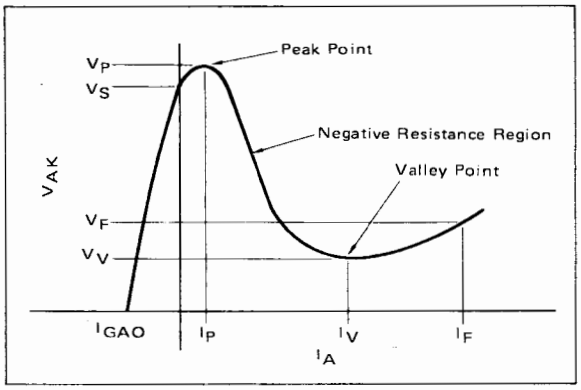

FIGURE 2b – Static Characteristics

the characteristic curve looking into the anode-cathode terminals would appear as shown in Figure 2b. The peak and valley points are stable operating points at either end of a negative resistance region. The peak point voltage (V_P) is essentially the same as the external gate reference, the only difference being the gate diode drop. Since the reference is circuit and not device dependent, it may be varied, and in this way, V_P is programmable. This feature is the most significant difference between the UJT and the PUT.

In characterizing the PUT, it is convenient to speak of the Thevenin equivalent circuit for the external gate voltage (V_S) and the equivalent gate resistance (R_G). The parameters are defined in terms of the divider resistors (R1 and R2) and supply voltage as follows:

$$V_S = R1\ V1/(R1 + R2)$$

$$R_G = R1\ R2/(R1 + R2)$$

TABLE I – Typical PUT Characteristics

Symbol	Test Circuit Figure	Test Conditions	MPU 131	MPU 132	MPU 133	Unit
I_P	3	R_G = 1 MΩ R_G = 10 kΩ	1.25 4.0	0.19 1.20	0.08 0.70	μA μA
I_V	3	R_G = 1 MΩ R_G = 10 kΩ	18.0 270	18.0 270	18.0 270	μA μA
V_{AG}		(See Figure 4)				
I_{GAO}		V_S = 40 V	See Figure 5			
I_{GKS}		V_S = 40 V	5.0	5.0	5.0	nA
V_F	Curve Tracer Used	I_F = 50 mA	0.8	0.8	0.8	V
V_O	6		16	16	16	V
t_r	7		40	40	40	ns

Most device parameters are sensitive to changes in V_S and R_G. For example, decreasing R_G will cause peak and valley currents to increase. This is easy to see since R_G actually shunts the device and will cause its sensitivity to decrease.

CHARACTERISTICS OF THE PUT

Table I is a list of typical characteristics of Motorola's MPU131 (plastic) and 231 (hermetic series) of programmable unijunction transistors. The test circuits and test conditions shown are essentially the same as for the data sheet characteristics. The data presented here defines the static curve shown in Figure 2b for a 10 V gate reference (V_S) with various gate resistances (R_G). It also indicates the leakage currents of these devices and describes the output pulse. Values given are for 25°C unless otherwise noted. The following paragraphs define these parameters and indicate how they are measured and used.

PEAK POINT CURRENT, (I_P)

The peak point is indicated graphically by the static curve in Figure 2b. Reverse anode current flows with anode voltages less than the gate voltage (V_S) because of leakage from the bias network to the charging network. With currents less than I_P, the device is in a blocking state. With currents above I_P, the device goes through a negative resistance region to its "on" state.

The charging current, or the current through a timing resistor, must be greater than I_P at V_P to insure that a device will switch from a "blocking" to an "on" state in an oscillator circuit. For this reason, maximum values of I_P are given on the data sheet. These values are dependent on V_S, temperature, and R_G. Typical curves on the data sheet indicate this dependence and must be consulted for most applications.

The test circuit in Figure 3 is a sawtooth oscillator which uses a 0.01 μF timing capacitor, a 20 V supply, an adjustable charging current, and equal biasing resistors (R). The two biasing resistors were chosen to give an equivalent R_G of 1 MΩ and 10 kΩ. The peak point current was measured with the device "off" just prior to oscillation as detected by the absence of an output voltage pulse. The 2N5270 field effect transistor circuit is used as a current source. A variable gate voltage supply was used to control this current.

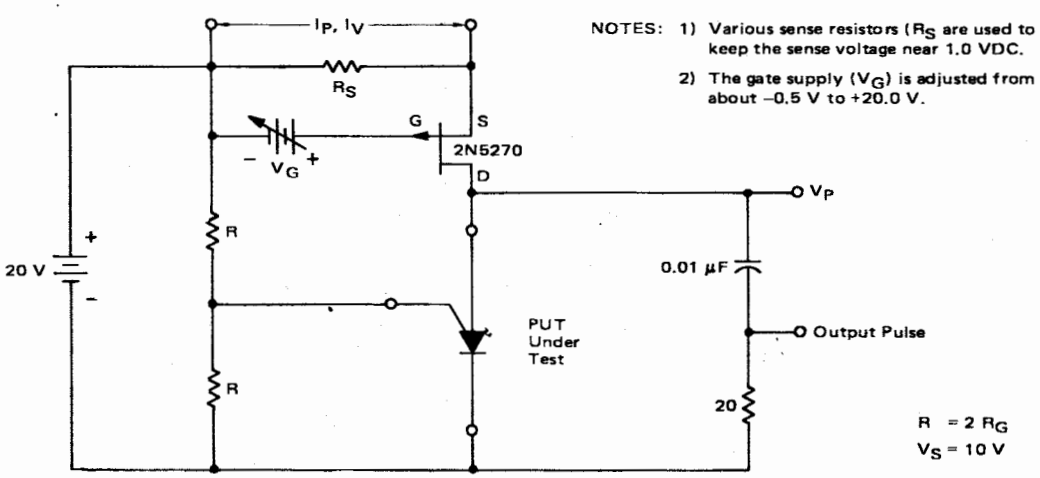

FIGURE 3 – Test Circuit for I_P, V_P and I_V

VALLEY POINT CURRENT, (I_V)

The valley point is indicated graphically in Figure 2b. With currents slightly less than I_V, the device is in an unstable negative resistance state. A voltage minimum occurs at I_V, and with higher currents, the device is in a stable "on" state.

When the device is used as an oscillator, the charging current or the current through a timing resistor must be less than I_V at the valley point voltage (V_V). For this reason, minimum values for I_V are given on the data sheet for R_G = 10 kΩ. With R_G = 1 MΩ, a reasonable "low" is 2 μA for all devices.

When the device is used as an SCR in the latching mode, the anode current must be greater than I_V. Maximum values for I_V are given with R_G = 1 MΩ. All devices have a reasonable "high" of 400 μA I_V with R_G = 10 kΩ.

LATCHING AND HOLDING CURRENT, (I_L, I_H)

Using the test circuit in Figure 3, an attempt was made to differentiate between latching current (I_L), holding current (I_H), and valley current. With the device latched on, reducing the current causes a voltage minimum which is the valley point. The device does remain on at lower currents until holding current (I_H) is reached. The holding current is measured as detected by the absence of an output voltage pulse just before oscillation occurs. The latching current is generally higher than I_H and is measured by increasing the current while the device is oscillating and recording the value at which oscillations stop. With the PUT, there was no measurable difference between these parameters. This is not necessarily true with a unijunction transistor.

The valley current does vary with circuit parameters and temperature as was true of I_P. Typical data sheet curves identify this dependence and are frequently used to approximate actual variations of I_V.

PEAK POINT VOLTAGE, (V_P)

The unique feature of the PUT is that the peak point voltage can be determined externally. This programmable feature gives this device the ability to function in voltage controlled oscillators or similar applications. The triggering or peak point voltage is approximated by

$$V_P \approx V_T + V_S,$$

where V_S is the unloaded divider voltage and V_T is the offset voltage. The actual offset voltage will always be higher than the anode-gate voltage V_{AG}, because I_P flows out of the gate just prior to triggering. This makes $V_T = V_{AG} + I_P R_G$. A change in R_G will affect both V_{AG} and $I_P R_G$ but in opposite ways. First, as R_G increases, I_P decreases and causes V_{AG} to decrease. Second, since I_P does not decrease as fast as R_G increases, the $I_P R_G$ product will increase and the actual V_T will increase. These second order effects are difficult to predict and measure. Allowing V_T to be 0.5 V as a first order approximation gives sufficiently accurate results for most applications.

The peak point voltage was tested using the circuit in Figure 3 and a scope with 10 MΩ input impedance across the PUT. A Tektronix, Type W plug-in was used to determine this parameter.

FORWARD ANODE-GATE VOLTAGE, (V_{AG})

The forward anode-to-gate voltage drop affects the peak point voltage as was previously discussed. The drop is essentially the same as a small signal silicon diode and is plotted in Figure 4. The voltage decreases as current decreases, and the change in voltage with temperature is greater at low currents. At 10 nA the temperature coefficient is about −2.4 V/°C and it drops to about −1.6 mV/°C at 10 mA. This information is useful in applications where it is desirable to temperature compensate the effect of this diode.

GATE-CATHODE LEAKAGE CURRENT, (I_{GKS})

The gate-to-cathode leakage current is the current that flows from the gate to the cathode with the anode shorted to the cathode. It is actually the sum of the open circuit gate-anode and gate-cathode leakage currents. The shorted leakage represents current that is shunted away from the voltage divider.

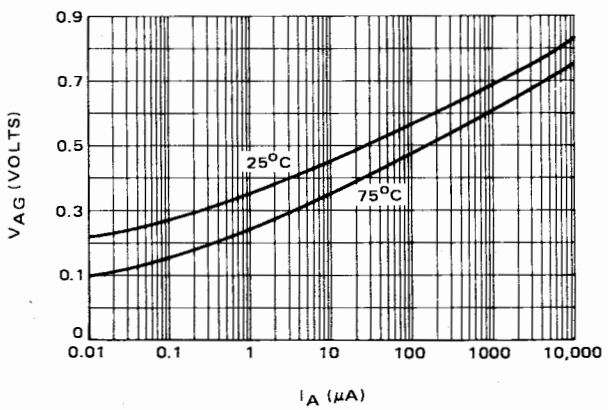

FIGURE 4 – Gate Voltage Drop of MPU131, and 231 Series

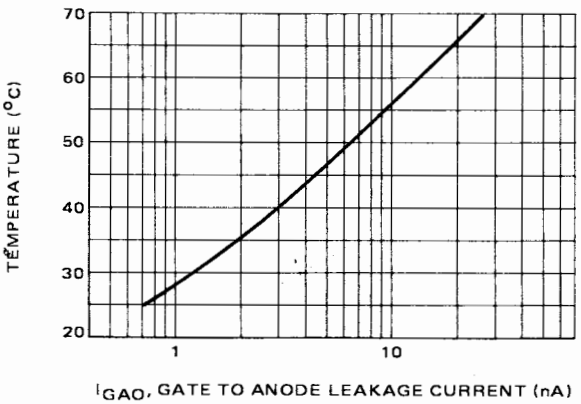

FIGURE 5 – Typical Leakage Current of the MPU131, 132 and 133 Reverse Voltage Equals 40 V

GATE-ANODE LEAKAGE CURRENT, (I_{GAO})

The gate-to-anode leakage current is the current that flows from the gate to the anode with the cathode open. It is important in long duration timers since it adds to the charging current flowing into the timing capacitor. The typical leakage currents measured at 40 V are shown in Figure 5. Leakage at 25°C is approximately 1 nA and the current appears to double for about every 10°C rise in temperature.

FORWARD VOLTAGE, (V_F)

The forward voltage (V_F) is the voltage drop between the anode and cathode when the device is biased on. It is the sum of an offset voltage and the drop across some internal dynamic impedance which both tend to reduce the output pulse. The typical data sheet curve shows this impedance to be less than 1 ohm for up to 2 A of forward current. This is essentially an order of magnitude better than the UJT which is closer to 20 ohms.

PEAK OUTPUT VOLTAGE, (V_o)

The peak output voltage is not only a function of V_P, V_F and dynamic impedance, but is also affected by switching speed. This is particularly true when small capacitors (less than 0.01 μF) are used for timing since they lose part of their charge during the turn on interval. The use of a relatively large capacitor (0.2 μF) in the test circuit of Figure 6 tends to minimize this last effect. The output voltage is measured by placing a scope across the 20 ohm resistor which is in series with the cathode lead.

RISE TIME, (t_r)

Rise time is a useful parameter in pulse circuits that use capacitive coupling. It can be used to predict the amount of current that will flow between these circuits. Rise time is specified using a real time scope and measuring between 0.6 V and 6.0 V on the leading edge of the output pulse. Even fast scopes (100 MHz bandpass) degrade this measurement and readings must be corrected by calculations. It is preferable to use a 1000 pF capacitor and a sampling scope as shown in Figure 7 to read the 10% to 90% points directly. The resulting typical rise times of 40 ns are significantly better than those of the UJT which are about 100 ns.

MINIMUM AND MAXIMUM FREQUENCY

In actual tests with devices whose parameters are known, it is possible to establish minimum and maximum values of timing resistors that will guarantee oscillation. The circuit under discussion is a conventional RC relaxation type oscillator.

To obtain maximum frequency, it is desirable to use low values of capacitance (1000 pF) and to select devices and bias conditions to obtain high I_V. It is possible to use stray capacitance but the results are generally unpredictable. The minimum value of timing resistance is obtained using the following rule of thumb:

$$R_{(MIN)} = 2(V_1 - V_V)/I_V$$

where the valley voltage (V_V) is often negligible.

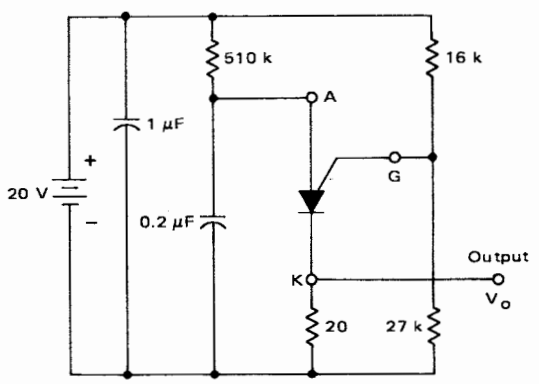

FIGURE 6 – PUT Test Circuit for Output Voltage (V_o)

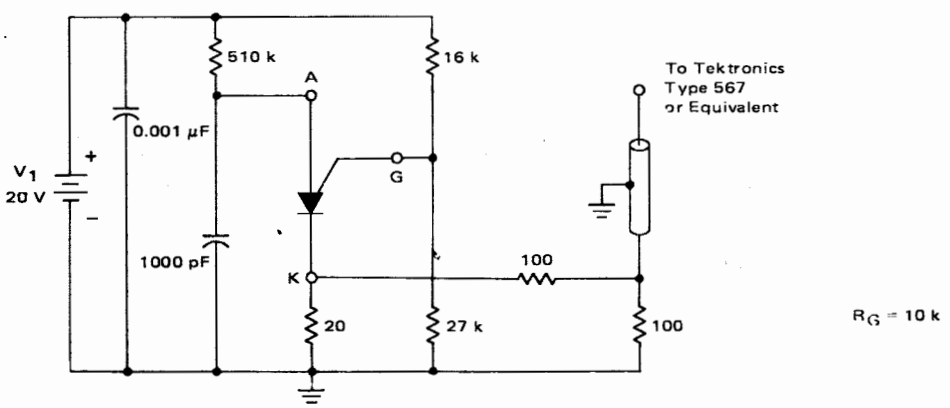

FIGURE 7 – t_r Test Circuit for PUTS

To obtain minimum frequency, it is desirable to use high values of capacitance (10 μF) and to select devices and bias conditions to obtain low I_P. It is important that the capacitor leakage be quite low. Glass and mylar dielectrics are often used for these applications. The maximum timing resistor is as follows:

$$R_{(MAX)} = (V_I - V_P)/2I_P$$

In a circuit with a fixed value of timing capacitance, our most sensitive PUT, the MPU133/233, offer the largest dynamic frequency range. Allowing for capacitance and bias changes, the approximate frequency range of a PUT is from 0.003 Hz to 2.5 kHz.

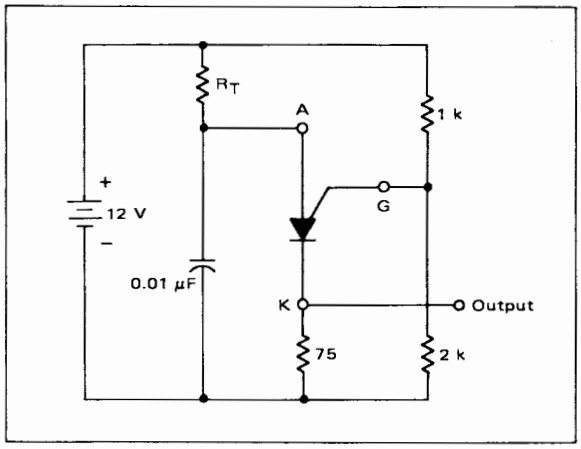

FIGURE 8 – Uncompensated Oscillator

TEMPERATURE COMPENSATION

The PUT with its external bias network exhibits a relatively small frequency change with temperature. The uncompensated RC oscillator shown in Figure 8 was tested at various frequencies by changing the timing resistor R_T. At discrete frequencies of 100, 200, 1000 and 2000 hertz, the ambient temperature was increased from 25° to 60°C. At these low frequencies, the negative temperature coefficient of V_{AG} predominated and caused a consistant 2% increase in frequency. At 10 kHz, the frequency remained within 1% over the same temperature range. The storage time phenomenon which increases the length of the output pulse as temperature increases is responsible for this result. Since this parameter has not been characterized, it is obvious that temperature compensation is

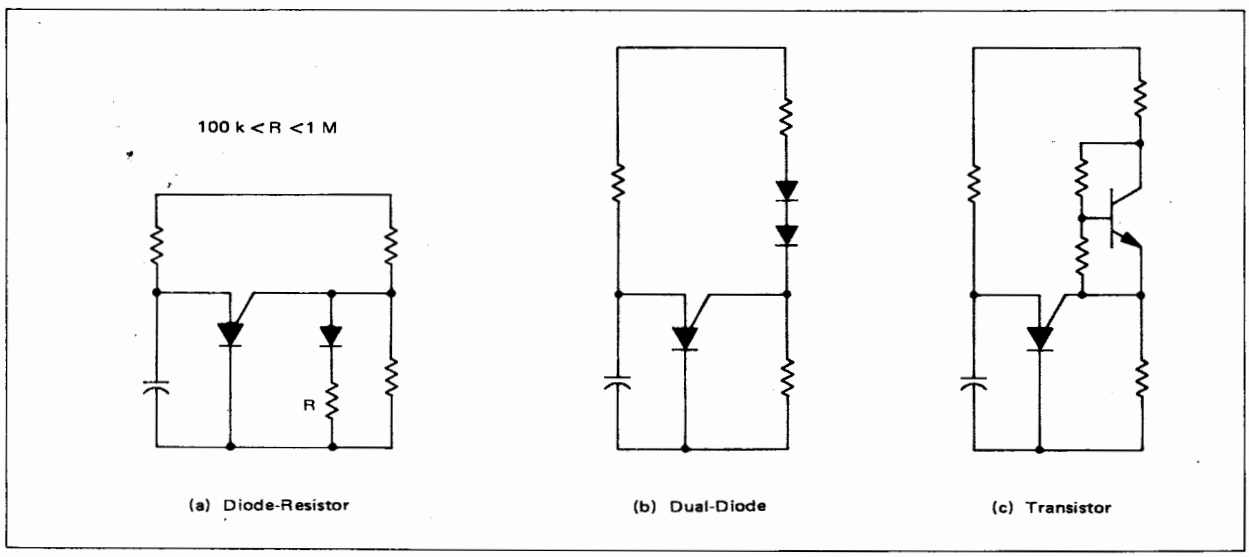

FIGURE 9 – Temperature Compensation Techniques

TABLE II – Typical UJT Characteristics

Symbol	Test Circuit Figure	Test Conditions	2N4870	2N4871	Unit
I_P	11		1.0	1.0	μA
I_V	11		5.0	7.0	μA
V_P	12	V_1 = 10 V	6.6	8.0	V
I_{EB20}		V = 30 V	See Figure 10		
$V_{EB1(sat)}$	Curve Tracer Used	I_E = 50 mA V_1 = 20 V	2.5	2.5	V
V_{OB1}	12	V_1 = 20 V	6.0	8.0	V
t_r	13		110	110	ns
R_{BB}	Curve Tracer Used	V = 3 V	6.0	6.0	kΩ

more practical with relatively low frequency oscillators.

Various methods of compensation are shown in Figure 9. In the low cost diode-resistor combination of 9a, the diode current is kept small to cause its temperature coefficient to increase. In 9b, the bias current through the two diodes must be large enough so that their total coefficient compensates for V_{AG}. The transistor approach in 9c can be the most accurate since its temperature coefficient can be varied independently of bias current.

CHARACTERISTICS OF THE UJT

Typical UJT characteristics are shown in Table II and in Figure 10 for comparison purposes. The test circuits are shown in Figures 11 through 13, and the measured parameters are essentially a duplication of the PUT parameters shown in Table I. AN-293 reviews the basic theory of UJT devices. The UJT is not as sensitive as the PUT and is a slower device. Its forward drop is higher and the intrinsic standoff ratio is not programmable. One distinct advantage is that the range of frequencies of the UJT is consistently better than two orders of magnitude (100 times) whereas the PUT is not quite that good. This difference is primarily due to I_V.

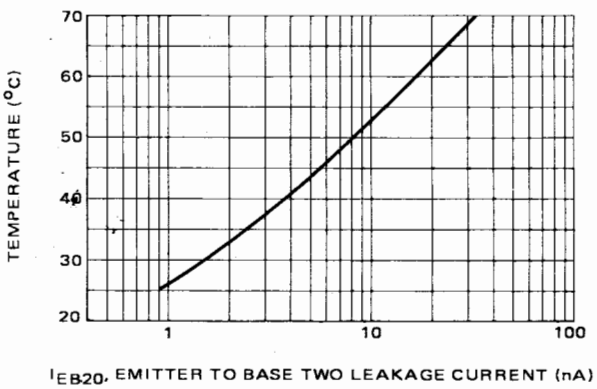

FIGURE 10 – Typical Leakage Current of the 2N4870 and 71 Reverse Voltage Equals 30 V

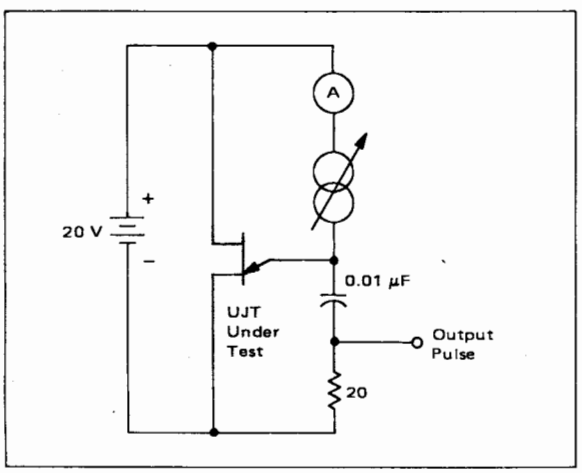

FIGURE 11 – UJT Test Circuit for I_P, I_V, I_L

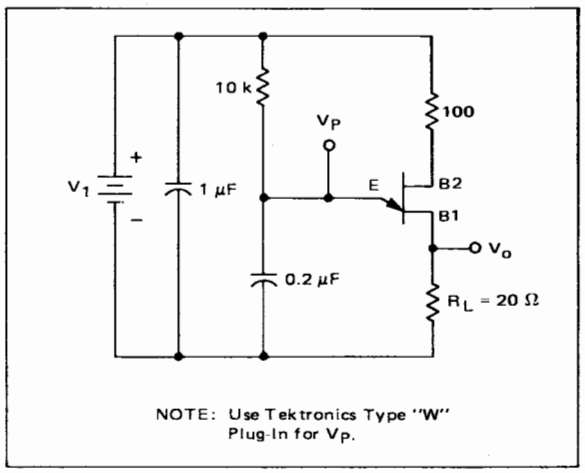

FIGURE 12 – UJT Test Circuit for V_O, V_P

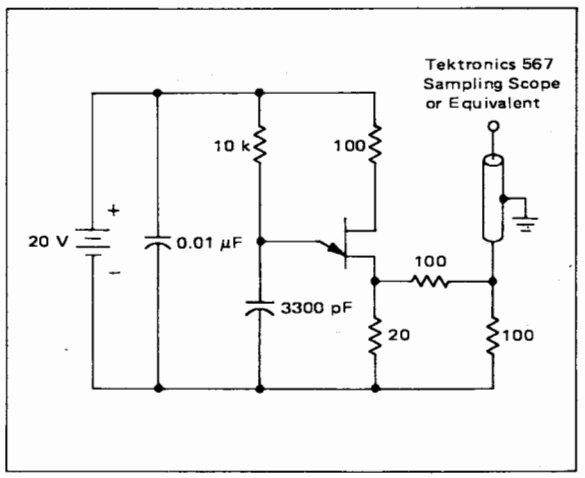

FIGURE 13 – UJT Rise Time Test Circuit

TYPICAL CIRCUITS

The following circuits show a few of the many ways in which the PUT can be used. The circuits are not optimized even though performance data is shown.

In several of the circuit examples, the versatility of the PUT has been hidden in the design. By this it is meant that in designing the circuit, the circuit designer was able to select a particular intrinsic standoff ratio or he could select a particular R_G (gate resistance) that would provide a maximum or minimum valley and peak current. This makes the PUT very versatile and very easy to design with.

LOW VOLTAGE LAMP FLASHER

One advantage of the PUT over a conventional unijunction transistor is that the PUT operates very well for low supply voltages. This is due to the low forward voltage drop of the PUT, 1.5 volts maximum for the MPU131-33, compared to the emitter saturation voltage of the UJT of 3.0 volts maximum for the 2N5431.

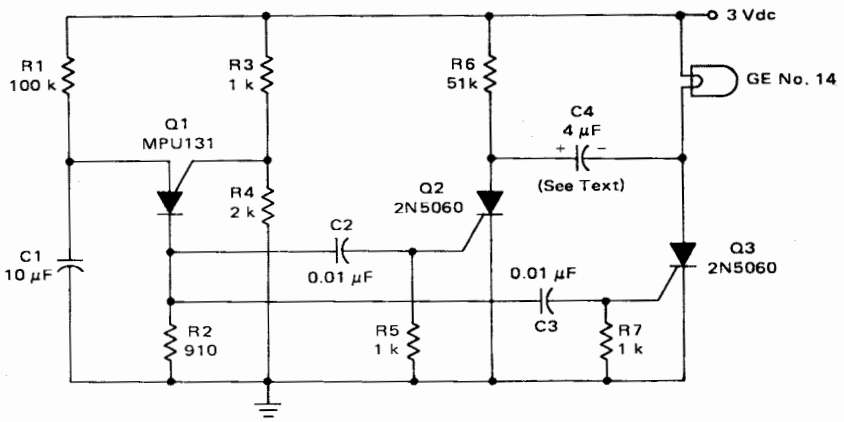

FIGURE 14 – Low Voltage Lamp Flasher

A circuit using the PUT in a low voltage application is shown in Figure 14 where a supply voltage of 3 volts is used. The circuit is a low voltage lamp flasher composed of a relaxation oscillator formed by Q1 and an SCR flip flop formed by Q2 and Q3.

With the supply voltage applied to the circuit, the timing capacitor C1 charges to the firing point of the PUT, 2 volts plus a diode drop. The output of the PUT is coupled through two 0.01 μF capacitors to the gate of Q2 and Q3. To clarify operation, assume that Q3 is "on" and capacitor C4 is charged plus to minus as shown in the figure. The next pulse from the PUT oscillator turns Q2 "on". This places the voltage on C4 across Q3 which momentarily reverse biases Q3. This reverse voltage turns Q3 "off". After discharging, C4 then charges with its polarity reversed to that shown. The next pulse from Q1 turns Q3 "on" and Q2 "off". Note that C4 is a non polarized capacitor.

For the component values shown, the lamp is on for about 1/2 second and off the same amount of time.

VOLTAGE CONTROLLED RAMP GENERATOR

The PUT provides a simple approach to a voltage controlled ramp generator, VCRG, as shown in Figure 15. The current source formed by Q1 in conjunction with capacitor C1 set the duration time of the ramp. As the positive dc voltage at the gate is changed, the peak point firing voltage of the PUT is changed which changes the duration time i.e., increasing the supply voltage increases the peak point firing voltage causing the duration time to increase.

Figure 16 shows a plot of voltage-versus-ramp duration time for a 0.0047 μF and a 0.01 μF timing capacitor. The figure indicates that it is possible to have a change in frequency of 3.0 ms and 5.4 ms for the 0.0047 μF and the 0.01 μF capacitor respectively as the control voltage is varied from 5 to 20 volts.

LOW FREQUENCY DIVIDER

The circuit shown in Figure 17 is a frequency divider with the ratio of capacitors C1 and C2 determining divi-

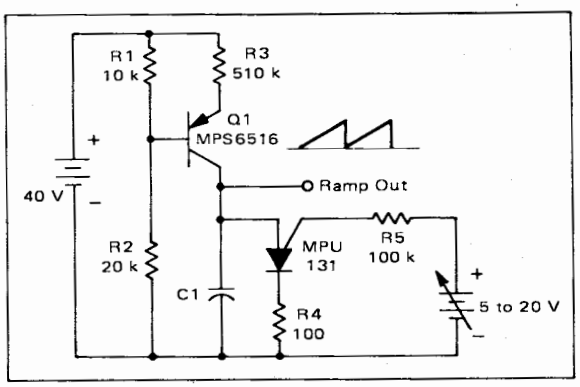

FIGURE 15 – Voltage Controlled Ramp Generator (VCRG)

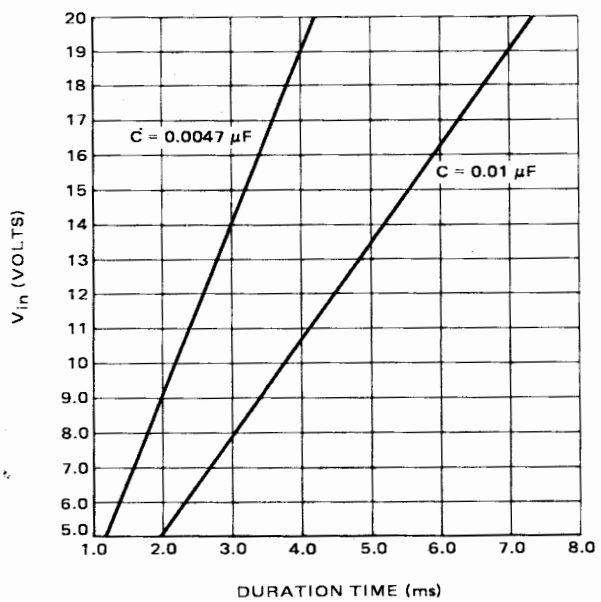

FIGURE 16 – Voltage versus Ramp Duration Time of VCRG

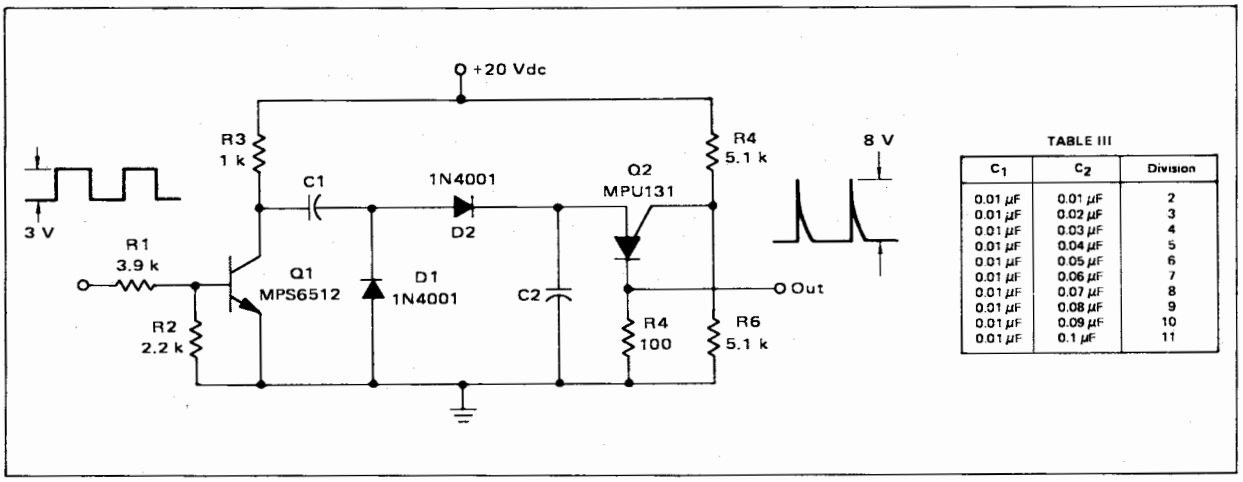

TABLE III

C_1	C_2	Division
0.01 µF	0.01 µF	2
0.01 µF	0.02 µF	3
0.01 µF	0.03 µF	4
0.01 µF	0.04 µF	5
0.01 µF	0.05 µF	6
0.01 µF	0.06 µF	7
0.01 µF	0.07 µF	8
0.01 µF	0.08 µF	9
0.01 µF	0.09 µF	10
0.01 µF	0.1 µF	11

FIGURE 17 – Low Frequency Divider

sion. With a positive pulse applied to the base of Q1, assume that C1 = C2 and that C1 and C2 are discharged. When Q1 turns "off", both C1 and C2 charge to 10 volts each through R3. On the next pulse to the base of Q1, C1 is again discharged but C2 remains charged to 10 volts. As Q1 turns off this time, C1 and C2 again charge. This time C2 charges to the peak point firing voltage of the PUT causing it to fire. This discharges capacitor C2 and allows capacitor C1 to charge to the line voltage. As soon as C2 discharges and C1 charges, the PUT turns off. The next cycle begins with another positive pulse on the base of Q1 which again discharges C1.

The input and output frequency can be approximated by the equation

$$f_{in} \approx \frac{(C1 + C2)}{C1} f_{out}$$

For a 10 kHz input frequency with an amplitude of 3 volts, Table III shows the values for C1 and C2 needed to divide by 2 to 11.

This division range can be changed by utilizing the programmable aspect of the PUT and changing the voltage on the gate by changing the ratio R6/(R6+R5). Decreasing the ratio with a given C1 and C2 decreases the division range and increasing the ratio increases the division range.

The circuit works very well and is fairly insensitive to the amplitude, pulse width, rise and fall times of the incoming pulses.

LONG DURATION TIMER

A long duration timer circuit that can provide a time delay of up to 20 minutes is shown in Figure 18. The circuit is a standard relaxation oscillator with a FET current source in which resistor R1 is used to provide reverse bias on the gate-to-source of the JFET. This turns the JFET off and increases the charging time of C1. C1 should be a low leakage capacitor such as a mylar type.

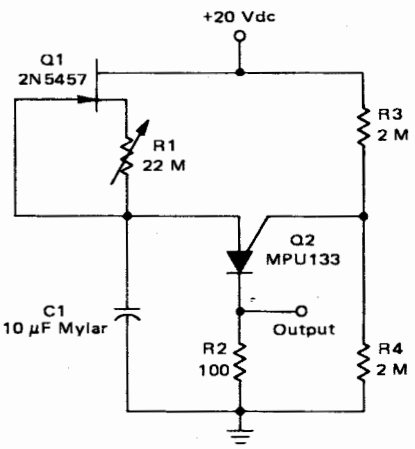

FIGURE 18 – 20-Minute, Long Duration Timer

The source resistor of the current source can be computed using the following equation*

$$V_{GS} = V_P(1 - \sqrt{I_O/I_{DSS}})$$

$$\therefore R1 = \frac{V_{GS}}{I_O}$$

where I_O is the current out of the current source.

V_P is the pinch off voltage,

V_{GS} is the voltage gate to source and,

I_{DSS} is the current, drain-to-source, with the gate shorted to the source.

The time needed to charge C1 to the peak point firing voltage of Q2 can be approximated by the following equation:

$$T = \frac{C\Delta V}{I},$$

*See AN-462

where T is time in seconds

C is capacitance in microfarads,

ΔV is the change in voltage across capacitor C1, and

I is the constant current used to charge C1.

Maximum time delay of the circuit is limited by the peak point firing current, I_P, needed to fire Q2. For charging currents below I_P, there is not enough current available from the current source to fire Q2, causing the circuit to lock up. Thus a PUT works better than a unijunction in a long duration timer because it has a lower peak point firing current. Also, because of the programmable aspect of the PUT, I_P can be made very small by making R_G (the equivalent parallel resistance of R3 and R4) large, (1 MΩ) as shown in Figure 18.

PHASE CONTROL

Figure 19 shows a circuit using a PUT for phase control of an SCR. The relaxation oscillator formed by Q2 provides conduction control of Q1 from 1 to 7.8 milliseconds or 21.6° to 168.5°. This constitutes control of over 97% of the power available to the load.

Only one SCR is needed to provide phase control of both the positive and negative portion of the sine wave by putting the SCR across the bridge composed of diodes D1 through D4.

BATTERY CHARGER

A short circuit proof battery charger is shown in Figure 20 which will provide an average charging current of about 8 amperes to a 12 volt lead acid storage battery.* The charger circuit has an additional advantage in that it will not function nor will it be damaged by improperly connecting the battery to the circuit.

*Motorola Power Circuits Handbook

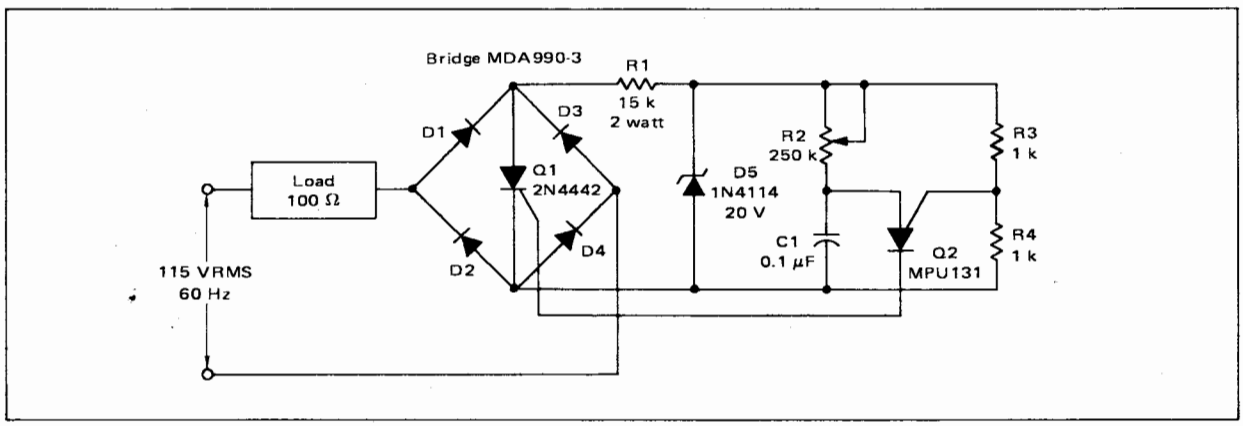

FIGURE 19 – SCR Phase Control

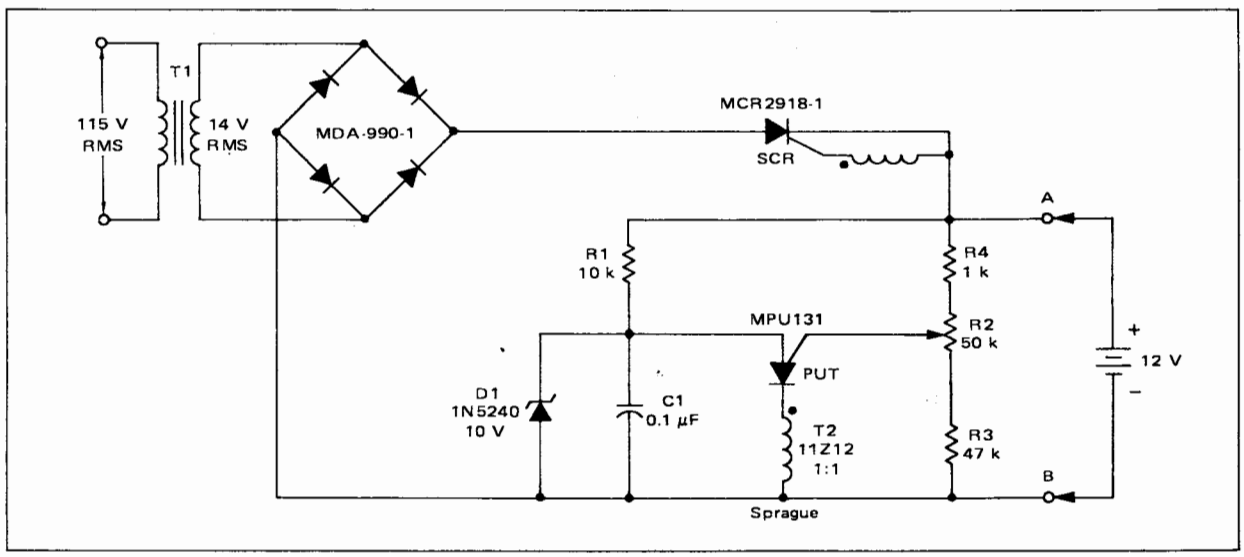

FIGURE 20 – 12 Volt Battery-Charger

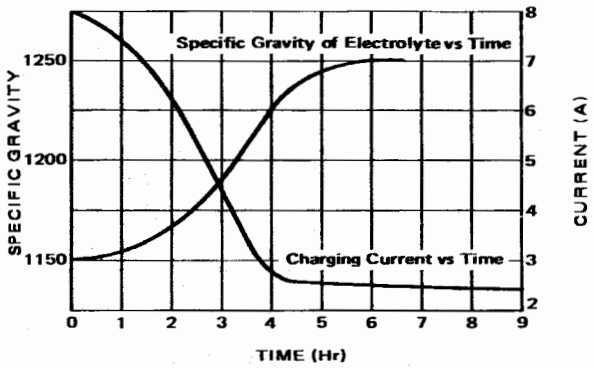

FIGURE 21 – Charging Characteristics of Battery Charger of Figure 20

With 115 volts at the input, the circuit commences to function when the battery is properly attached. The battery provides the current to charge the timing capacitor C1 used in the PUT relaxation oscillator. When C1 charges to the peak point voltage of the PUT, the PUT fires turning the SCR on which in turn applies charging current to the battery. As the battery charges, the battery voltage increases slightly which increases the peak point voltage of the PUT. This means that C1 has to charge to a slightly higher voltage to fire the PUT. The voltage on C1 increases until the zener voltage of D1 is reached which clamps the voltage on C1 and thus prevents the PUT oscillator from oscillating and charging ceases. The maximum battery voltage is set by potentiometer R2 which sets the peak point firing voltage of the PUT.

In the circuit shown, the charging voltage can be set from 10 V to 14 V, the lower limit being set by D1 and the upper limit by T1. Lower charging voltages can be obtained by reducing the reference voltage (reducing the value of zener diode D1) and limiting the charging current (using either a lower voltage transformer (T1) or adding resistance in series with the SCR.)

Resistor R4 is used to prevent the PUT from being destroyed if R2 were turned all the way up.

Figure 21 shows a plot of the charging characteristics of the battery charger in Figure 20.

RMS VOLTAGE REGULATOR

The circuit of Figure 22 is an open loop rms voltage regulator that will provide 500 watts of power at 90 V rms with good regulation for an input voltage range of 110-130 V rms.

With the input voltage applied, capacitor C1 charges until the firing point of Q3 is reached causing it to fire. This turns Q5 on which allows current to flow through the load. As the input voltage increases, the voltage across R10 increases which increases the firing point of Q3. This delays the firing of Q3 because C1 now has to charge to a higher voltage before the peak-point voltage is reached. Thus the output voltage is held fairly constant by delaying the firing of Q5 as the input voltage increases. For a decrease in the input voltage, the reverse occurs.

Another means of providing compensation for increased input voltage is achieved by Q2 and the resistive divider formed by R6 and R7. As input voltage increases, the voltage at the base of Q2 increases causing Q2 to turn on harder which decreases the charging rate of C1 and further delays the firing of Q5.

To prevent the circuit from latching up at the beginning of each charging cycle, a delay network consisting of Q1 and its associated circuitry is used to prevent the current source from turning on until the trigger voltage has reached a sufficiently high level. This is achieved in the following way: Prior to the conduction of D2, the voltage on the base of Q1 is set by the voltage divider (R4 + R5)/(R1 + R3 + R4 + R5). This causes the base of Q1 to be more positive than the emitter and thus prevents Q1 from conducting until the voltage across R3 is sufficient to forward bias the base-emitter junction of Q1. This occurs when the line voltage has increased to about 15 volts.

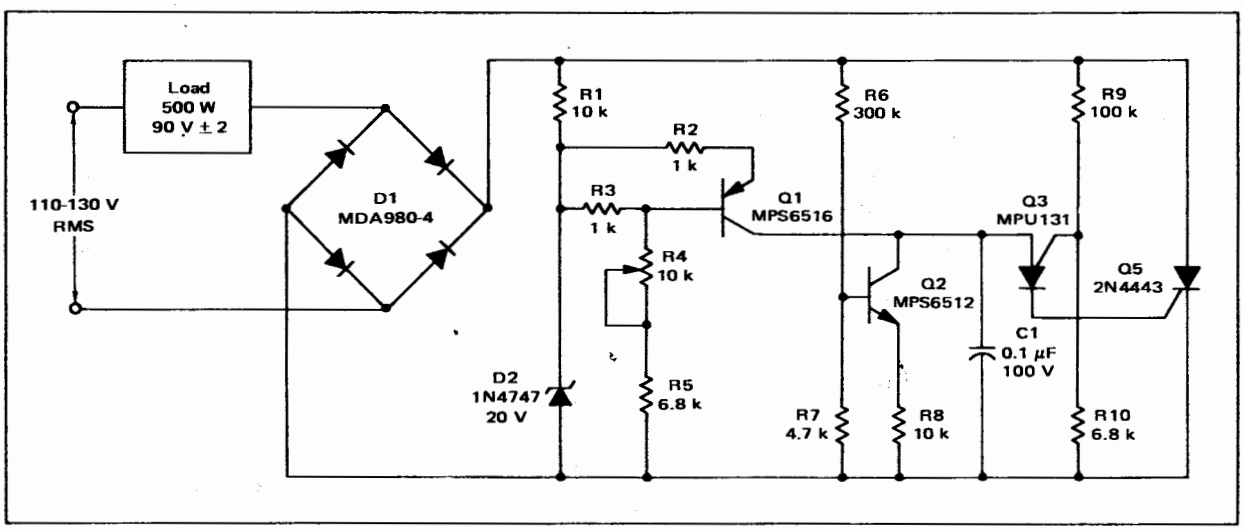

FIGURE 22 – RMS Voltage Regulator

The circuit can be operated over a different voltage range by changing resistors R6 and/or R4 which change the charging rate of C1.*

Figure 23 provides a plot of output voltage and conduction angle vs. input voltage for the regulator in Figure 22. As the figure indicates, good regulation can be obtained between the input voltage range of 110 to 130 volts.

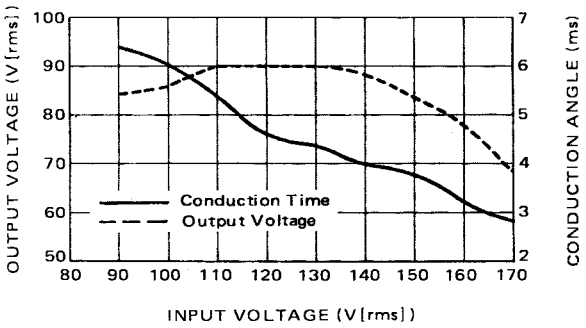

FIGURE 23 – Output Voltage and Conduction Angle Versus Input Voltage

*Further information about this circuit and other RMS regulators can be found in an application note, AN-509.