Leadless Power Package Cuts SO-8 Down to Size

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Now available from multiple sources, a 3.3-mm x 3.3-mm MOSFET package reduces pc-board space requirements by up to 63% versus the SO-8, while offering similar thermal and electrical performance.

A typical challenge power engineers face when designing voltage regulators is increasing power density of the power stage without downgrading performance. One way to achieve this is to use smaller MOSFET packages. A common package used for dc-dc conversion for current levels of 15 A or less has been the SO-8. However, by using a 3.3-mm × 3.3-mm leadless power package, case temperatures can be equivalent or better than the SO-8 across the load range for similar on-resistance ratings, and pc-board area consumed can be reduced by as much as 63%.

So, why take a look at the 3.3-mm × 3.3-mm power package now? Simply because this package has stood the test of time. It gives power engineers the flexibility to optimize designs. Most importantly, it is an excellent substitute for the SO-8 package, especially when space is an issue. Compared to the SO-8 package, a 3.3-mm × 3.3-mm package has three main benefits: a smaller size, better thermal resistance ratings and higher in-circuit performance.

When it was first introduced to the market seven years ago, there were no other MOSFET vendors offering this package. Now, due to its usefulness in power applications and demand from power engineers across market segments, there are multiple vendors offering the package with the exact same footprint.

In addition, when it was first introduced, customers were concerned about the solderability of this type of leadless package. Now, however, there is sufficient knowledge among original equipment manufacturers and original design manufacturers to use it without issues in manufacturing. Furthermore, advancements in silicon technology have made available both n-channel and p-channel MOSFETs in a 3.3-mm × 3.3-mm package with a wide range of drain-to-source voltage (V_{DS}) and gate-to-source voltage (V_{GS}) ratings as well as very low on-resistance ratings. Previously, such ratings could only be achieved with the SO-8 package.

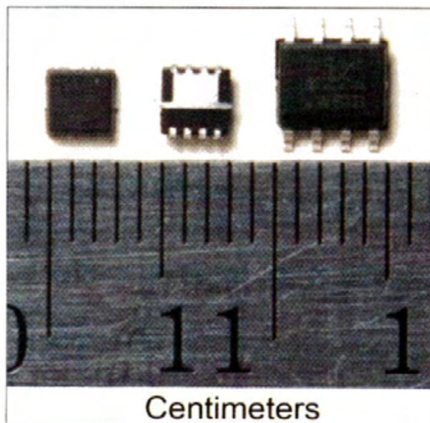

Fig. 1. *Top and bottom views of the 3.3-mm × 3.3-mm leadless package (left) show it is much smaller in size than an SO-8 package (right).*

Keeping Things Cool

The demand for the 3.3-mm × 3.3-mm power package arose from the need to keep the junction temperature of the MOSFET cooler as load current levels were rising, just as space was being reduced on the pc board.

A driving application for its use was point-of-load (POL) converters, especially one-sixteenth brick power modules, which needed maximum power density in a very small footprint. Mostly used in distributed power architectures requiring power conversion from the standard 48-V inputs down to 12 V and lower, this package was ideal not just for synchronous rectification, but also for primary-side switching. The proliferation of telecom equipment made this POL format attractive, and the 3.3-mm × 3.3-mm package helped optimize the power design.

The market trend continues in favor of this package style, especially in computers, which is helping to drive the package into the mainstream. While CPU current loads are still too high for the 3.3-mm × 3.3-mm package, it is ideal for lower-current rails like the memory voltage regulator (VR), which is a perfect application for it, especially in notebook PCs where board space is becoming a design constraint.

Package type	Profile (mm)	$R_{TH_{J-A}}$ maximum ≤ 10 sec (°C/W)	$R_{TH_{J-A}}$ maximum steady (°C/W)	$R_{TH_{J-C}}$ maximum steady (°C/W)	Power dissipation ≤ 10 sec (W)	Power dissipation steady (W)
3.3 mm x 3.3 mm	1.04	33	81	2.4	3.8	1.5
SO-8 6 mm x 4.9 mm	1.55	35	80	16.0	3.5	1.6

Table 1. *A comparison of dimensions and thermal resistance values for 3.3-mm × 3.3-mm and SO-8 packages.*

For other rails requiring between 5 A and 12 A of load current, the 3.3-mm × 3.3-mm power package is an excellent device to use for the high side and low side of a buck converter. This circuit has been dominated by the SO-8 package. However, test results show that the circuit can be handled with the smaller power package without downgrading performance. In addition, as more functions are integrated into the CPU, there will be more VRs required in a small area surrounding the CPU to convert voltage for different functions, leading to the need for smaller packages.

A Look at the Comparisons

Take a closer look at how the 3.3-mm × 3.3-mm package fares versus the SO-8. First, there's the smaller size. The nominal area of the package is 10.89 mm^2 compared to 29.4 mm^2 for the SO-8, an area reduction of 63%. As shown in Fig. 1, almost two packages can fit in the same area covered by one SO-8. In addition, the nominal profile or height of the package is 1.04 mm, which is 0.51 mm lower than that of the SO-8; this helps with height-constrained boards in cases where the package might need to fit under a heatsink or some other physical object. The layout of the package is similar to the popular 6-mm × 5-mm power package with a large drain pad on the bottom of the package and three leads in front for the source and one for the gate, which makes pc-board trace design convenient.

Second, the thermal resistance from junction-to-case for the 3.3-mm × 3.3-mm package is superior to the SO-8 package. As shown in Table 1,

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Function	Device	Package	V_{DS} (V)	V_{GS} (V)	$R_{DS_{ON}}$ maximum at 4.5 V (mΩ)	$R_{DS_{ON}}$ typical at 4.5 V (mΩ)	Total gate charge (Q_G) typical at 4.5 V (nC)	Gate-drain charge (Q_D) (nC)	Gate resistance typical (Ω)
High side	Si4800BDY	SO-8	30.0	25	30.0	23.0	8.7	3.5	1.40
	Si7326DN	3.3 x 3.3 mm	30.0	20	30.0	22.0	8.7	3.5	1.40
Low side	Si4386DY	SO-8	30.0	20	9.5	7.8	11.0	3.0	1.70
	Si7114DN	3.3 x 3.3 mm	30.0	20	10.0	8.1	12.5	3.6	1.40

Table 2. *A comparison of electrical specifications of the MOSFETs used in the case temperature evaluation.*

Function	Device	V_{DS} (V)	V_{GS} (V)	$R_{DS_{ON}}$ maximum at 10 V (mΩ)	$R_{DS_{ON}}$ maximum at 4.5 V (mΩ)	Q_G typical at 4.5 V (nC)	Gate-source charge (Q_{GS}) typical (nC)	Q_{GD} typical (nC)	R_G typical (Ω)
Low side	SIS402DN	30	20	6.00	8.00	12.0	5.4	4.6	1.2
High side	SI7716ADN	30	20	13.5	16.5	7.3	2.3	2.2	0.8

Table 3. *A comparison of electrical ratings for a pair of 3.3-mm × 3.3-mm MOSFETs used in a typical notebook computer (19 V_{IN}, 1.8 V_{OUT}, 300 kHz).*

the maximum rating steady state for the 3.3-mm × 3.3-mm package is around 2.4°C/W, whereas the SO-8 is rated around 16°C/W. The 3.3-mm × 3.3-mm package's thermal path from the junction of the MOSFET die to the board has less thermal resistance than the SO-8, even though its size is smaller, which means that heat can be dissipated more easily to the pc board. The drain pad on the bottom of the 3.3-mm × 3.3-mm package replaces the inferior thermal path of the eight leads of the SO-8, which are a thermal bottleneck. This value also impacts the maximum current-carrying capability of the package itself:

$$I_D = \sqrt{\left(\frac{(T_{J_{MAX}} - T_C)}{(R_{DS_{ON}} \times R_{TH_{J-C}})}\right)}.$$

The thermal resistance, junction-to-ambient, of the 3.3-mm × 3.3-mm package is similar to the SO-8, which is a value more critical when doing worst-case analysis. Both are roughly 33°C/W for a time less than 10 sec and 81°C/W for steady-state conditions. Finally, the power dissipation of the package is around 3.8 W, which is similar to the SO-8, making it an effective replacement.

Third, and most importantly, is the in-circuit analysis. While data-sheet comparisons are useful in comparing the two packages, the performance under typical operating conditions helps illustrate the 3.3-mm × 3.3-mm package's advantages.

Consider the case-temperature analysis across a load range in a dc-dc buck-converter circuit that compares the 3.3-mm × 3.3-mm package to the SO-8. The purpose of this test is to run MOSFETs with equivalent on-resistance ratings for the high side and the low side in both packages, so that a fair comparison of the package capability could be made. By measuring the case temperature, it can be determined how well the package manages the heat generated by the MOSFET die. The expectation was to have a performance level no worse than that of the SO-8 package per the thermal resistance and power dissipation specifications in the data sheet. This expectation was exceeded.

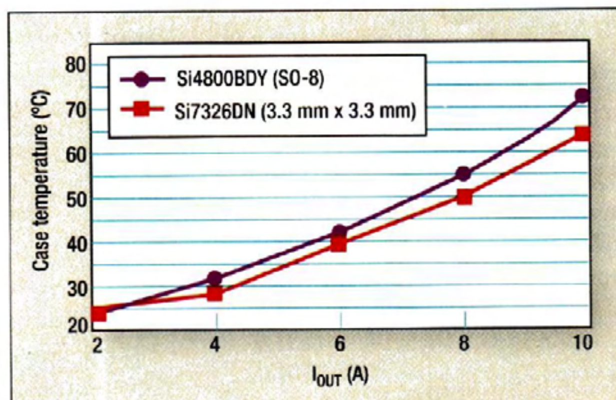

Fig. 2. *A MOSFET housed in a 3.3-mm × 3.3-mm package (the Si7326DN) features lower case temperatures as a function of load, compared with a MOSFET housed in an SO-8 package (the Si4800BDY), for the high-side switch.*

A conventional single-phase evaluation board was used with one unit for the high-side MOSFET and one unit for the low-side MOSFET. The case temperature was plotted against load current. The input voltage was 19 V, and the

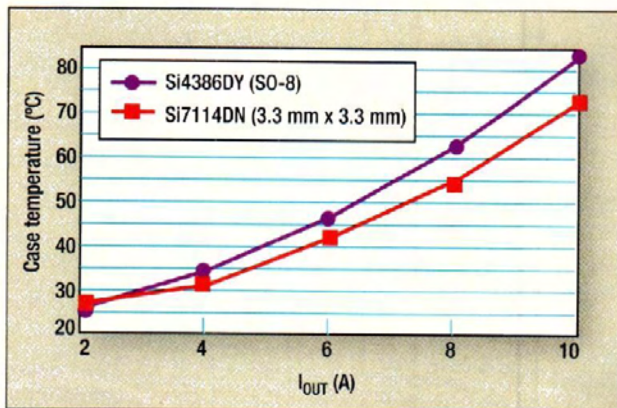

Fig. 3. *A MOSFET housed in a 3.3-mm × 3.3-mm package (the Si7114DN) features lower case temperatures as a function of load, compared with a MOSFET housed in an SO-8 package (Si4386DY), for the low-side switch.*

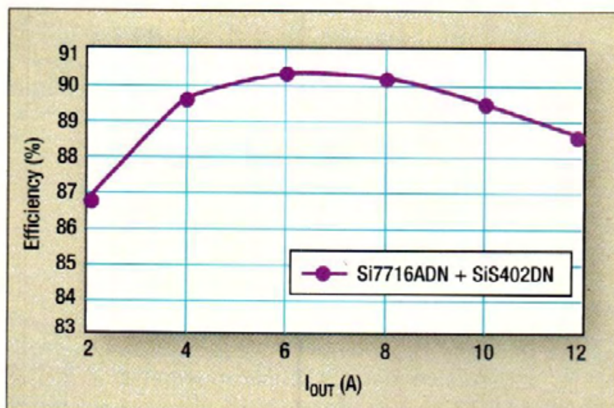

Fig. 4. *This curve shows that high efficiency levels, above 90%, can be achieved using a high-side MOSFET (Si7716ADN) and a low-side MOSFET (SiS402DN) used together, both packaged in the 3.3-mm × 3.3-mm leadless cases.*

output voltage was 1.2 V. The switching frequency was 300 kHz. The gate-drive voltage was 4.5 V.

This configuration was modeled after a typical notebook buck-converter application. Load current was swept from 2 A up to 10 A. Table 2 shows the comparable specification points for the high-side and low-side 30-V MOSFETs, using the same silicon technologies to isolate the performance of the package.

As shown in Figs. 2 and 3, the MOSFETs in the 3.3-mm × 3.3-mm package ran cooler than those in the SO-8 package across the entire load range. The case temperatures of the high-side MOSFETs were measured as well as the low-side ones. In Fig. 2, showing the high-side comparison, the smaller power package case temperature ran 6°C cooler than the SO-8 at 10 A at the maximum current load. In Fig. 3, for the low-side comparison, the smaller power package ran almost 10°C cooler at the maximum load. This is an important difference, because the maximum load is where the MOSFETs are most thermally challenged.

Further inspection of the curves reveals that the SO-8 case temperature for the low-side MOSFET reaches 85°C, which is a typical limit set by power engineers in open-air conditions. The 3.3-mm × 3.3-mm package still had more than 10°C headroom, allowing for higher current operation. The high-side MOSFET in the leadless power package had almost a 20°C margin. This advantage not only provides engineers a way to reduce space without degrading performance, but also a way to keep the power stage running cooler.

Now that it has been established the 3.3-mm × 3.3-mm power package is a viable alternative to the SO-8 package, it is possible to optimize the MOSFETs' electrical ratings, based on the application, to achieve the highest efficiency. For many lower-current dc-dc applications in the range of 4 A to 6 A, products with higher on-resistance ratings — such as 30 mΩ for the high side and 20 mΩ for the low side — seem to be the most popular solution in notebook PCs.

By using MOSFETs in 3.3-mm × 3.3-mm power packages with even lower on-resistance ratings, excellent efficiency levels above 9% can be achieved, above 90% in the same compact space (Fig. 4). For a 10-A to 15-A solution, one 30-V MOSFET rated at 13.5 mΩ typical at 4.5 V_{GS} for the high side and one rated at 6.4 mΩ typical at 4.5 V_{GS} for the low side can provide a high-efficiency solution for a typical 19-V input, 1.8-V output notebook application (Table 3). **PETech**

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