circuit file

Using the 4007UB 'FETset' IC

The 4007UB comprises two pairs of complementary MOSFETs and a simple MOSFET inverter stage, all independently accessible, which makes this simple IC a very versatile chip indeed.

Ray Marston

THE 4007UB is the simplest chip in the entire CMOS range. It contains little more than two pairs of complementary MOSFETs, plus a simple CMOS inverter stage. All of these elements are, however, independently accessible, enabling them to be configured in a wide variety of ways, thereby making the IC the most versatile in the entire CMOS range.

The 4007UB is an ideal device for demonstrating CMOS principles to students, technicians and engineers. It is sometimes known as the 'design-it-yourself' CMOS chip, and can readily be configured to act as a multiple digital inverter, NAND or NOR gate, transmission gate, or as a uniquely versatile 'micropower' linear amplifier, oscillator or multivibrator. We'll look at some practical examples of these applications later. In the meantime, let's look at 4007UB basics.

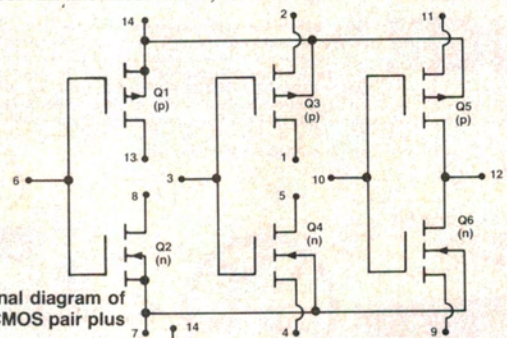


Figure 1a. **Functional diagram of the 4007UB dual CMOS pair plus inverter.**

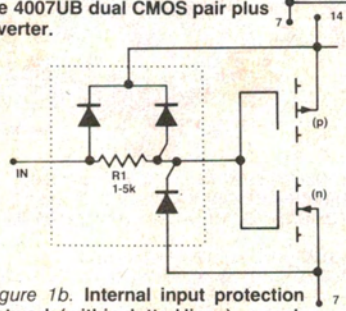


Figure 1b. **Internal input protection network (within dotted lines) on each input of the 4007UB.**

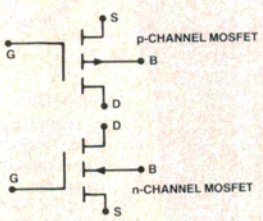


Figure 1c. **MOSFET terminal notations. G = Gate. D = Drain. S = Source. B = Bulk substrate.**

Basics: digital operation

Figure 1a shows the functional diagram and pin numbering of the 4007UB. Each of the three independent input terminals of the IC is internally connected to the standard CMOS protection network shown in Figure 1b. All MOSFETs in the 4007UB are enhancement-mode devices; Q1, Q3 and Q5 are p-channel MOSFETs, and Q2, Q4 and Q6 are n-channel MOSFETs. Figure 1c shows the terminal notations of the two MOSFET types; note that the B terminal represents the bulk substrate.

The term 'CMOS' actually stands for 'Complementary Metal Oxide Silicon field-effect transistors' and it is fair to say that all CMOS ICs are designed around the basic elements shown in Figure 1. It is thus worth getting a good basic understanding of these elements. Let's look first at the digital characteristics of the basic MOSFETs.

The input (gate) terminal of a MOSFET presents a near-infinite impedance, and the magnitude of an external voltage applied to the gate controls the magnitude of source-to-drain current flow. Basic characteristics of the enhancement-mode n-channel MOSFET are that the source-to-drain path is open circuit when the gate is at the same potential as the source, but becomes a near short-circuit (a low resistance) when the gate is heavily biased positive with respect to the source. Thus the

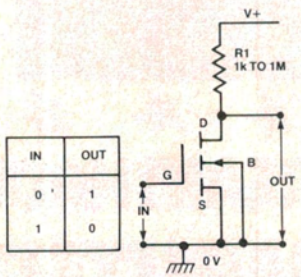


Figure 2. **Digital inverter made from n-channel MOSFET.**

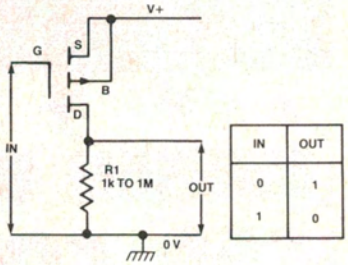


Figure 3. **Digital inverter made from p-channel MOSFET.**

n-channel MOSFET can be used as a digital inverter by wiring it as shown in Figure 2. With a logic 0 (zero volts) input the MOSFET is cut off and the output is at logic 1 (positive rail voltage), but with a logic 1 input the output is at logic 0.

Basic characteristics of the p-channel enhancement-mode MOSFET are that the source-to-drain path is open when the gate is at the same potential as the source, but becomes a near-short when the gate is heavily biased *negative* to the source. The p-channel MOSFET can thus be used as a digital inverter by wiring it as shown in Figure 3.

Note in the Figures 2 and 3 inverter circuits that the *on* currents of the MOSFETs are determined by the value of R1 and that these circuits draw a finite quiescent current when they are in one of their logic states. This snag can be overcome by connecting a complementary pair of MOSFETs in the standard CMOS inverter configuration shown in Figure 4a.

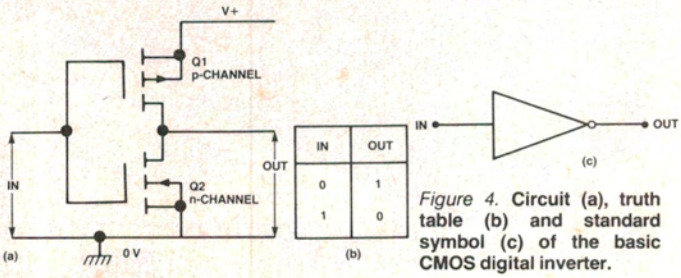


Figure 4. **Circuit (a), truth table (b) and standard symbol (c) of the basic CMOS digital inverter.**

Here, with a logic 0 input applied, Q1 is shorted, so the output is firmly tied to the logic 1 (positive rail) state, but Q2 is open and the inverter thus passes zero quiescent current via this transistor. With a logic 1 input applied, Q2 is shorted and the output is firmly tied to the logic 0 (zero volt) state, but Q1 is open and the circuit again passes zero quiescent current. This

'zero quiescent current' characteristic of the complementary MOSFET inverter is one of the most important features of the CMOS range of digital ICs, and the Figure 4a circuit forms the basis of almost the entire CMOS family. Figure 4c shows the standard symbol used to represent a CMOS inverter stage. Q5 and Q6 of the 4007UB are fixed-wired in this inverter configuration.

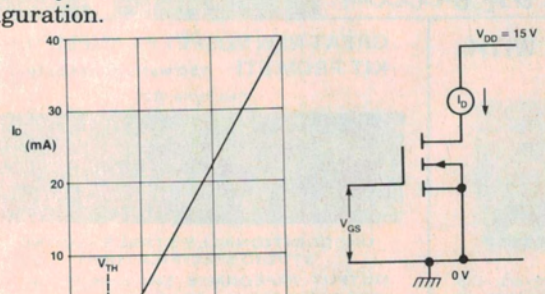


Figure 5. **Typical gate-voltage to drain-current characteristics of an n-channel MOSFET.**

Basics: linear operation

To truly understand the operation and vaguaries of CMOS circuitry, it is essential to understand the linear characteristics of basic MOSFETs. Figure 5 shows the typical gate-voltage to drain-current graph of an n-channel enhancement mode MOSFET. Note that negligible drain current flows until the gate voltage rises to a 'threshold' value of about 1.5 to 2.5 volts, but that the drain current then increases almost linearly with further increases in the gate voltage.

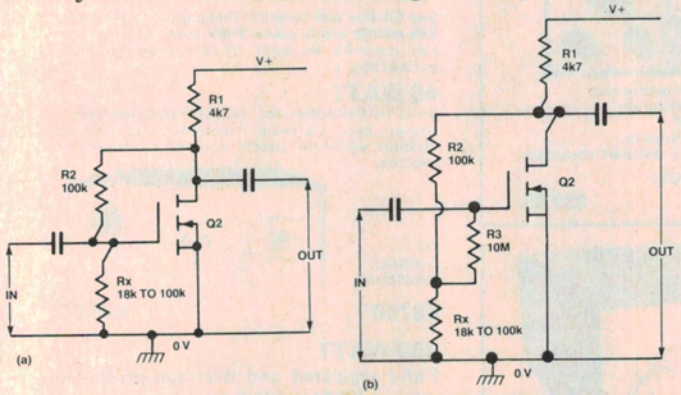


Figure 6. **Methods of biasing an n-channel 4007UB MOSFET for use as a linear inverting amplifier.**

Figure 6 shows how to connect an n-channel 4007UB MOSFET as a linear inverting amplifier. R1 serves as the drain load of Q2 and R2-Rx bias the gate so that the device operates in the linear mode. The Rx value must be selected to give the desired quiescent drain voltage; the Rx value is normally in the range 18k to 100k. If you want the amplifier to give a very high input impedance, wire a 10M isolating resistor between the R2-Rx junction and the gate of Q2, as shown in Figure 6b.

Figure 7 shows the typical I_D to V_{DS} characteristics of an n-channel MOSFET at various fixed values of gate-to-source voltage. Imagine here that, for each set of curves, V_{GS} is fixed at the V_{DD} voltage, but that the V_{DS} output voltage can be varied by altering the value of drain load R_L. The graph can be divided into two characteristic regions, as indicated by the dotted line, these being the triode region and the saturated region.

When the MOSFET is in the saturated region (with V_{DS} at some value in the nominal range 50% to 100% of V_{GS}) the drain acts like a constant current source, with it's current value controlled by V_{GS}. A low V_{GS} value gives a low constant-current value, and a high V_{GS} value gives a high constant-current value. These saturated 'constant-current' characteristics provide CMOS with its short-circuit proof feature and also determine it's operating speed limits at different supply voltage values.

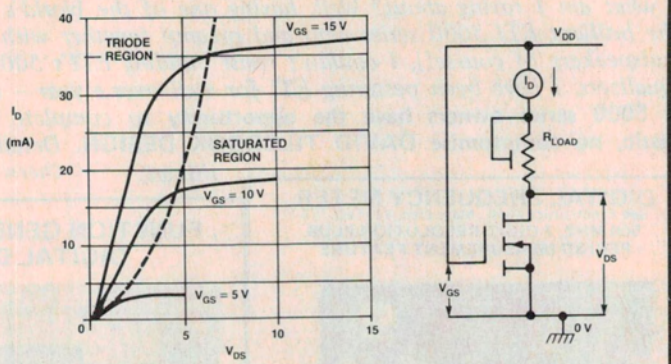


Figure 7. **Typical I_D to V_{DS} characteristics of the n-channel MOSFET at various fixed values of V_{GS}.**

When the MOSFET is in the triode region (with V_{DS} at some value in the nominal range 1% to 50% of V_{GS}) the drain acts like a voltage-controlled resistance, with the resistance value increasing approximately as the square of the V_{GS} value.

The p-channel MOSFET has an I_D to V_{DS} characteristics graph that is complementary to that of Figure 7. Consequently, the action of the standard CMOS inverter of Figure 4 (which uses a complementary pair of MOSFETs) is such that it's current-drive capability into an external load, and also it's operating speed limits, increases in proportion to the supply rail voltage.

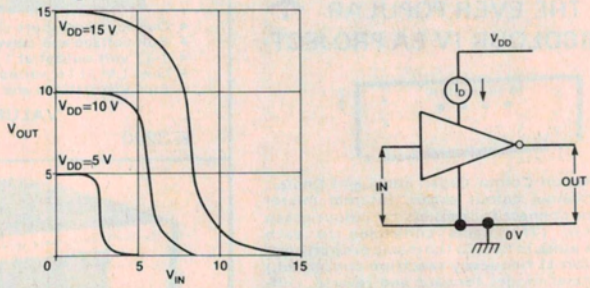


Figure 8. **Typical voltage transfer characteristics of the 4007UB simple CMOS inverter.**

Figure 8 shows the typical voltage-transfer characteristics of the standard CMOS inverter at different supply voltage values. Note (on the 15 V V_{DD} line, for example) that the output voltage changes by only a small amount when the input voltage is shifted around the V_{DD} and 0 V levels, but that when V_{in} is biased at roughly half-supply volts a small change of input voltage causes a large change of output voltage.

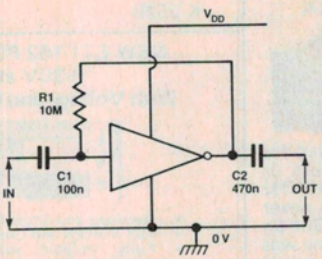


Figure 9. **Method of biasing the simple CMOS inverter for linear operation. Typical gain and bandwidth performance figures are 30 dB and 2.5 MHz at 15 V supply, 40 dB and 710 kHz at 5 V.**

Typically, the inverter gives a voltage gain of about 30 dB when used with a 15 V supply, or 40 dB at 5 V. Figure 9 shows how to connect the CMOS inverter for use as a linear amplifier; the circuit has a typical bandwidth of 700 kHz at 5 V supply, or 2.5 MHz at 15 V. ▶

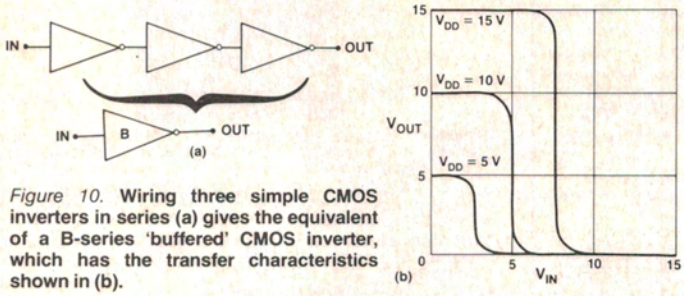
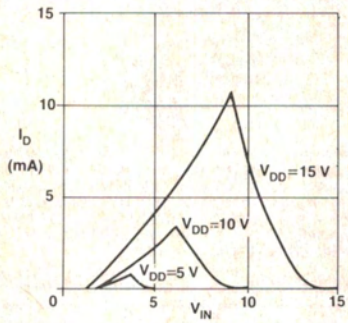


Figure 10. **Wiring three simple CMOS inverters in series (a) gives the equivalent of a B-series 'buffered' CMOS inverter, which has the transfer characteristics shown in (b).**

Wiring three simple CMOS inverter stages in series (Figure 10a) gives the direct equivalent of a modern B-series 'buffered' inverter stage, which has the overall voltage transfer graph shown in Figure 10b. The B-series inverter, typically gives about 70 dB of linear voltage gain, but tends to be grossly unstable when used in the linear mode.



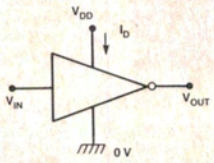


Figure 11. **Drain-current transfer characteristics of the simple CMOS inverter.**

Finally, Figure 11 shows the drain-current transfer characteristics of the simple CMOS inverter. Note that the drain current is zero when the input is at zero or full supply volts, but rises to a maximum value (typically 0.5 mA at 5 V supply, or 10.5 mA at 15 V supply) when the input is at approximately half-supply volts, under which condition both MOSFETs of the inverter are biased on. In the 4007UB, these *on* currents can be reduced by wiring extra resistance in series with the source of each MOSFET of the CMOS inverter; we use this technique in the 'micropower' circuits shown later in this article.

Using the 4007UB

The usage rules of the 4007UB are quite simple. In any specific application, all unused elements of the device must be disabled. Complementary pairs of MOSFETs can be disabled by connecting them as standard CMOS inverters and tying their inputs to ground, as shown in Figure 12. Individual MOSFETs can be disabled by tying their source to their substrate (B) and leaving the drain open circuit.

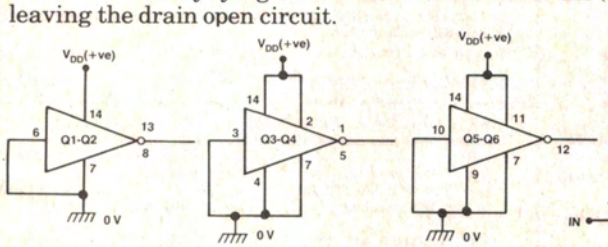


Figure 12. **Individual 4007UB complementary MOSFET pairs can be disabled by connecting them as CMOS inverters and grounding their inputs.**

In use, the input terminals must not be allowed to rise above V_{DD} (the supply voltage) or below V_{SS} (zero volts). To use an n-channel MOSFET, the source must be tied to V_{SS}, either directly or via a current-limiting resistor. To use a p-channel MOSFET, the source must be tied to V_{DD}, either directly or via a current-limiting resistor.

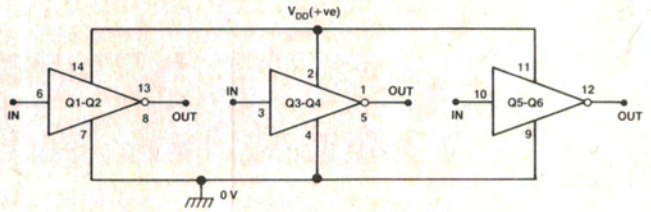


Figure 13. **4007UB triple inverter.**

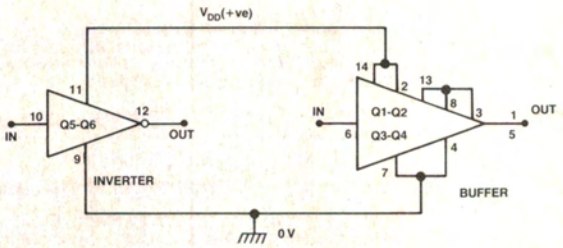


Figure 14. **4007UB inverter plus non-inverting buffer.**

Practical 4007UB circuits: digital

The 4007UB elements can be configured to act as any of a variety of standard digital circuits. Figure 13 shows how to wire it as a triple inverter, using all three sets of complementary MOSFET pairs. Figure 14 shows the connections for making an inverter plus non-inverting buffer; here, the Q1-Q2 and Q3-Q4 inverter stages are simply wired directly in series, to give an overall non-inverting action.

The maximum source (load-driving) and sink (load-absorbing) output currents of a simple CMOS inverter stage self-limit at 10-20 mA as one or other of the output MOSFETs turns fully on. Higher sink currents can be obtained by simply wiring n-channel MOSFETs in parallel in the output stage.

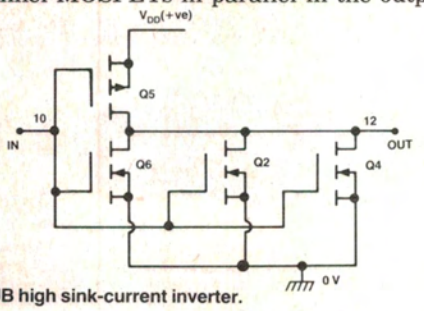


Figure 15. **4007UB high sink-current inverter.**

Figure 15 shows how to wire the 4007UB so that it acts as a high sink-current inverter that will absorb triple the current of a normal inverter. Similarly, Figure 16 shows how to wire the IC to act as a high source-current inverter, and Figure 17 shows the connections for making a single inverter that will sink or source three times more current than a standard inverter stage.

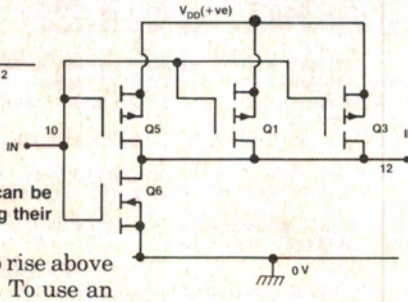


Figure 16. **4007UB high source-current inverter.**

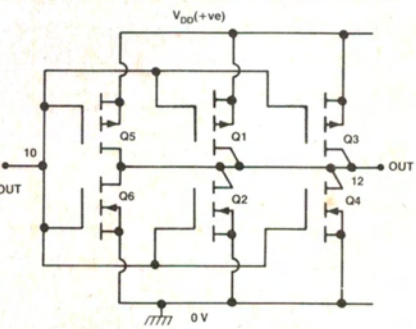
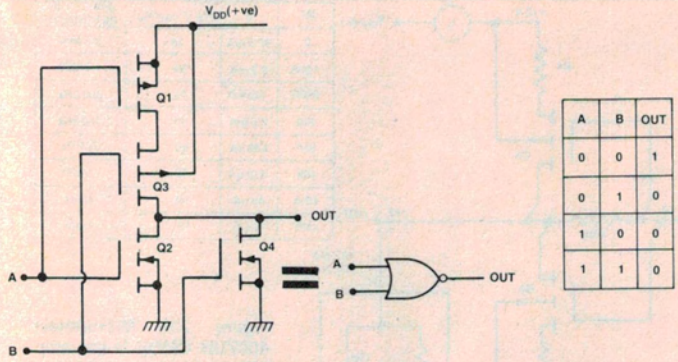


Figure 17. **4007UB high-power inverter, with triple the sink- and source-current capability of a standard inverter.**



A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	0

Figure 18. **4007UB two-input NOR gate.**

The 4007UB is a perfect device for demonstrating the basic principles of CMOS logic gates. Figure 18 shows the basic connections for making a two-input NOR gate. Note that the two n-channel MOSFETs are wired in parallel so that either can pull the output to ground from a logic 1 input, and the two p-channel MOSFETs are wired in series so that both must turn on to pull the output high from a logic 0 input. The truth table shows the logic of the circuit. A three-input NOR gate can be made by simply wiring three p-channel MOSFETs in series and three n-channel MOSFETs in parallel, as shown in Figure 19.

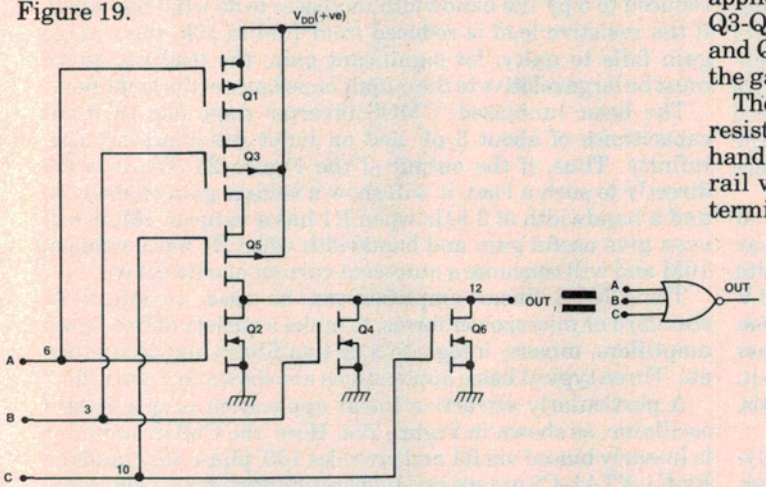
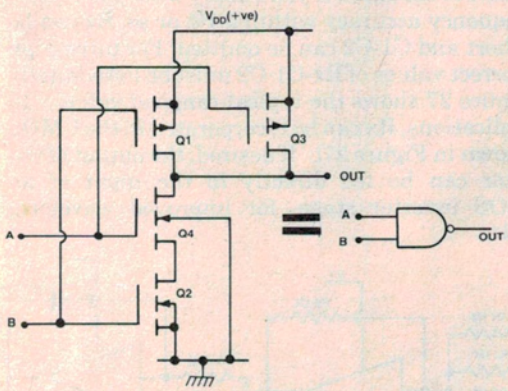


Figure 19. **4007UB three-input NOR gate.**



A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Figure 20. **4007UB two-input NAND gate.**

Figure 20 shows how to wire the 4007UB as a two-input NAND gate. In this case the two p-channel MOSFETs are wired in parallel and the two n-channel MOSFETs are wired in series. A three-input NAND gate can be made by similarly wiring three p-channel MOSFETs in parallel and three n-channel MOSFETs in series.

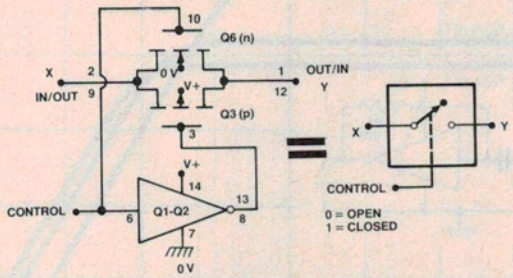


Figure 21. **4007UB transmission gate or bilateral switch.**

Figure 21 shows the basic circuit for using the 4007UB to make another important CMOS element, the so-called transmission gate or bilateral switch. This device acts like a near-perfect switch that can conduct signals in either direction and can be turned on (closed) by applying a logic 1 to the control terminal or turned off (open) via a logic 0 control signal. Here, an n-channel and a p-channel MOSFET are wired in parallel (source-to-source, drain-to-drain), but their gate signals are applied in anti-phase via the Q1-Q2 inverter. To turn the Q3-Q6 transmission gate on (closed), Q6 gate is taken to logic 1 and Q3 gate to logic 0 via the inverter. To turn the switch off, the gate polarities are simply reversed.

The 4007UB transmission gate has a near-infinite OFF resistance and an ON resistance of about 600 ohms. It can handle all signals between zero volts and the positive supply rail value. Note that, since the gate is bilateral, either of its terminals can function as input or output.

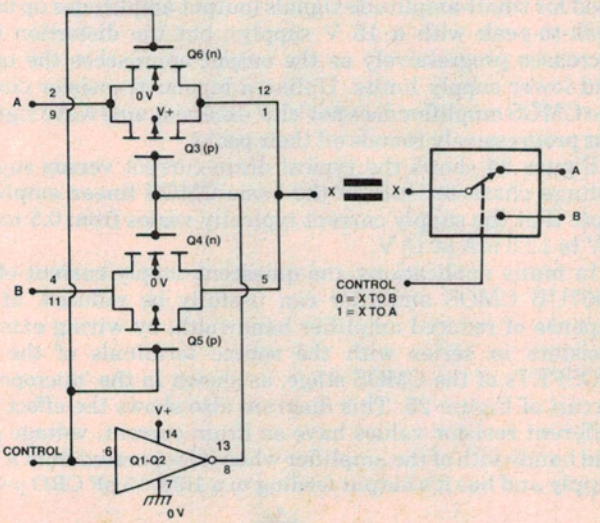


Figure 22. **4007UB two-way transmission gate.**

Finally, Figure 22 shows how the 4007UB can be wired as a dual transmission gate that functions like a single-pole double-throw (SPDT) switch. In this case the circuit uses two transmission elements, but their control voltages are applied in antiphase, so that one switch opens when the other closes, and vice versa; the 'X' sides of the two gates are shorted together, to give the desired SPDT action. ▶

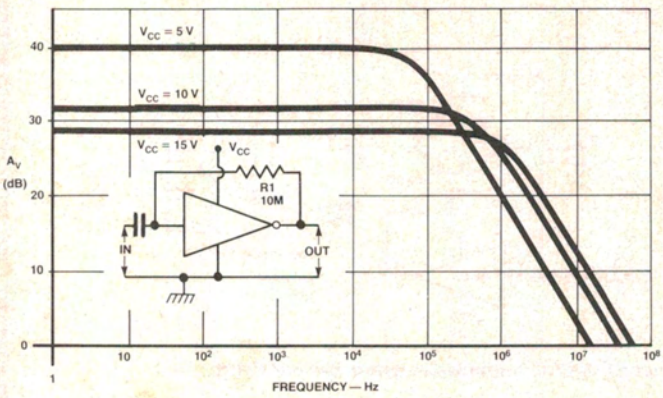
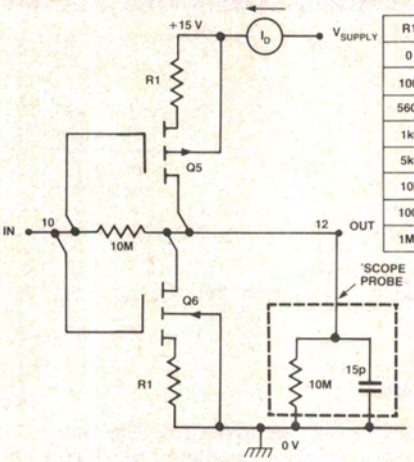


Figure 23. **Typical A_V and frequency characteristics of the linear-mode basic CMOS amplifier.**



R1	I_D	A_V (V_{OUT}/V_{IN})	UPPER 3 dB BANDWIDTH
0	12.5 mA	20	2.7 MHz
100R	8.2 mA	20	1.5 MHz
560R	3.9 mA	25	300 kHz
1k0	2.5 mA	30	150 kHz
5k6	600 uA	40	25 kHz
10k	370 uA	40	15 kHz
100k	40 uA	30	2 kHz
1M0	4 uA	10	1 kHz

Figure 25. **'Micropower' 4007UB CMOS linear amplifier, showing method of reducing I_D, with measured performance details.**

Practical 4007UB circuits: linear

We've already seen in Figures 6 and 9 that the basic 4007UB MOSFETs and the CMOS inverter can be used as linear amplifiers. Figure 23 shows the typical voltage gain and frequency characteristics of the linear CMOS inverter when operated from three alternative supply rail values. This graph assumes that the amplifier output is feeding into the high impedance of a 10M/15 pF 'scope probe. The output impedance of the open-loop amplifier typically varies from 3k at 15 V, to 5k at 10 V, to 22k at 5 V, and it is the product of the output impedance and output load capacitance that determines the bandwidth of the circuit, increasing the load capacitance or output impedance reduces the bandwidth.

As you would expect from the voltage transfer graph of Figure 8, the distortion characteristics of the CMOS linear amplifier are not particularly wonderful. Linearity is quite good for small-amplitude signals (output amplitudes up to 3 V peak-to-peak with a 15 V supply), but the distortion then increases progressively as the output approaches the upper and lower supply limits. Unlike a bipolar transistor circuit, the CMOS amplifier does not 'clip' excessive sine wave signals, but progressively rounds off their peaks.

Figure 24 shows the typical drain-current versus supply-voltage characteristics of the basic CMOS linear amplifier. Note that the supply current typically varies from 0.5 mA at 5 V to 12.5 mA at 15 V.

In many applications, the quiescent supply current of the 4007UB CMOS amplifier can usefully be reduced, at the expense of reduced amplifier bandwidth, by wiring external resistors in series with the source terminals of the two MOSFETs of the CMOS stage, as shown in the 'micropower' circuit of Figure 25. This diagram also shows the effect that different resistor values have on drain current, voltage gain and bandwidth of the amplifier when it is operated from a 15 V supply and has it's output feeding to a 10M/15 pF CRO probe.

It is very important to appreciate in the Figure 25 circuit that these additional resistors add to the output impedance of the amplifier (the output impedance is roughly equal to the R1-Av product) and this impedance and the external load resistance/capacitance has a great effect on the overall gain and bandwidth of the circuit. When using 10k values for R1, for example, if the load capacitance is increased to 50 pF the bandwidth falls to about 4 kHz, but if the capacitance is reduced to 5 pF the bandwidth increases to 45 kHz. Similarly, if the resistive load is reduced from 10M to 10k, the voltage gain falls to unity; for significant gain, the load resistance must be large relative to the output impedance of the amplifier.

The basic (unbiased) CMOS inverter stage has an input capacitance of about 5 pF and an input resistance of near-infinity. Thus, if the output of the Figure 25 circuit is fed directly to such a load, it will show a voltage gain of about 30 and a bandwidth of 3 kHz when R1 has a value of 1M; it will even give useful gain and bandwidth when R1 has a value of 10M and will consume a quiescent current of only 0.4 uA!

The CMOS linear amplifier can be used, in either its standard or micropower forms, to make a variety of fixed-gain amplifiers, mixers, integrators, active filters and oscillators, etc. Three typical basic applications are shown in Figure 26.

A particularly attractive linear application is as a crystal oscillator, as shown in Figure 27a. Here, the CMOS amplifier is linearly biased via R1 and provides 180° phase shift, and the Rx-C1-XTAL-C2 pi-type crystal network provides an additional 180° of phase shift at the crystal resonant frequency, thereby causing the circuit to oscillate. If you simply want the crystal to provide a frequency accuracy within 0.1% or so, Rx can be replaced by a short and C1-C2 can be omitted. For ultra-high accuracy, the correct values of Rx-C1-C2 must be individually determined (Figure 27 shows the typical range of values). In micropower applications, Rx can be incorporated in the CMOS amplifier, as shown in Figure 27b. If desired, the output of the crystal oscillator can be fed directly to the input of an additional CMOS inverter stage, for improved waveform shape/amplitude.

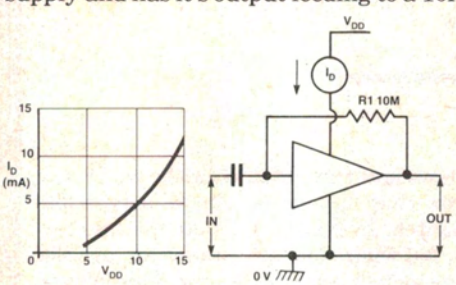


Figure 24. **Typical I_D/V_{DD} characteristics of the linear-mode CMOS amplifier.**

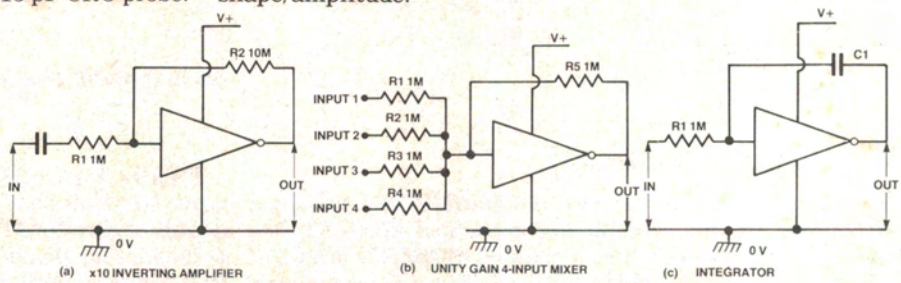


Figure 26. **The CMOS amplifier can be used in a variety of linear inverting amplifier applications. Three typical examples are shown here.**

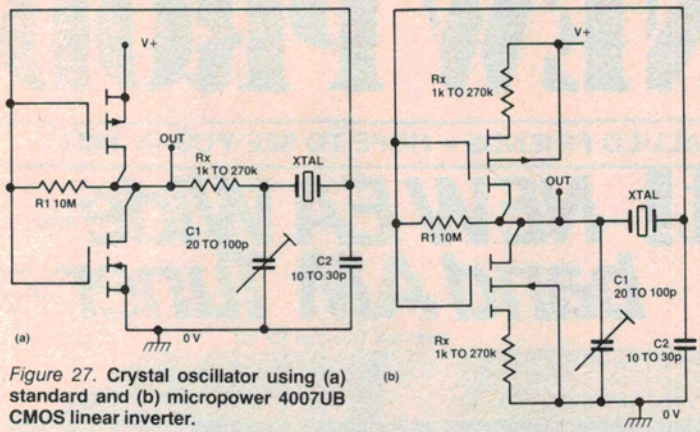


Figure 27. **Crystal oscillator using (a) standard and (b) micropower 4007UB CMOS linear inverter.**

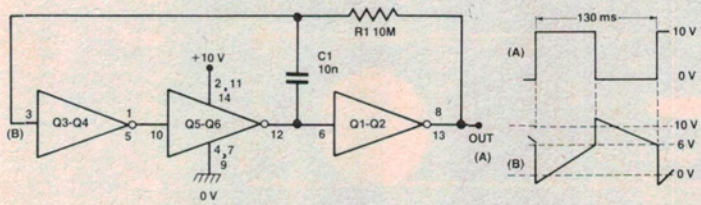


Figure 28. **This 4007UB ring-of-three astable consumes 280 uA at 6 V, 1.6 mA at 10 V.**

Practical 4007UB circuits: astables

One of the most useful applications of the 4007UB is as a ring-of-three astable multivibrator. Figure 28 shows the basic configuration of the circuit. Waveform timing is controlled by the values of R1 and C1, and the output waveform (A) is approximately symmetrical. Note that for most of the waveform period the front-end (waveform B) part of the circuit operates in the linear mode, so the circuit consumes a significant running current.

In practice, the running current of the Figure 28 astable circuit is far higher than that of an identically configured B-series 'buffered' CMOS chip such as the 4001B, the comparative figures being 280 uA at 6 V and 1.6 mA at 10 V for the 4007UB against 12 uA at 6 V and 75 uA at 10 V for the 4001B. The 4007UB circuit, however, has far lower propagation delays than the 4001B and typically has a maximum astable operating speed that is three times higher than that of the 4001B.

The running current of the 4007UB astable can be greatly reduced by operating it's first two stages in the 'micropower' mode, as shown in Figure 29. This technique is of particular value in low frequency operation, and the Figure 29 circuit in fact consumes a mere 1.5 uA at 6 V or 8 uA at 10 V, these figures being far lower than those obtainable from any other IC in the CMOS range. The frequency stability of the

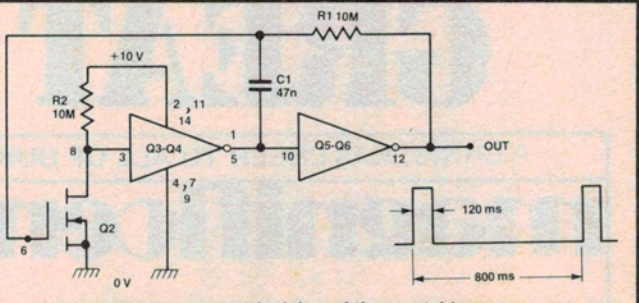


Figure 30. **This 4007UB asymmetrical ring-of-three astable consumes 2 uA at 6 V, 5 uA at 10 V.**

Figure 29 circuit is not, however, very good, the period varying from 200 ms at 6 V to 80 ms at 10 V.

Figure 30 shows how the 4007UB can be configured as an asymmetrical ring-of-three astable. In this case the 'input' of the circuit is applied to n-channel MOSFET, Q2. The circuit consumes 2 uA at 6 V or 5 uA at 10 V.

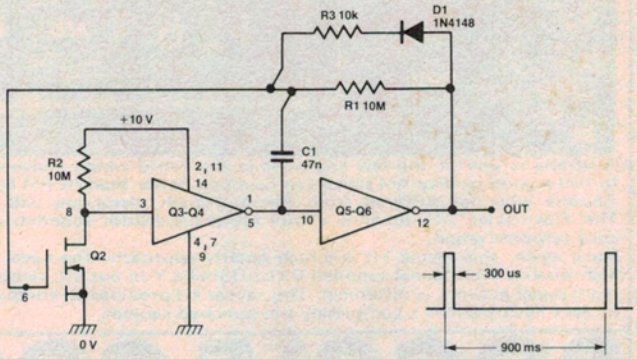


Figure 31. **This dual time constant version of the 4007UB astable generates a very narrow output pulse.**

Figure 31 shows how the symmetry of the above circuit can be varied by shunting R1 with the D1-R3 network, so that the charge and discharge times of C1 are independently controlled. With the component values shown, the circuit produces a 300 us pulse once every 900 ms and consumes a mere 2 uA at 6 V or 4.5 uA at 10 V. Note that these characteristics are similar to those of the ideal 'sample-pulse generator' circuit that was mentioned at the end of the last Circuit File, on Voltage and Window Comparators (ETI, November '82, pp 48-51).

Finally, to round off this edition of Circuit File, Figure 32 shows how the current consumption of the above circuit can be even further reduced, by operating the Q3-Q4 CMOS inverter in the micropower mode. The table gives details of circuit performance with alternative C1 and R3 values. This circuit will give years of continuous operation from a single battery supply. ●

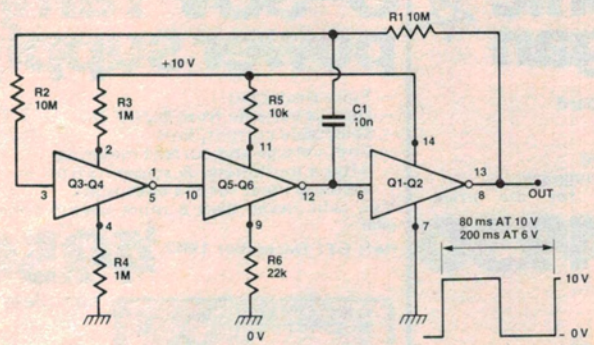
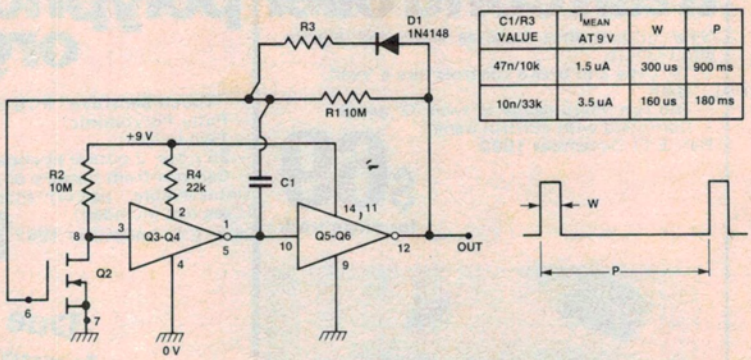


Figure 29. **This micropower ring-of-three symmetrical 4007UB astable consumes 1.5 uA at 6 V, or 8 uA at 10 V.**



C1/R3 VALUE	I_{MEAN} AT 9 V	W	P
47n/10k	1.5 uA	300 us	900 ms
10n/33k	3.5 uA	160 us	180 ms

Figure 32. **This micropower version of the 4007UB dual time constant astable consumes absolutely minimal currents.**