Micropower High Side MOSFET Drivers

Tim Skovmand

Portable electronic equipment, such as notebook and palmtop computers, portable medical instruments and battery powered tools, are increasingly dependent upon efficient power management to meet the challenge of extracting more useful energy (time) from less battery volume and weight.

One link in the power management chain which has received increasing scrutiny, as power supply efficiencies soar above 90%, is the logic controlled power switch. Large sections of a typical notebook computer system, for example, are powered via topside or "high side" MOSFET switches. These switches can become significant sources of power loss if not properly designed.

At first glance, P-channel MOSFETs appear to be the natural choice for high side switching. Unfortunately, the $R_{DS(ON)}$ exhibited by most P-channels is prohibitively high. (Mother Nature has decreed that electron mobility shall exceed hole mobility in silicon by about 2.5 times, so that a P-channel MOSFET with the same $R_{DS(ON)}$ and voltage rating as its N-channel counterpart is roughly 2 to 3 times larger and more expensive.) Also, the gate drive for a P-channel switch is limited to the supply voltage which may not fully enhance the switch as the supply voltage drops.

N-channel MOSFETs may seem less attractive because they require a gate voltage higher than the power supply voltage to become fully enhanced in high side switching applications. This limitation is eliminated by high side MOSFET drivers such as the LTC1155, which have built-in charge pumps to fully enhance N-channel switches.

The LTC1155, dual micropower MOSFET driver, generates 12V from a 5V rail to fully enhance logic-level N-channel switches with no external components required (see Figure 1). Further, the supply current is typically 85µA with the switch fully enhanced and 8µA with the LTC1155 in the standby mode (both inputs off). This combination of low-drop N-channel MOSFET switch and micropower

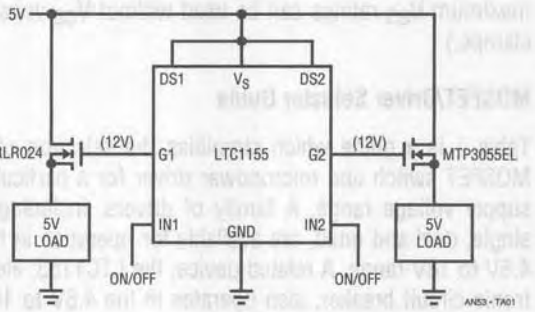

Figure 1. High Efficiency Dual High Side Switch

driver is the most efficient means of powering complex electrical loads. Switch efficiencies in the 98% to 99%+ range are easily attained with practical and economic N-channel switches.

MOSFET SWITCH SELECTION

N-channel MOSFET switches fall into two main categories: logic-level and standard.

Logic-Level MOSFET Switches

Although there is some variation among manufacturers, logic-level MOSFET switches are typically rated with V_{GS} = 4.0V with a maximum continuous V_{GS} rating of ±10V. $R_{DS(ON)}$ and maximum V_{DS} ratings are similar to standard MOSFETs and there is generally little price differential. Logic-level MOSFETs are frequently designated by an "L" and are usually available in surface mount packaging.

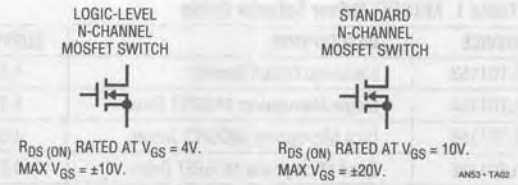

Figure 2. Logic-Level and Standard N-channel MOSFET V_{GS} Ratings

Standard MOSFET Switches

Standard N-channel MOSFET switches are rated with V_{GS} = 10V and are generally restricted to a maximum of ±20V. Again, there is some variation among MOSFET manufacturers and individual data sheets should be consulted before making a final selection. (E.g., MOSFETs with ±30V maximum V_{GS} ratings can be used without V_{GS} voltage clamps.)

MOSFET/Driver Selector Guide

Table 1 is a guide which simplifies the selection of a MOSFET switch and micropower driver for a particular supply voltage range. A family of drivers, including a single, dual and quad, are available for operation in the 4.5V to 18V range. A related device, the LTC1153, electronic circuit breaker, also operates in the 4.5V to 18V range.

The LTC1157, dual 3.3V micropower MOSFET driver, is designed specifically for low voltage operation between 2.7V and 5.5V. Finally, the LTC1255, dual high side MOSFET driver, is designed to work in the 9V to 24V automotive and industrial range.

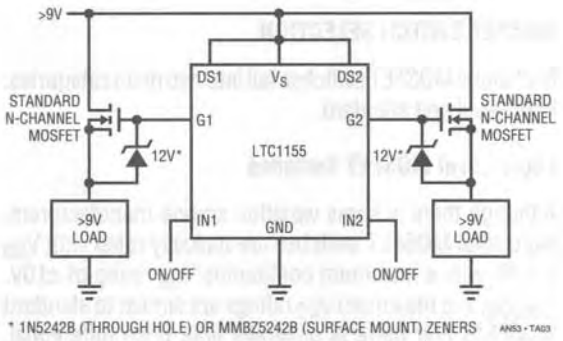

Figure 3. Adding 12V V_{GS} Clamps when V_S > 9V

Each driver works with either logic-level or standard MOSFETs over a portion of the supply voltage range and is designed to work with 12V V_{GS} Zener clamp diodes when the supply range exceeds 9V as shown in Figure 3.

APPLICATIONS

Powering Large Capacitive Loads

Electrical subsystems in portable battery powered equipment are typically bypassed with large filter capacitors to reduce supply transients and supply induced glitching. If not properly switched however, these capacitors may themselves become the source of supply induced glitching.

For example, if a 100µF capacitor is powered through a P-channel switch as shown in Figure 4, and the slew rate of the switch is 0.1V/µs, the current during start-up is:

$$I_{START} = C(dV/dt)$$
$$= (100 \times 10^{-6})(1 \times 10^{5})$$
$$= 10A$$

Obviously, this is too much current for the regulator to supply and the output glitches by many volts!

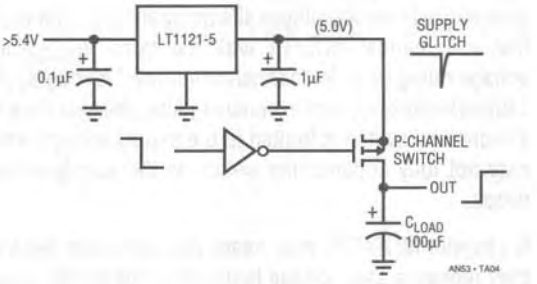

Figure 4. Power Up Supply "Glitch" Produced by Fast Starting a Large Capacitive Load

Table 1. MOSFET/Driver Selector Guide

DEVICE	DESCRIPTION	SUPPLY RANGE	USE LL FET	USE STD FET	STD FET & 12V CLAMP
LTC1153	Electronic Circuit Breaker	4.5V – 18V	4.5V – 5.5V	5.5V – 9V	9V – 18V
LTC1154	Single Micropower MOSFET Driver	4.5V – 18V	4.5V – 5.5V	5.5V – 9V	9V – 18V
LTC1155	Dual Micropower MOSFET Driver	4.5V – 18V	4.5V – 5.5V	5.5V – 9V	9V – 18V
LTC1156	Quad Micropower MOSFET Driver	4.5V – 18V	4.5V – 5.5V	5.5V – 9V	9V – 18V
LTC1157	Dual 3.3V high Side/Low Side Driver	2.7V – 5.5V	2.7V – 4.0V	4.0V – 5.5V	NA
LTC1255	Dual Industrial MOSFET Driver	9V – 24V	NA	NA	9V – 24V

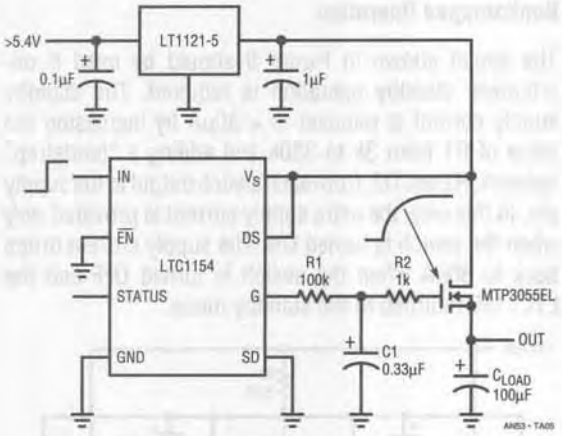

Figure 5. Slew Rate Reduction Network for Powering "Large" Capacitive Loads

The start-up current can be substantially reduced by reducing the slew rate at the gate of an N-channel switch as shown in Figure 5. The gate drive output of the LTC1154, single micropower MOSFET driver, is passed through a simple RC network, R1 and C1, which substantially slows the slew rate of the MOSFET gate to approximately 1.5 x 10^{-4}V/µs. Since the MOSFET is operating as a source follower, the slew rate at the source is essentially the same as that at the gate, reducing the start-up current to approximately 15mA which is easily managed by the system regulator. R2 is required to eliminate the possibility of parasitic MOSFET oscillations during switch transitions. Also, it is good practice to isolate the gates of paralleled MOSFETs with 1k resistors to decrease the possibility of interaction between switches.

Bidirectional Switch

Sometimes it is necessary to use "back-to-back" MOSFET switches to completely isolate the power source from the load, or from another power source, when the switch is turned off. This is the case when the supply voltage is higher or lower than the load voltage when powered by a secondary source.

A switched battery application, as shown in Figure 6, illustrates a bidirectional (fully isolated) switch. When the wall unit power supply is connected to V_{IN}, the load is disconnected from the battery by a fully isolated switch which allows the load voltage to fluctuate above or below the battery voltage without forcing current into the battery or pulling current out of it.

The bidirectional battery switch shown in Figure 7 illustrates how the LTC1154 drives two "back-to-back" low

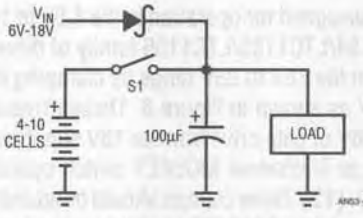

Figure 6. Switched Battery Application

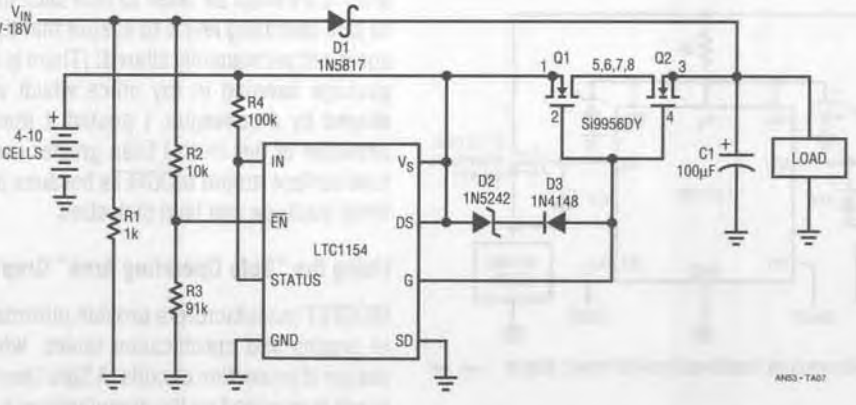

Figure 7. Bidirectional Switch Using Two "Back-to-Back" MOSFETs

$R_{DS(ON)}$ N-channel MOSFETs, Q1 and Q2, to fully disconnect the battery from the load immediately after the wall unit power supply is connected to V_{IN}. The two body diodes in Q1 and Q2 are also connected "back-to-back" and therefore no current can flow through the switch when the gate drive is removed.

The LTC1154 $\overline{\text{ENABLE}}$ input senses when the wall unit voltage exceeds 3V and inverts the action of the switch so that the two MOSFETs are turned off when the wall unit power supply is connected. The battery is subsequently reconnected immediately after the wall unit power supply is disconnected. D2 and D3 are only required for battery voltages above 9V and limit the gate drive voltage to the MOSFET switches to 12V above the battery voltage. C1 supplies load current during the short period of time (tens of microseconds) when the wall unit is disconnected and the battery switch is turned back on. R1 acts as a bleed resistor to ensure that the V_{IN} line is pulled down quickly after the the wall unit is unplugged.

18V – 28V Operation

Although designed for operation in the 4.5V to 18V range, the LTC1154/LTC1155/LTC1156 family of drivers can be operated in the 18V to 28V range by clamping the supply pin to 18V as shown in Figure 8. These drivers typically produce 36V of gate drive from an 18V supply which fully enhances an N-channel MOSFET switch operating from 18V to 28V. (12V Zener clamps should be added to ensure that the maximum MOSFET V_{GS} is never exceeded.)

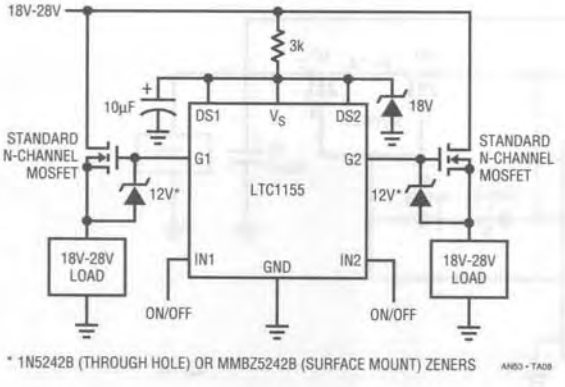

Figure 8. Using the LTC1155 from 18V to 28V

Bootstrapped Operation

The circuit shown in Figure 9 should be used if micropower standby operation is required. The standby supply current is reduced to < 30µA by increasing the value of R1 from 3k to 330k and adding a "bootstrap" network, R2 and D2, from each switch output to the supply pin. In this way, the extra supply current is provided *only* when the switch is turned ON. The supply current drops back to 30µA when the switch is turned OFF and the LTC1155 returned to the standby mode.

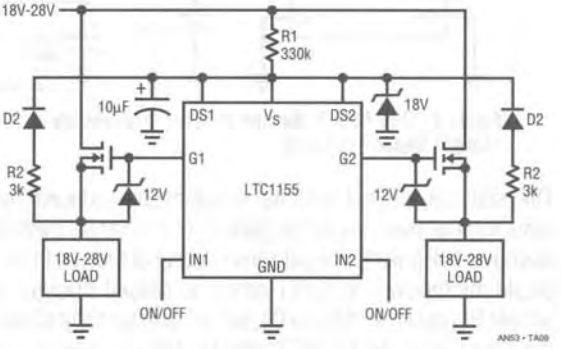

Figure 9. Bootstrapping the Supply

MOSFET SWITCH PROTECTION

Contrary to popular belief, power MOSFETs are not indestructible. They are more rugged, in some regards, than bipolar power transistors, but are still limited to operation within well defined current, voltage and power boundaries. Care must be taken to limit each of these quantities to safe operating levels to ensure that the MOSFET package is not permanently altered! (There is a power MOSFET package hanging in my office which was permanently altered by a colleague. I posted it there as a constant reminder of this truth.) Even greater care must be taken with surface mount MOSFETs because of their extremely small package and heat sink sizes.

Using the "Safe Operating Area" Graph

MOSFET manufacturers provide information, in the form of graphs and specification tables, which facilitate the design of protection circuits. A Safe Operating Area (SOA) graph is provided on the manufacturer's data sheet which establishes the electrical and physical limitations of the

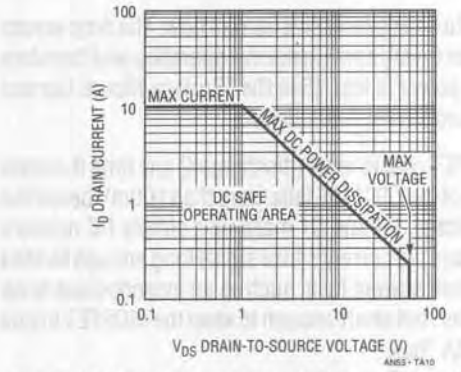

Figure 10. Typical Surface Mount MOSFET DC Safe Operating Area Graph

MOSFET in a particular package. Figure 10 is a generalized graph for a surface mount MOSFET. The X axis of the graph is drain-to-source voltage and the Y axis is drain current.

The DC Safe Operating "Box"

Three intersecting lines, along with the two axes, establish a "box" which bounds the DC Safe Operating Area (SOA) of the power MOSFET. Any excursion outside of these lines is considered destructive and must be avoided.

A horizontal line at the top of the graph specifies the maximum continuous drain current which can be conducted without damaging the leads or bond wires. Larger peak currents can be sustained for short periods and are sometimes indicated with a dotted horizontal line above the DC line.

A second line defines the maximum DC power that can be dissipated by the MOSFET package. The angle of the constant power line is –45°, as it is simply the product of voltage and current; i.e., the power dissipated at 1V and 10A is the same as that dissipated at 10V and 1A. So, a straight line intersecting these two points defines a maximum DC power dissipation limit of 10W. Note that there is no curvature in this line, as is typical in bipolar SOA graphs, because power MOSFETs do not suffer from the secondary breakdown characteristic exhibited by bipolar power transistors.

The *position* of the maximum power dissipation line is heavily dependent on the thermal resistance of the package and the external heat sinking. Surface mount packaged MOSFETs have substantially higher thermal resistance than those housed in metal cans or large plastic packages because of their small physical size and small heat sink footprint. Some surface mount MOSFET packages are scarcely larger than the silicon die they house. Therefore, surface mount MOSFETs have relatively low maximum DC power dissipation lines, typically in the range of 1W to 10W.

A third, vertical line, at the right-hand side of the graph, sets the upper limit of voltage exposure. This limit is set lower than the actual breakdown voltage of the MOSFET and should not be exceeded in normal operation. If the MOSFET is required to operate in the avalanche mode, the total energy dissipated must be held within the bounds set by the manufacturer in the Maximum Avalanche Energy graph which is sometimes given as a secondary measure of ruggedness.

The AC Safe Operating Area "Box"

Another set of lines on the SOA graph, as shown in Figure 11, establish the AC or pulsed capabilities of the MOSFET. These lines are dotted, and are drawn at the same –45° angle as the continuous DC power line, but have shorter and shorter time periods associated with them as they "move up" the graph. These lines define the maximum power which can be safely dissipated by the package and the heat sink for a given length of time. Because of their smaller package mass, surface mount MOSFETs are less able to dissipate energy (power × time) than those housed in large metal cans or plastic packages with large copper tabs (TO-220, etc.). And, therefore, greater care must be

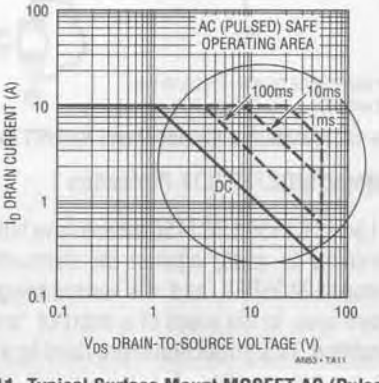

Figure 11. Typical Surface Mount MOSFET AC (Pulsed) Safe Operating Area Graph

taken to limit both the DC power dissipation and the AC (pulsed) power dissipation to safe levels.

Keeping the MOSFET Inside the "Box": A "Real" World Example

Armed with this information, it is now possible to develop protection schemes which ensure that the MOSFET stays inside the Safe Operating Area "box" and *inside the plastic package*! This process starts with an analysis of the electrical characteristics of the power source.

A NiCad battery pack, for example, is capable of supplying peak currents well in excess of the normal operating current of a typical load. The internal resistance of a typical NiCad cell is in the 0.025Ω to 0.1Ω range and therefore currents in the 10A to 50A range are possible. This is why NiCad batteries are not recommended for applications which might experience short circuit or "near" short circuit conditions, e.g. stalled motors. A surface mounted MOSFET switch powered from a NiCad battery pack, as shown in Figure 12, must be protected if it is to survive a momentary short across the motor or a sustained stall condition.

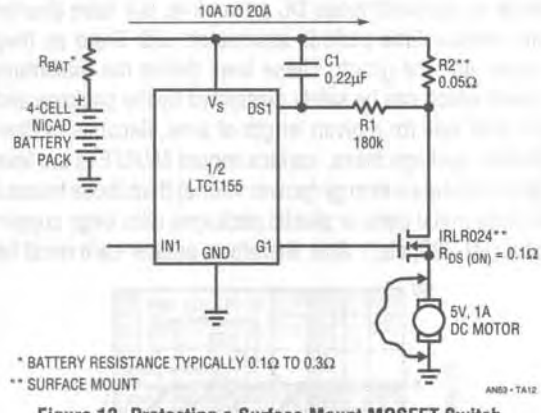

Figure 12. Protecting a Surface Mount MOSFET Switch

Surface Mount MOSFET SOA Protection

The LTC1154/LTC1155/LTC1156 drivers have built-in protection circuitry to guard against the destruction of a surface mount MOSFET, and the surrounding printed circuit board area, in the event of a short or "soft" short circuit condition. This protection is provided by a continuous drain current monitor. A small valued resistor or current shunt, R2, creates an IR drop which is used by the LTC1155 to detect excessive current flow. The drop across the resistor is very small in normal operation and therefore very little power is lost. (See the "Surface Mount Current Shunts" section for more detail.)

The MOSFET gate is reset (discharged) any time the drain sense pin of the LTC1155 falls more than 100mV below the supply voltage. R1 and C1 make up a simple RC network which delays the current sense signal long enough to start a high inrush current load, such as an incandescent lamp or DC motor, but short enough to keep the MOSFET inside the AC SOA "box."

Selecting R_{DELAY} and C_{DELAY}

Figure 13 is a graph of normalized over current shutdown time versus normalized MOSFET current. This graph is used to select the maximum RC time constant which will protect the MOSFET. The Y axis is normalized to one RC time constant. The X axis is normalized to the set current.

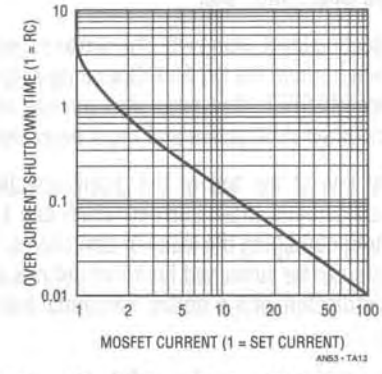

Figure 13. Shutdown Time vs MOSFET Current

The SOA graph for the surface mount MOSFET shown in Figure 11 indicates that it should not conduct 20A at V_{DS} = 5V for more than 10ms. The set current in our example is 2A (the set current is defined as the current required to develop 100mV across the drain sense resistor). 20A is 10 times the set current of 2A. By drawing a line up from 10 and reflecting it off the curve, we establish that the shutdown time at 20A is 0.1 × RC. The maximum RC time constant should therefore be set at 10 times 10ms, or 100ms. This time constant should be viewed as a maximum safe delay time and should be reduced if the competing requirement of starting a high inrush current load is less stringent; i.e. if the inrush time period is known to be

20ms, the RC time constant should be set at roughly 2 or 3 times this time period and not at the maximum of 100ms. A 40ms time constant would be produced with a 180k resistor and a 0.22µF capacitor as shown in Figure 12.

Note that the shutdown time in Figure 13 is shorter and shorter for increasing levels of MOSFET current — similar to a circuit breaker. It turns out that this is what is required by the MOSFET AC SOA graph; i.e. the product of power and time (energy) must be limited if the MOSFET is to be fully protected.

LOAD PROTECTION

As a general rule, the switch current should be terminated as quickly as possible during a short circuit or overload event. This rule is complicated somewhat by the nature of the load that is being protected.

Resistive Loads

Loads that are primarily resistive should be protected with as short a delay as possible to minimize the amount of time that the MOSFET and load are subjected to an overload condition. The drain sense circuitry has a built-in delay of approximately 10µs to eliminate false triggering by power supply or load transient conditions. This delay is sufficient to "mask" short load current transients and the starting of a small capacitor (<1µF) in parallel with the load. The drain sense pin can therefore be connected directly to the drain current sense resistor as shown in Figure 14.

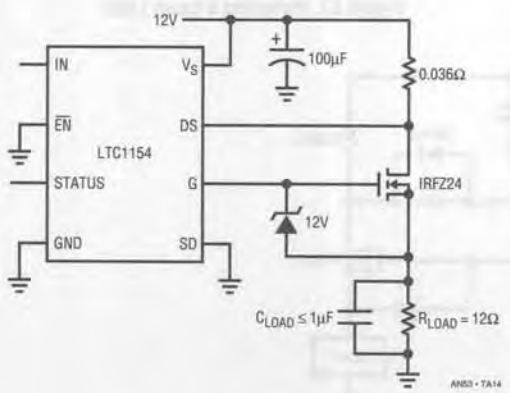

Figure 14. Protecting a Resistive Load

Inductive Loads

Loads that are primarily inductive, such as: relays, solenoids and stepper-motor windings should also be protected with as short a delay as possible to minimize the amount of time that the MOSFET and load are subjected to an over load condition. The built-in 10µs delay will ensure that the over current protection is not false triggered by a supply or load transient. No external delay components are required as shown in Figure 15.

Large inductive loads (>0.1mH) may require diodes connected directly across the inductor to safely divert the stored energy to ground. Many inductive loads have these diodes included. If not, a diode of the proper current rating should be connected across the load, as shown in Figure 15, to safely divert the stored energy.

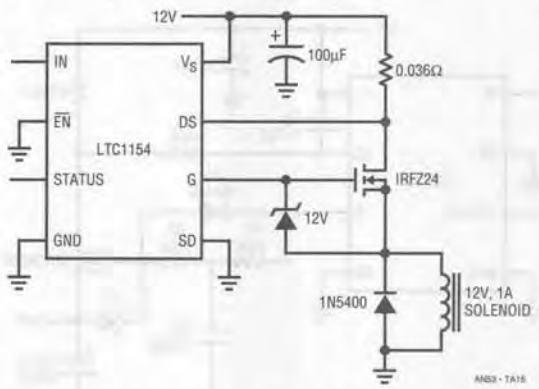

Figure 15. Protecting an Inductive Load

Capacitive Loads

Large capacitive loads, such as complex electrical systems with large bypass capacitors, should be powered using the circuit shown in Figure 16. The gate drive to the power MOSFET is passed through an RC delay network, R1 and C1, which greatly reduces the turn on ramp rate of the switch. And since the MOSFET source voltage follows the gate voltage, the load is powered smoothly and slowly from ground. This dramatically reduces the start-up current flowing into the supply capacitor(s) which, in turn, reduces supply transients and allows for slower activation of sensitive electrical loads. Diode, D1, provides a direct path for the LTC1154 protection circuitry to quickly discharge the gate in the event of an over current condition.

The RC network, R_D and C_D, in series with the drain sense input should be set to trip based on the expected characteristics of the load *after* start-up; i.e., with this circuit, it is possible to power a large capacitive load and still react quickly to an over current condition. The ramp rate at the output of the switch as it lifts off of ground is approximately:

$$dV/dt = (V_{GATE} - V_{TH})/(R1 \times C1)$$

And therefore the current flowing into the capacitor during start-up is approximately:

$$I_{START\text{-}UP} = C_{LOAD} \times dV/dt$$

Using the values shown in Figure 16, the start-up current is less than 100mA and does not false trigger the drain sense circuitry which is set at 2.7A with a 1ms delay.

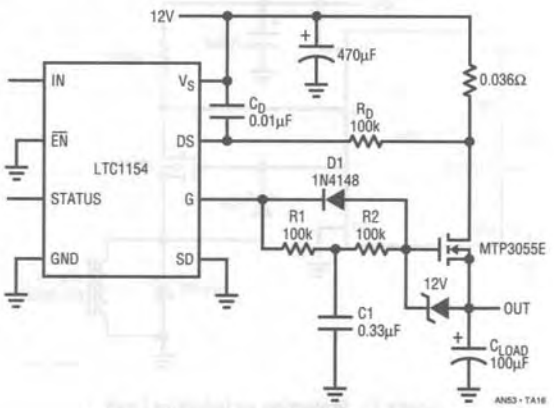

Figure 16. Powering a Large Capacitive Load

Lamp Loads

The inrush current created by a lamp during turn on can be 10 to 20 times greater than the rated operating current. The circuit shown in Figure 17 shifts the current limit threshold up by a factor of 11:1 (to 30A) for 100ms when the bulb is first turned on. The current limit then drops down to 2.7A after the inrush current has subsided.

Using a Speed-Up Diode

To reduce the amount of time that the power MOSFET is in a short circuit condition, "bypass" the delay resistor with a small signal diode as shown in Figure 18. The diode will engage when the drop across the drain sense resistor exceeds about 0.7V, providing a direct path to the sense pin and dramatically reducing the amount of time the

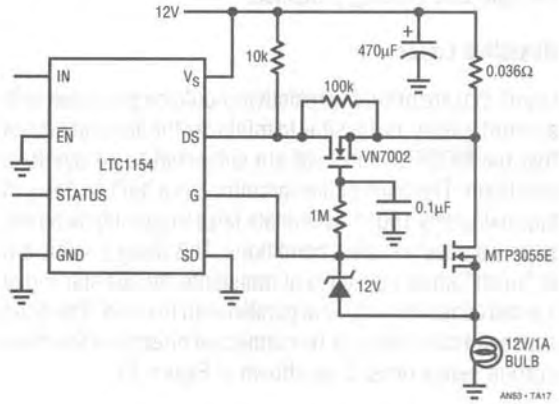

Figure 17. Protecting a Lamp Load

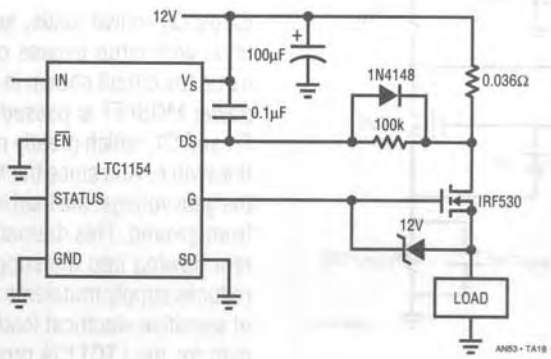

Figure 18. Using a Speed-Up Diode

MOSFET is in an over load condition. The drain sense resistor value is selected to limit the maximum DC current to 2.8A. The diode conducts when the drain current exceeds 20A and reduces the turn-off time to 15µs.

Reverse Battery Protection

The LTC1154/LTC1155/LTC1156 family of MOSFET drivers can be protected against reverse battery conditions by connecting a resistor in series with the ground lead as shown in Figure 19. The resistor limits the supply current to less than 50mA with –12V applied. Since the LTC1154 draws very little current while in normal operation, the drop across the ground resistor is minimal. The 5V µP (or control logic) is protected by the 10k resistors in series with the input, enable and status pins.

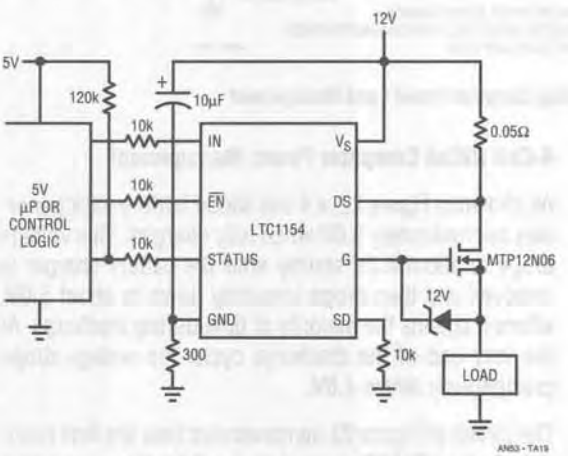

Figure 19. Reverse Battery Protection

Current Limited Power Supplies

The LTC1154/LTC1155/LTC1156 family of drivers require at least 3.5V at the supply pin to ensure proper operation. It is therefore necessary that the supply pin be held higher than 3.5V at all times, even when the output of the switch is short-circuited to ground. The output voltage of a current limited regulator may drop very quickly during short circuit and pull the supply pin of the LTC1154 below 3.5V before the shutdown circuitry has had time to respond and remove drive from the gate of the power MOSFET. A supply filter should be added as shown in Figure 20 which holds the supply pin of the LTC1154 high

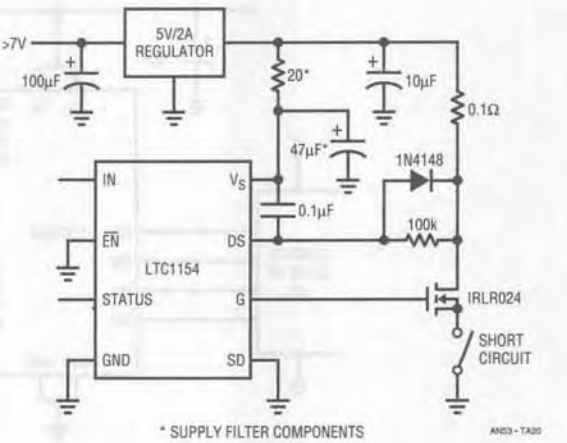

Figure 20. Supply Filter for Current Limited Supplies

long enough for the over current shutdown circuitry to respond and fully discharge the gate.

5V linear regulators with small output capacitors are the most difficult to protect as they can "switch" from a normal voltage mode to a current limited mode very quickly. The large output capacitors on many switching regulators, on the other hand, may be able to hold the supply pin of the micropower driver above 3.5V sufficiently long that this extra filtering is not required.

Because all of the drivers are micropower in both the standby and ON state, the voltage drop across the supply filter is less than 2mV, and does not significantly alter the accuracy of the 100mV drain sense threshold voltage.

NOTEBOOK COMPUTER POWER MANAGEMENT

Notebook computers are dependent upon low loss MOSFET switches to efficiently manage power and maximize the operating time from a single battery charge. High efficiency switching regulators and micropower standby circuits have also become crucial elements in the quest for increased operating time.

Notebook Load Management

One technique which is frequently used in notebook computers to conserve power is to disable high current loads when not in use. Figure 21 demonstrates how the LTC1156 quad MOSFET driver is used to power and protect four low loss

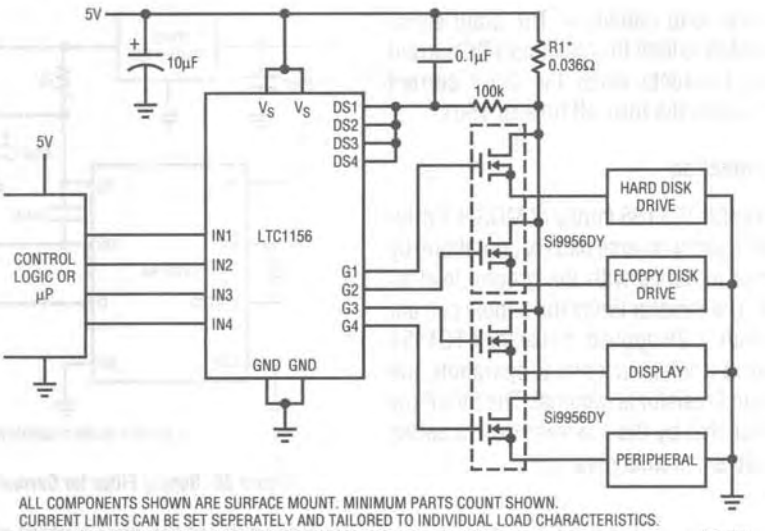

Figure 21. Quad High Side Switch for Laptop Computer Power Load Management

switches in a notebook computer power management system. Each load is a complex system which is only activated by the µP when it is required to process or display information. The rest of the time is spent in the standby mode where quiescent current is reduced to microamp levels to conserve power. The standby current of the LTC1156 is typically 16µA with all four inputs turned OFF.

The total current through the four switches is monitored by a very small valued resistor, R1, which drops less than 100mV at 2A. The LTC1156 current sense circuitry continuously monitors this resistor and ensures that the offending switch is turned OFF in the event the voltage drop exceeds 100mV. A short delay has been added to eliminate false triggering. The switches are re-engaged after the short circuit condition is removed by turning the inputs OFF and then back ON. It should be noted that the circuit shown in Figure 21 is the minimum parts count implementation. The LTC1156 contains four separate current limit circuits which can be tailored to the individual load characteristics. All the components shown in Figure 21 are available in surface mount packaging, including the current sense resistor (see the Current Shunt section for more detail).

4-Cell NiCad Computer Power Management

As shown in Figure 22, a 4-cell NiCad battery pack generates approximately 5.6V when fully charged. This voltage drops to about 5.2V shortly after the battery charger is removed and then drops smoothly down to about 5.0V, where it spends the majority of time during discharge. At the very end of the discharge cycle, the voltage drops precipitously below 4.6V.

The circuit of Figure 23 demonstrates how the first channel of an LTC1156 is used to regulate the output of a

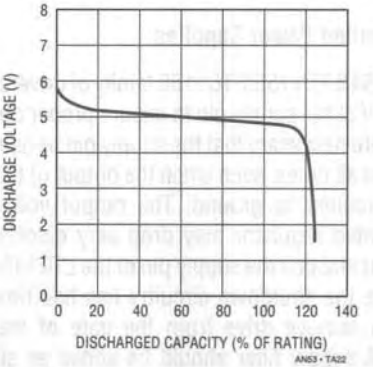

Figure 22. Typical 4-cell NiCad Discharge Characteristic

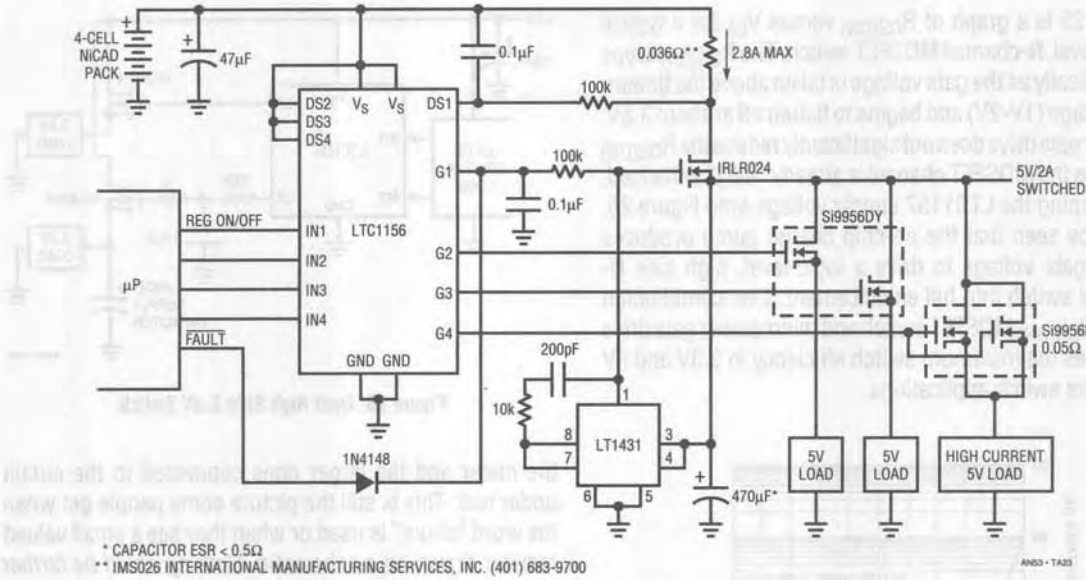

Figure 23. A 4-cell NiCad Computer Power Management System

four-cell NiCad battery pack to power a notebook or palmtop computer system. This approach forgoes the expense and complexity of a switching regulator to convert the battery voltage to 5V. The regulator consists of the first channel of the LTC1156 and an LT1431 programmable reference. As long as the input voltage to the regulator is sufficient to produce 5V at the output, the regulator output will limit at 5V. When the battery pack voltage drops below 5V, the MOSFET becomes fully enhanced and acts as a direct connection between the battery and the computer circuitry. A simple battery voltage monitor in the µP decides when the battery voltage drops off below 4.6V and house keeping is performed (storing data, etc.) before the batteries are completely discharged. The other three channels of the LTC1156 act as simple switches under µP control to intelligently power the other 5V sections of the computer. The number of switches can be increased by adding more LTC1155 or LTC1156 circuits as needed. All of the components shown in Figure 23, with the exception of the regulator output capacitor, are surface mount and occupy a very small amount of board space. The large capacitor value is required to maintain good load regulation during large changes in load current.

High Side Switching at 3.3V

Many circuits in notebook and palmtop computers are being designed to operate at 3.3V. The LTC1157, dual low voltage MOSFET driver, is specifically designed for operation between 2.7V and 5.5V where P-channel switches are less attractive because they are not rated with V_{GS} below 4.0V.

The LTC1157 internal charge pump boosts the gate drive voltage 5.4V above the positive rail (8.7V above ground) as shown in Figure 24, fully enhancing a logic-level N-channel MOSFET for 3.3V high side switching applications.

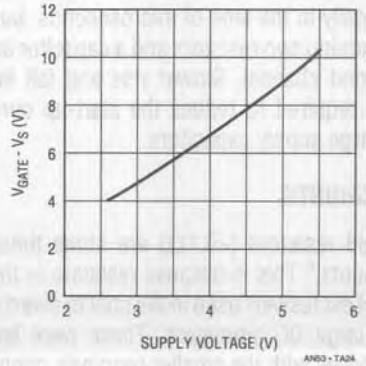

Figure 24. LTC1157 Gate Voltage *Above* Supply

Figure 25 is a graph of $R_{DS(ON)}$ versus V_{GS} for a typical logic-level, N-channel MOSFET switch. The $R_{DS(ON)}$ drops dramatically as the gate voltage is taken above the threshold voltage (1V-2V) and begins to flatten off at about 3.5V. Further gate drive does not significantly reduce the $R_{DS(ON)}$ because the MOSFET channel is already "fully" enhanced. By mapping the LTC1157 supply voltage onto Figure 25, it can be seen that the on-chip charge pump produces ample gate voltage to drive a logic-level, high side N-channel switch into full enhancement. This combination of low $R_{DS(ON)}$ MOSFET switch and micropower gate drive produces the maximum switch efficiency in 3.3V and 5V high side switch applications.

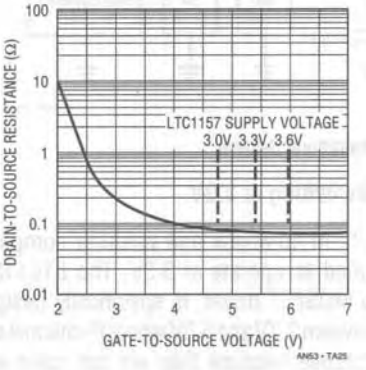

Figure 25. Typical Logic-Level N-Channel MOSFET $R_{DS(ON)}$

Figure 26 demonstrates how two surface mount MOSFETs and the LTC1157 (also available in 8-pin SO packaging) can be used to switch two 3.3V loads. The gate rise and fall time is typically in the tens of microseconds, but can be slowed by adding two resistors and a capacitor as shown on the second channel. Slower rise and fall times are sometimes required to reduce the start-up current demands of large supply capacitors.

CURRENT SHUNTS

Small valued resistors (<0.1Ω) are some times called "current shunts." This is because resistors in this range were almost exclusively used in the past to divert or shunt current in large DC ammeters. These were large four terminal devices with the smaller terminals connected to

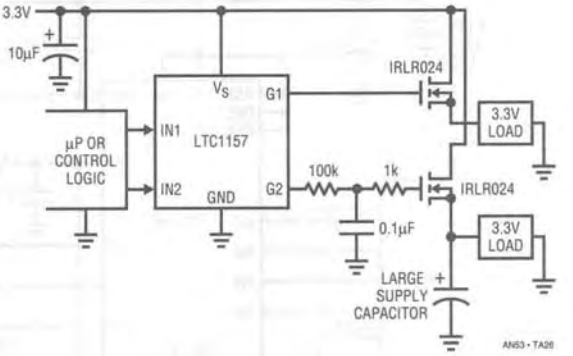

Figure 26. Dual High Side 3.3V Switch

the meter and the larger ones connected to the circuit under test. This is still the picture some people get when the word "shunt" is used or when they see a small valued resistor drawn on a schematic. *Nothing could be farther from the truth!* Current shunts (small valued resistors) are now used in a wide variety of current sensing applications including: motor controllers, switching regulators, industrial and automotive load switches and portable computer power management systems, and in significantly smaller packaging.

Surface Mount Current Shunts

All of the current shunts shown in this application note are small surface mount resistors which occupy a tiny fraction of the board space once required to sense large (1A-30A) currents. This is true, not only because of advances in surface mount package technology, but because the small voltage drops (<100mV) required by the LTC1154/LTC1155/LTC1156 to sense current reduces the power dissipation in the sense resistor to surprisingly small levels.

Figure 27 is a graph of power dissipation versus set current for a sense resistor used with the LTC1154/LTC1155/LTC1156. The set current is defined as the current required to develop 100mV across the resistor. It is assumed in this calculation that the nominal load current is 50% of the set current and therefore the nominal drop across the resistor is 50mV. Note that the power dissipation and, therefore the resistor power rating, is quite small even at large set currents. For example, the

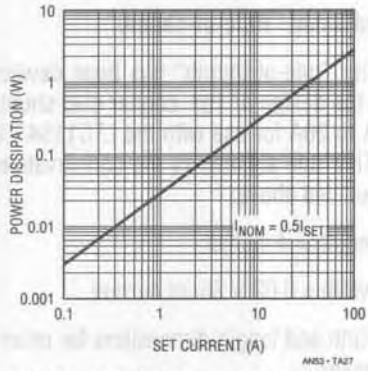

Figure 27. Sense Resistor Power Dissipation vs Set Current

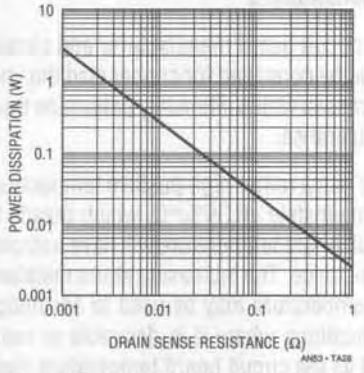

Figure 28. Sense Resistor Power Dissipation vs Sense Resistance

power dissipated by a 0.05Ω resistor (I_{SET} = 2A) is only 50mW and is therefore extremely small (the same size as a standard value surface mount resistor). The power dissipated by a 0.01Ω resistor (I_{SET} = 10A) is only 0.25W and is still quite small.

Figure 28 is similar to Figure 27, except the X axis has been converted from set current to sense resistor value. Either graph can be used to determine the power rating of the sense resistor.

Current Shunt Manufacturers

Table 2 is a list of surface mount resistors suitable for sensing MOSFET drain current. Both two terminal and four terminal resistors are available. Kelvin connections are usually not required however above 0.01Ω if the printed circuit board is designed carefully, i.e. with the "force" traces leading to the power supply and MOSFET drain, and the "sense" traces leading to the driver.

Table 2. Surface Mount Shunt Manufacturers

MANUFACTURER	PART NUMBERS
Dale Electronics, Inc. 1122 23rd Street Columbus, NE 68601 (402) 563-6506	WSC-1/2 WSC-1 WSC-2
International Manufacturing Services, Inc. 50 Schoolhouse Lane Portsmouth, R.I. 02871 (401) 683-9700	IMS026
International Resistive Company, Inc. P.O. Box 1860 Boone, NC 28607 (704) 264-8861	MSM-1 MSM-2 LR2010 LR2512
Isotek Corporation 566 Wilbur Ave. Swansea, MA 02777 (508) 673-2900	SMR SMV
Ohmite Manufacturing Co. 3601 Howard St. Skokie, IL 60076 (708) 675-2600	RW1S0BA RW1S5CA RW2S0CB
KRL/Bantry Components, Inc. 160 Bouchard St. Manchester, NH 03103 (603) 668-3210	SL-1 SL-2 SL-3

Printed Circuit Board Shunts

A carefully designed printed circuit board trace can be used in place of a current shunt in applications where tolerances can be relaxed, and where sufficient board space is available. This technique is inherently less accurate than using a 2 or 4 wire low resistance current shunt, but is sufficiently accurate for many applications.

Printed circuit board copper is expressed in units of ounces of copper per square foot, i.e. 1/2oz., 1oz., 2oz., etc. The thickness of 1oz. copper clad is approximately 1.35 mils (0.00343 cm). Since the resistivity of pure copper is 1.822 μΩ-cm, the "sheet" resistance of a 0.00343 cm thick layer of copper is approximately 530μΩ/

square. This means that a section of 1oz. copper clad, one unit long by one unit wide, has a resistance of 530μΩ regardless of the unit size.

For example, a 0.01Ω resistor to sense 10A, would be approximately 20 squares long, i.e. the strip would be 1 unit wide by 20 units long. The area of the trace must be large enough to dissipate the power produced by a 10A current flow without over stressing the copper or the laminate beneath it. A maximum current density of 50A/inch width of 1oz. copper is considered conservative and therefore a 10A, 0.01Ω,1oz. copper clad shunt should be 0.2 inches wide and 4 inches long as shown in Figure 29.

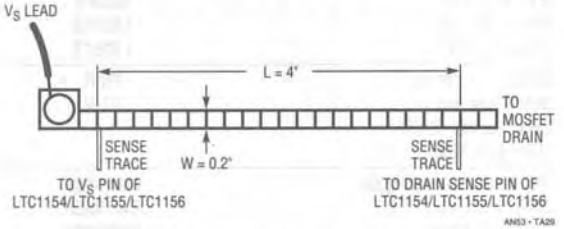

Figure 29. 0.01Ω Printed Circuit Board Current Shunt

Note that there are four connections to the shunt. The two "force" connections are made to the power supply and the drain of the MOSFET. The smaller "sense" connections are made along the length of the shunt. The length of the resistor is defined by the distance between the two sense traces and not by the total length of the force trace.

It is also possible to turn corners with the shunt as shown in Figure 30. Each corner square however is counted as 0.6 squares (318μΩ) instead of a "whole" square (530μΩ). This is because the current flowing through the corner square does not flow uniformly but is concentrated at the inside corner. The total resistance is calculated by adding the number of corner squares times 0.6 plus the number of mid body squares and multiplying by the per square resistance as shown in Figure 30.

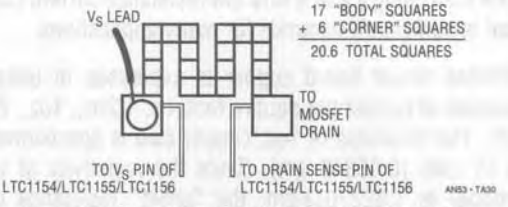

Figure 30. 'Serpentine' 0.01Ω Printed Circuit Board Current Shunt

Copper Clad Shunt "Rule-of-Thumb"

The following "rule-of-thumb" has been developed for simplifying the design of 1oz. copper clad shunts in the range of 1A to 20A for use with the LTC1154/LTC1155/LTC1156. This rule adheres to the conservative design approach outlined above:

Shunt length = 4 inches

Shunt width = 0.02 × Shunt current

Scale the width and length dimensions for other copper clad thicknesses.

Further Considerations

The printed circuit board manufacturer and circuit board etcher should be consulted for copper clad thickness and etching tolerances which ultimately determine the copper clad shunt tolerance.

Also, copper has a rather high positive temperature coefficient, approximately +0.39%/°C, which means that the printed circuit board temperature will have a strong effect on shunt resistance. The increasing shunt resistance with increasing temperature may be used to advantage however in applications where it is desirable to reduce the current limit as the circuit board temperature rises.

LTC1153: Electronic Circuit Breaker

The LTC1153 electronic circuit breaker is related to the LTC1154/LTC1155/LTC1156 family of micropower MOSFET drivers and is most similar to the LTC1154. The LTC1153 is designed to work with a low cost, N-channel power MOSFET to interrupt power to a sensitive electronic load in the event of an over current condition. The breaker is tripped by an over current condition and remains tripped for a period of time programmed by an external timing capacitor, C_T. The switch is then automatically reset and the load momentarily retried. If the load current is still too high, the switch is shutdown again. This cycle continues until the over current condition is removed, thereby protecting the sensitive load and the power MOSFET.

The gate voltage for the high side MOSFET N-channel switch is generated completely on-chip by a high frequency charge pump, similar to the LTC1154/LTC1155/LTC1156.

Programmable Timing

The trip current, trip delay time and auto-reset period are programmable over a wide range to accommodate a variety of load impedances. Figure 31 demonstrates how the LTC1153 is used in a typical circuit breaker application. The DC trip current is set by a small valued resistor, R_{SEN}, in series with the drain lead which drops 100mV when the current limit is reached. In the circuit of Figure 31, the DC trip current is set at 1A (R_{SEN} = 0.1Ω).

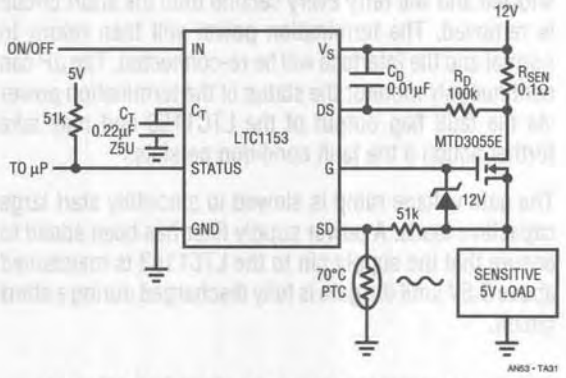

Figure 31. LTC1153 5V/1A Circuit Breaker with Thermal Shutdown

The trip delay time is set by the two delay components, R_D and C_D which establish an RC time constant in series with the drain sense resistor, producing a trip delay which is shorter for increasing breaker current (similar to a mechanical circuit breaker). Figure 32 is a graph of the trip delay time versus the circuit breaker current for a 1ms RC time constant. Note that the trip time is 0.63ms at 2A, but falls to 55µs at 20A. This characteristic ensures that the load, and the MOSFET switch, are protected against a wide range of overload conditions.

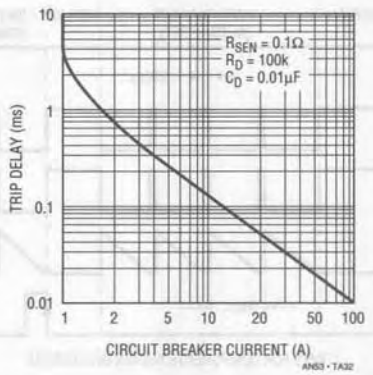

Figure 32. Trip Delay Time versus Breaker Current (for circuit shown in Figure 31).

Auto Reset Function

The auto-reset time is typically set in the range of tens of milliseconds to a few seconds by selecting the timing capacitor, C_T. The auto-reset period for the circuit in Figure 31 is 200ms, i.e. the circuit breaker is automatically reset (retried) every 200ms until the overload condition is removed. The switch then returns to normal operation and continues to power the load until another fault condition is encountered.

An open drain status output is provided to warn the host µP whenever the circuit breaker has been tripped. The µP can either wait for the auto-reset function to reset the load, or shut the switch OFF after a fixed number of retries.

A shutdown input is also provided which interfaces directly with a PTC thermistor to sense over temperature conditions and trip the circuit breaker whenever the load temperature, or MOSFET switch temperature, exceeds a safe level. The thermistor shown in Figure 31 trips the circuit breaker when the load temperature exceeds approximately 70°C.

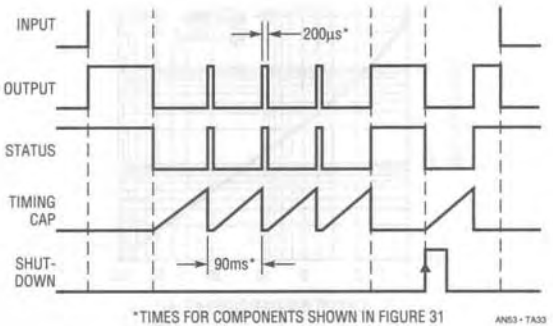

Figure 33. LTC1153 Typical Timing Diagram

Figure 33 is a timing diagram with some typical waveforms generated by the circuit breaker in the normal operating mode, the overload mode and the shutdown mode. Note that the timing capacitor, C_T, is held low until a fault condition is encountered and then charged by a small internal current source until the threshold is reached and the switch turned back on. This cycle continues until the overload is removed and the switch returned to normal operation.

The termination power for a SCSI interface is protected to avoid damaging the drivers, the connectors and the printed circuit board in the event of a short circuiting of the connector or interconnecting cable. This protection is provided by the circuit breaker circuit shown in Figure 34. With the component values shown, the DC current is limited to 1A with a trip delay time constant of 1ms. The breaker will trip if the cable or connector is accidently shorted and will retry every second until the short circuit is removed. The termination power will then return to normal and the interface will be re-connected. The µP can continuously monitor the status of the termination power via the fault flag output of the LTC1153 and may take further action if the fault condition persists.

The gate voltage ramp is slowed to smoothly start large capacitive loads. A power supply filter has been added to ensure that the supply pin to the LTC1153 is maintained above 3.5V until the gate is fully discharged during a short circuit.

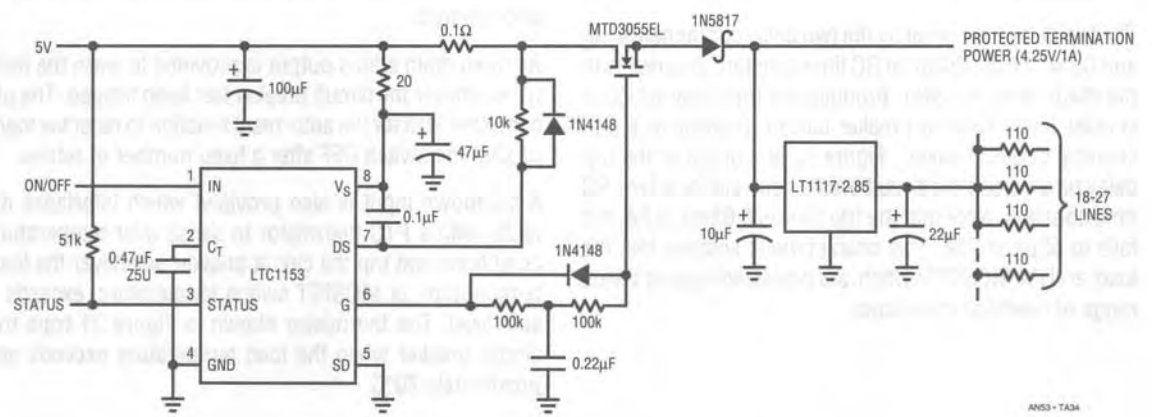

Figure 34. LTC1153 SCSI Termination Power Protection