Sets 27 & 28: Complementary m.o.s.

The first few cards of set 27 form a useful potted summary of the properties of complementary f.e.ts for readers not wholly familiar with c.m.o.s. devices. Properties that characterize these devices—high input impedance, low quiescent consumption, relatively wide supply range, large output swing—are dealt with first, page 92, followed by dynamic considerations and device equations on page 93, and then modes of connection on page 94. Another characteristic feature is the very wide variation in dissipation with supply voltage, page 93, and the pronounced sensitivity of c.m.o.s. devices to voltage is more fully illustrated by the curves of page 96.
Many circuits based on op-amps can be constructed using c.m.o.s. inverters and gates. Examples included are the rectangular-to-triangle wave converter of page 101, the two- and three-phase oscillators of pages 108 & 109, and the filters of pages 104 & 105. Eight sensing and detection applications are given in pages 106 & 107, using the D-type flip flop.
(Typographical slips on card 6 have been corrected on page 108—they involved incorrect inequality signs in the first and last few lines.)

Linear c.m.o.s. circuits

By considering the various families of logic circuits one can deduce what parameters, designed-in to optimize digital operation, result in adverse performance if the circuits are used in the analogue mode. The most interesting family that is available at a low cost is complementary symmetry metal oxide semiconductor logic or c.m.o.s. By adding an extra diffusion to the processing steps needed for a single type of device, Fig. 1, the complementary type can be produced. Thus the p-channel device is obtained by diffusing p^+ source and drain into the n-type substrate; a deeper p-type well is diffused to contain the n-channel device.

In addition to the conducting channels between the respective sources and drains, there are a number of p-n junctions. Though these are normally reverse-biased by the selected operating mode, their parasitic effects cannot always be ignored. Other p-n junctions are deliberately introduced at the inputs to prevent damage to the thin oxide films by high voltages that might be produced electrostatically or due to external transients.

The conductivity of the channels is increased by a forward bias on the gates. For an n-channel device this corresponds to a gate voltage positive with respect to the source. The conductivity tends to zero for zero gate-source voltage because the doping of the channel is such that there are virtually zero current carriers available. At a particular value of gate voltage, called the threshold voltage, charges induced in the channel by the resulting field allow conduction to commence. No gate current flows because of the insulation provided by the oxide layer. Drain-source conductivity continues to increase with rising gate-source voltage, while the current flow depends on both V_{gs} and V_{ds}. At low values of V_{ds}, the slope resistance is reasonably linear and is controlled by V_{gs}. Ultimately, the output current reaches a limiting value again set by V_{gs} i.e. the output slope resistance becomes very high making the device suitable for various forms of constant-current circuits.

The basic inverter stage is shown in Fig. 2 and the transfer function in Fig. 3. When the input voltage is low, there is insufficient forward bias on the n-channel device to bring it above the threshold of conduction. The reverse is true for the p-channel device which has a high conductivity i.e. the output is virtually equal to $+V_s$. Conversely a very positive input voltage pushes the output close to zero. When lightly loaded the output swings to within 1% of the supply voltage. At voltages in the region of $+V_s/2$ both transistors are conducting. This region is traversed rapidly when the inverter is used as a

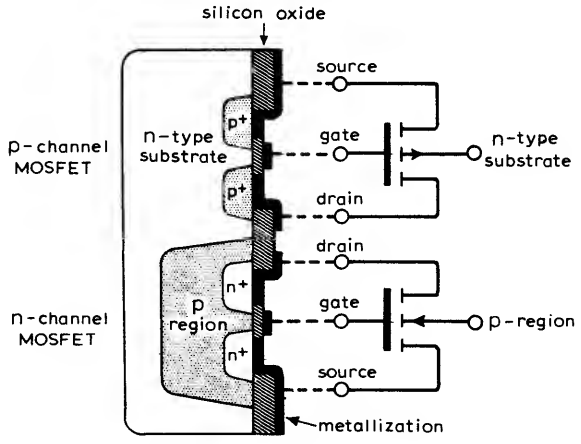


Fig. 1. Structure of c.m.o.s. inverter.

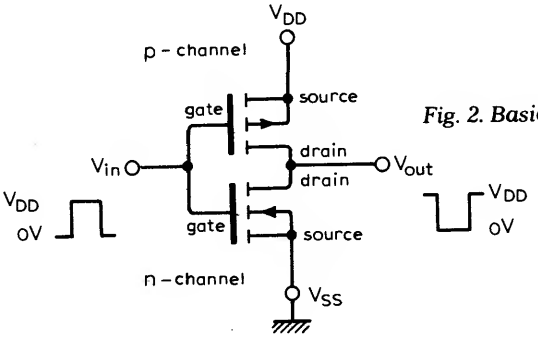


Fig. 2. Basic c.m.o.s. inverter.

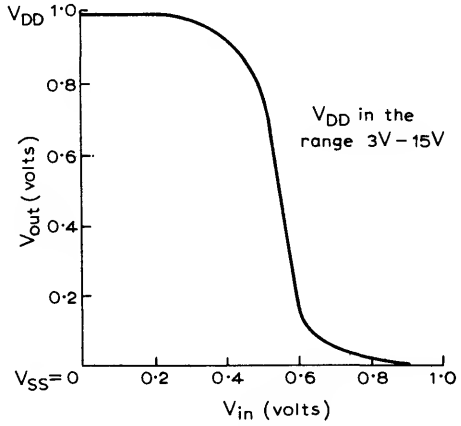


Fig. 3. Transfer function of c.m.o.s. inverter.

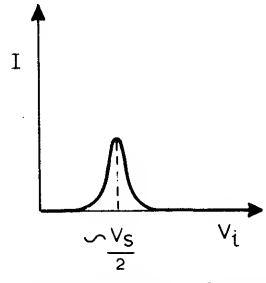


Fig. 4. Variation of inverter current with input voltage.

logic level inverter, but the transient current pulse as shown in Fig. 4 is then the only significant contribution to current drain, as one or other of the transistors is non-conducting in each of the logic states. (At high pulse rates power consumption is associated with the multiple charge/discharge of internal and load capacitances.)

For analogue systems this central region of the characteristic is of great interest. The slope is moderately high, corresponding to a voltage gain of the order −10 to −100 with the unusual property that the gain is greater at lower values of supply voltage (both transconductance and output conductance fall, the last-mentioned more rapidly than the first).

Although not designed for high d.c. stability, temperature dependence of the transfer function is small. Recently c.m.o.s. i.cs have been produced designed specifically for analogue applications; though the configurations may be identical to particular logic circuits, the processing is optimized for linear operation.

Because each m.o.s. transistor can be used as a voltage-controlled resistor, packages containing several devices offer interesting possibilities. The drain-source resistance characteristic remains approximately linear for small values of reverse voltage and current, making a.c. operation feasible. The devices on a common chip will be similar and will be subject to the same temperature variations. Thus, operated from a common gate-source voltage supply, they offer closely-matched resistance characteristics for use in amplifiers etc.

An interesting extension of this technique is possible even where single devices are not accessible separately. By grounding the positive supply line of a package containing multiple inverters, the p-channel devices are kept out of conduction provided the p.d. applied between output and ground of each device is small. Thus a hex buffer inverter i.c. can be used as a set of six matched n-channel f.e.t.s.

Any inverting amplifier can be used with n.f.b. to give a see-saw amplifier of reduced but well-defined voltage gain. As only a single gain-stage is involved external compensation against high-frequency stability is not required even with 100% negative feedback. The bandwidth is not particularly high though well above the audio-frequency range, with some gain to beyond 1MHz. High values of resistors may be used without loading effects due to amplifier input impedance, though the resulting RC time constants due to strays can further reduce the bandwidth.

A recent example of the way in which device technologies change forces a warning note at this point. To improve the performance of gates/inverters for their main functions in purely digital applications, some manufacturers produce "fully-buffered" versions. These might contain three inverters in cascade to perform the function previously using a single inverter. The improved response is welcome to users with critical requirements in the digital field; those wishing to adapt them for analogue circuits, as decribed in Circards Set 27, would find high-frequency instability resulting from the much-increased loop gain and multiple phase-shifts. Remember to check the characteristics of any device or circuit rather than assume that similar titles guarantee identical performance.

If logic circuits could be adapted only for amplifying functions, the exercise would still be worthwhile — it would avoid having to add separate operational amplifiers on those occasions when only simple signal processing is needed. In fact most other electronic circuits can be designed if care is taken to work with the characteristics of c.m.o.s. rather against them. A restriction is that only inverting stages can be used with negative feedback, there being no equivalent to the series-applied feedback circuits (e.g. voltage followers) common in operational amplifier designs. Non-inverting buffers or cascaded inverters lend themselves to positive feedback functions such as Schmitt trigger circuits. Variety can be introduced by using individual devices from certain c.m.o.s. i.cs in combination with inverters and gates.

As a general rule it is simpler to adapt those familiar circuits that use inverting amplifiers, unless the function required cannot be performed in this way.

Circuits that can be designed using inverting amplifiers include active filters such as the two-integrator loop, three-stage phase-shift oscillators, and the like. There is no need to restrict ourselves to simple buffers and inverters; other i.cs can be readily applied in analogue circuits of various kinds. For the more complex i.cs, the degree of internal interconnection reduces flexibility and it is less easy to see ways in which non-logic functions can be performed.

One form of flip-flop, the D-type, has a pair of outputs Q and $\overline{Q}$. When fed with a positive-going pulse on the clock input C, the output Q is forced to take up the logic state on the data input D at the instant of clocking. This state at the output is retained regardless of any variation at D until the next clock pulse. Such a flip-flop finds application in the processing of analogue signals, as in some forms of analogue to digital converters and phase-locked loops. In a particular application, the delta-sigma modulator, the integrator receives a current from the input voltage, which causes its output to change until the comparator output swings through zero. On the succeeding clock pulse the Q-output must change, since the D value has changed, and this changes the f.e.t. between its conducting and non-conducting states. The polarity of input and reference voltage must be opposite so that the fed-back reference can reverse the direction of integration. Combining the clock pulse with Q (or $\overline{Q}$) in a suitable logic gate gives a pulse train in which the average number of pulses is proportional to input voltage.

The above appears to be a complex system, but two properties of c.m.o.s. allow efficient use of the flip-flop. The sharpness of the transfer-function means that the region of doubt at the D input is very small i.e. that even voltages close to $V_s/2$ are clearly distinguished as either logic 0 or logic 1. Hence the comparator can be dispensed with, the flip-flop acting as its own comparator. Similarly the output of the flip-flop is well-defined, and for a stable supply voltage the f.e.t. and separate voltage reference can also be eliminated reducing the system to one op-amp and a flip-flop.

Similar considerations lead to economical circuits for Schmitt trigger, astable and monostable circuits, by making use of the S and R or set and reset inputs, also available in D-type flip-flops. It must be remembered that such circuits may depend on properties which may not be covered directly by manufacturer's data, although the experimental evidence for their satisfactory behaviour is clear.

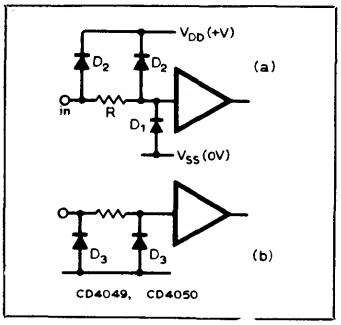
A semi-digital mode of operation is where inverters are used to drive power transistors. Output stages for class-D power amplifiers are examples where this technique is of use, the c.m.o.s. drivers also helping to switch the transistors off rapidly, though delays may be needed at the inverter inputs to avoid the possibility of simultaneous conduction of both transistors.

There is one family of c.m.o.s. circuits designed specifically for use in linear and non-linear analogue circuits viz the analogue gate/bilateral switch. By driving a parallel complementary pair of m.o.s. transistors with anti-phase logic level signals their conduction can be linearized so that the transfer of voltage is near unity when lightly loaded. This extends over the whole supply range and these gates can be used to switch components in and out of circuit as well as for direct gating of signals. Applications include d. to a. conversion, waveform synthesis and switched filters.

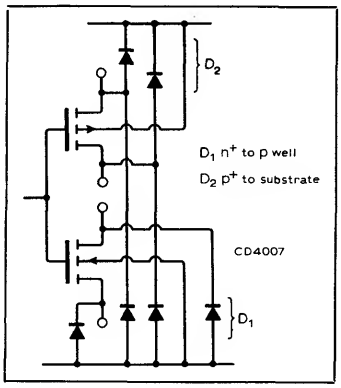
The technology developed for logic applications in c.m.o.s. has proved to have many characteristics that can be pressed into the service of linear circuit designers. The very low cost of these i.cs must commend them, and with care their limitations can be overcome or side-stepped in a wide variety of applications.

wireless world circard

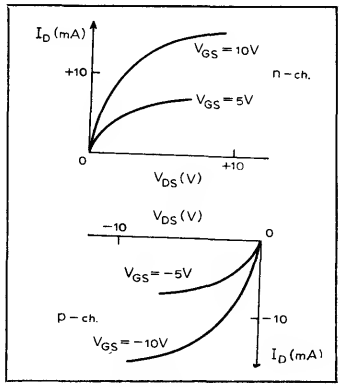
Devices and characteristics



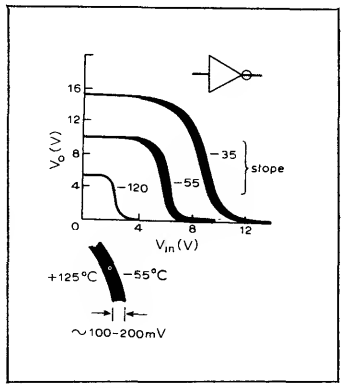
Input protection
A network of diodes at the input of each gate/inverter protects against transients. In linear applications they limit the range of input voltages that can be applied, in particular when the designer seeks access to individual devices, using a non-standard supply voltage to disable unwanted devices. Most packages conform to Fig. 1(a)—certain buffers to Fig. 1(b).



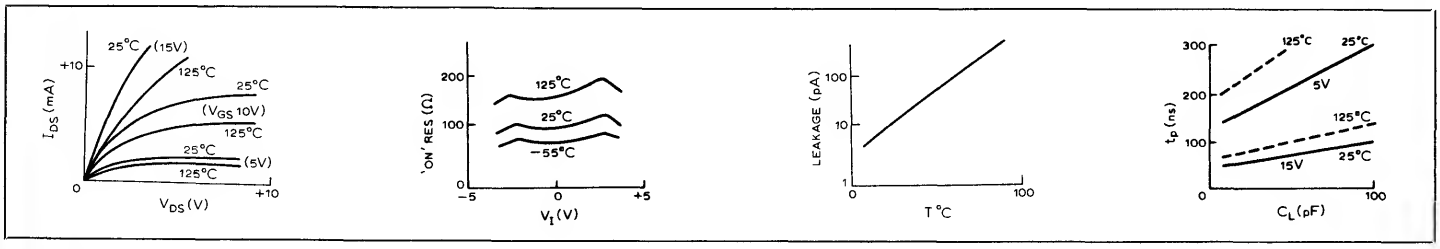
Output diodes
The processing steps needed to produce complementary devices leave a number of p-n junctions between source and drain and the supply terminals. In most devices the sources are already directly connected, but the junctions become apparent in certain i.cs with access to individual devices.



Device characteristics
Each device has a current that is a function of both gate and drain potentials. Above a critical voltage on the drain, which varies with V_{GS}, the drain current becomes largely constant i.e. the slope resistance is large and the device is in a constant-current mode, and said to be saturated. Below this voltage the output resistance is lower, non-linear and is varied by the gate-source voltage.



Transfer function
The output voltage changes sharply with input voltage at a particular input that is remarkably stable against temperature, has a broad tolerance from device to device but is at a roughly fixed percentage of supply for a given device.



Device temperature drift
The drift in characteristics for individual f.e.ts, is much larger than for a complete inverter, verifying the matching characteristics of p-channel and n-channel devices. The resistance increases by about 0.3%/degC. The current for any combination of V_{DS} and V_{GS} falls by around 30% for the temperature range indicated. The current depends on a square-law relationship involving V_{GS} and V_{DS}, except in saturation when V_{DS} has little further effect.

Analogue gate : on-resistance
One class of c.m.o.s. i.cs uses complementary pairs in parallel with the gates driven in antiphase, so that either they are conducting or non-conducting simultaneously. The result is an analogue gate or switch with a very high off-resistance and a low but non-linear on-resistance. Again the resistance is temperature dependent, with a comparable temperature coefficient (caused by the same change in mobility of the current carriers). The pattern repeats itself at all voltages and currents.

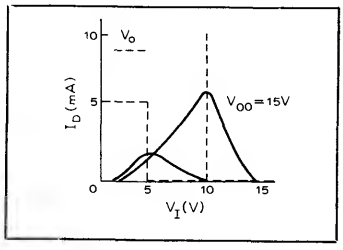
Gate input leakage
The input resistance of a f.e.t. is exceedingly high—in practice swamped by external leakage effects due to package pins or p.c. boards. The protective diodes at the input of c.m.o.s. circuits, provide leakage paths which leave the input current either positive or negative depending on the input voltage. Though still very small the current varies exponentially with temperature. A leakage current of 10pA at room temperature could increase a hundredfold at the device maximum temperature. It is generally safe to assume an input resistance in excess of 10MΩ.

Propagation delay
The self-capacitance of a device is a function of its geometry, and is not affected by temperature changes. The increase in resistance increases all the time-constants and, for example, the propagation delay increases at about 0.3%/degC. Similar figures apply to most pulse characteristics, the speed at higher voltages being markedly improved. This is because the sharp fall in resistance allows the larger voltage swing to be achieved in a much shorter time. For linear operation, the bandwidth is much increased at higher voltages, and somewhat decreased at higher temperatures.

wireless world circard

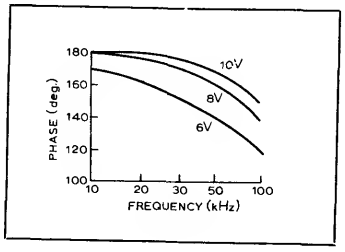
Set 27: C.m.o.s.—2

Linear circuit characteristics

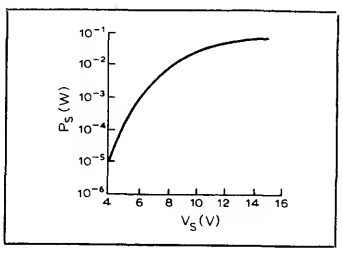


Current variations
When the input voltage to an inverter is varied, it is no longer true that the current remains at zero as in logic applications. For $V_I \approx V_{DD}/2$ the inverter output is in its linear region, both devices are forward-biased and the current rises to a maximum. At high supply voltages the current can be >20mA for high-current buffers. At low supply voltages the current is so low that the operation approximates to class B.

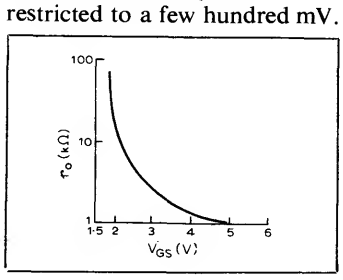
Phase/frequency variation
The change in characteristics with supply, extends to the phase shift at high frequencies. In a multi-stage amplifier this could bring the frequency at which instability might occur to below 100kHz (60° phase lag per stage at 6V supply would give a total phase shift of 180° in a three stage feedback amplifier). This together with the drastically increased output resistance makes it difficult to design linear amplifiers at supply voltages of 5V and below.

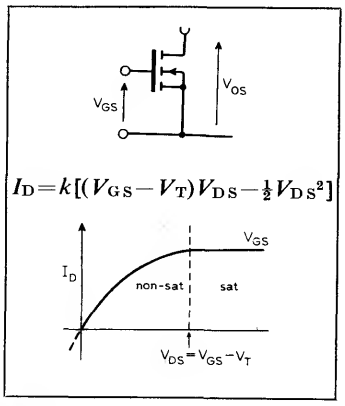


Power dissipation
As an example a NOR gate was biased for $V_O = V_I$ and the supply voltage varied from 4 to 15V. At the low end the current fell to 2μA with a dissipation below 10μW. At the supply maximum the dissipation approached 100mW—the limit suggested for any single gate or buffer with a package limit of 200mW. Thus it would not be safe to operate all four gates in the linear mode at the otherwise safe supply voltage of 15V.



Output resistance
The slope-resistance of a m.o.s.f.e.t. is moderately linear close to the origin, and can be varied over a very wide range. At high values of V_{GS} the resistance can fall well below 1kΩ. As V_{GS} approaches the threshold voltage, the device is cut off and the slope resistance tends to infinity. In practice a controlled resistance of order 100kΩ is possible. In all cases the polarity of V_{DS} may be reversed, and the V/I characteristic is continuous though the voltage swing for reasonable linearity is restricted to a few hundred mV.





Basic device equations
The equation gives the drain current as a function of the p.ds between gate and source, and drain and source in the unsaturated region. As V_{DS} is increased to the point where $V_{DS} = V_{GS} - V_T$ (*) the current becomes substantially constant. Alternatively when V_{GD} exceeds the threshold V_T, the channel is pinched-off to an extent that inhibits any further increase. Both regions of operation are of interest for different applications.

Below saturation
Both drain and gate potentials have an effect, but if V_{DS} is small then the equation approximates to a linear one—it extends below the origin but there is an additional constraint imposed by protective diodes.
$I_D \approx k(V_{GS} - V_T)V_{DS}$
Thus the slope resistance at low voltages becomes
$dV_{DS}/dI_D \approx 1/k(V_{GS} - V_T)$
This is a voltage-controlled resistance though it is neither a linear resistor nor a linear function of the controlling voltage. The departure from linearity is small enough for $V_{DS} < 100$mV to use the resistor in feedback networks etc to control gain, but distortion prevents its use at higher voltages than a few hundred millivolts.

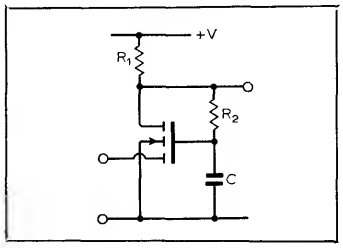
Above saturation
The current is assumed to be constant at the value it has for the condition given by *.
Hence $I_D = k(V_{GS} - V_T)^2/2$
This is a square-law function requiring the elimination of V_T by some compensating circuit if a square law relationship is to be obtained between input and output voltages.
Transconductance can be obtained by differentiating I_D with respect to V_{GS}
$g_m = dI_D/dV_{GS} = k(V_{GS} - V_T)$
i.e. $g_m \propto \sqrt{I_D}$. As the drain current is increased by increasing the forward bias on the gate, the g_m increases, but more slowly than the fall in load resistance that would be needed in a resistively loaded stage to allow that current to flow. Since the voltage gain depends on the product of g_m and R_L, higher voltage gains can be obtained by operating at the smallest possible current, increasing R_L accordingly. This information does not apply directly to c.m.o.s. inverters where the load of one m.o.s. device is the output of the other; it indicates a different pattern for f.e.ts from that familiar in bipolar designs where comparable voltage gains are available at all current levels.

Assuming that the device is operated with the lowest possible V_{DS} to maximize R_L i.e. just at pinch-off, voltage gain becomes
$-2[(V_{DD} - V_{GS} + V_T)/(V_{GS} - V_T)]$
This is the maximum possible voltage gain for a m.o.s.f.e.t. with threshold voltage V_T operated with a gate-source voltage V_{GS} and with a supply voltage V_{DD}. In practice the voltage gain will be smaller in magnitude because of finite output resistance etc.
N.B. The basic form of these equations applies to all m.o.s.f.e.ts; the coefficients of practical devices differ from those given and account has to be taken of this—see card 7.

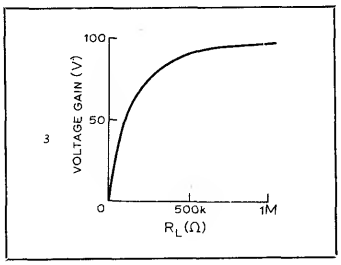
Further reading
Motorola, McMOS Handbook, 2nd edition 1974, pp. 1-7 to 1-18 and 3-1 to 3-7.
Santoni, A. & Trolese, G. Design ideas with COS/MOS, *New Electronics*, April 30, 1974, pp. 27-34.

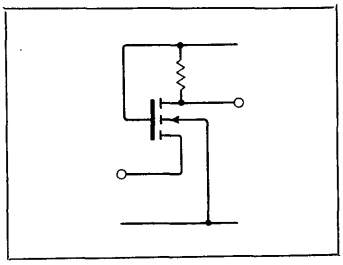
wireless world circard

Device configurations



Typical performance
IC CD4007AE
n-channel device
Supply +10V
R_1 100kΩ
R_2 10MΩ
C 100nF
Voltage gain +50



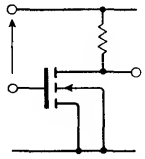


Circuit description
In certain c.m.o.s. i.cs, access may be gained to the sources/drains of individual f.e.ts (CD4007, CD3600 and similar). Where this is so, circuits may be constructed that are the counterparts of the more familiar common-base common-collector etc. Consider the common-gate amplifier shown above. The gate is grounded for a.c. purposes by the capacitor. The gate current is negligible and the p.d. across R_2 may be assumed to be zero. The d.c. operating conditions for the amplifier are thus $V_{GD}=0$ and R_1 defines the direct current flow. The alternating voltage gain depends on the parallel value of R_1, R_2. The input impedance is low, and to a good approximation is $1/g_m$ where g_m is the transconductance of the device as usually defined. This varies with the operating current being proportional to $\sqrt{I_D}$. Since $I_D \propto 1/R_1$ if the p.d. across R_1 is constant (a reasonable approximation when the supply voltage is well above the device threshold voltage) then the voltage gain ($\approx g_m R_1$) is proportional to $\sqrt{R_1}$. The approximation is not valid at very low currents and the voltage gain is limited to about +100. The voltage gain for a given value of R_1 is roughly proportional to the square root of the supply voltage by the same reasoning, falling more rapidly as this approaches the threshold values. The amplifier has a high non-inverting voltage gain, a low input-impedance and a high output-impedance.

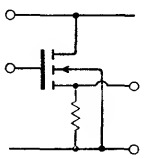
Component changes
IC: must be package with separate access to drain. Any discrete m.o.s. device (enhancement mode can be used in these circuits—the aim here being to indicate where c.m.o.s. packages can be adapted to provide functions that would otherwise require separate discrete components).
Supply: +5 to +15V.
Some gain available at lower supply voltages.
R_1: sets the quiescent levels and the output impedance. Can be replaced by current source for increased voltage gain.
10k to 1MΩ.
R_2, C: provide decoupling and the time-constant must be long compared with period of lowest frequency. R_2 1M to 22MΩ.

Circuit modifications
- The gate can be connected directly to the positive supply, which reduces the component count, but removes the stabilizing action of the d.c. negative feedback. Otherwise, the a.c. properties are comparable.
- Each of the other device configurations is possible, the common-source version simply disregarding the presence of the p-channel device by ensuring that its source and/or drain is open circuit. The voltage gain is comparable to that for the common-gate stage but the input current is now zero, and the output is inverted.
- A common-drain or source-follower configuration can often be provided while using the other transistor of the complementary pair in some other circuit, e.g. astable oscillator. Whatever waveform appears at the common gate is transferred to the source with some attenuation but without loading the waveform. Since source and drain currents are equal an antiphase output can be obtained at the drain.
A novel arrangement joins the gate to the drain for 100% negative feedback. The device is now apparently a two-terminal device and might be expected to behave as a non-linear resistor. In fact it acts as a non-inverting voltage amplifier with a low voltage gain. This is because the substrate connection acts as a subsidiary gate and the operation is that of a grounded-gate amplifier with the gain much reduced by the feedback to the main gate.
Any of the multi-transistor circuits can be implemented using several devices from a package and the example illustrated is the cascode circuit useful for high voltage gains where input-output isolation is important.

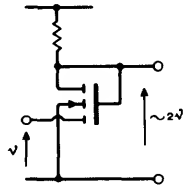
Cross references
Set 27, card 2.
Set 20, card 8.



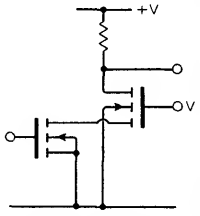
common source



common drain

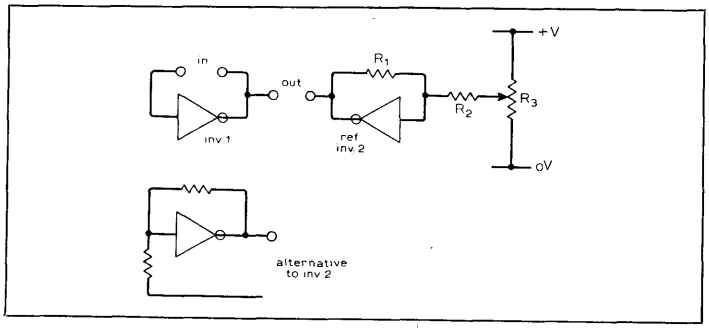


two-terminal amplifier

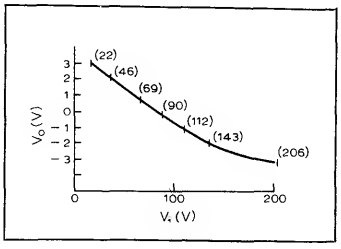


cascade amplifier

D C amplifiers



Typical performance
IC CD4001AE NOR gates with 2 inputs active
Supply +10V
R_1 27kΩ
R_2 1MΩ
R_3 100kΩ



Circuit description
C.m.o.s. inverters are not suited to the amplification of small d.c. voltages. They have a threshold voltage range below and above which the output is saturated. The simplest way of biasing an inverter/gate into its linear region is via direct or resistive feedback from output to input. This ensures $V_{out} = V_{in}$ which is near the middle of its linear region, the voltage gain lying between −10 and −100. Although there is a measure of matching between devices on the same chip, the tolerances are much relaxed for digital circuits. The output voltage under these conditions may have a total spread of up to 40%, with the difference between gates from a given chip reduced to the order of 100mV. This allows the use of a pair of gates, one as the amplifier and the other to act as an artificial ground point. The offset voltage can be ruled out by injecting a portion of the supply via R_3 and R_2 as shown, while the offset itself has a relatively small temperature dependence. There remains one major advantage of these devices as d.c. amplifiers, viz their very high input impedance. If feedback is to be used to define the voltage gain while exploiting this high input impedance as fully as possible, the source can be connected between the input and output of the inverter. For a voltage gain of −100, 99% of the source voltage appears at the output terminal and 1% at the input i.e. the accuracy with which an input signal is transmitted to the load can be well within the tolerance of moving-coil meters. The current drawn from the source is not specified in the data sheets as these devices are intended for digital functions, but is basically due to the minute leakage currents of the reverse biased protective diodes. With some sample gates, the output changed by <1% for a change in source resistance of 4.7MΩ. The configuration is clearly restricted to a floating source (high impedance transducer such as piezo-electric devices) or would require a floating power supply. The second inverter compensates for most of the quiescent output by its matched characteristics, the remainder being cancelled by injecting a variable current via R_2, R_3.

Component changes
● The only changes in the resistors are to vary this offset compensation. The values are not critical, but $R_2 \gg R_3$ and R_1/R_2 = offset voltage/supply voltage, indicate the values.

The inverters can be buffers, NOR and NAND gates or the inverters constructed from CD4007 or CD3600 packages. None of these compete in performance with op-amps constructed from the appropriate m.o.s. and bipolar transistors. They are intended only to extend the applications of inverters/gates to simple d.c. applications where the signal voltages are large enough that significant offset can be tolerated.

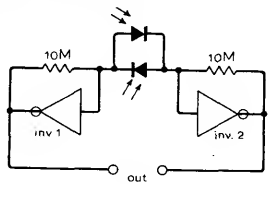
Circuit modifications
● A possible application is in the amplification of small currents from photo-diodes used in their photo-voltaic mode. For matched diodes exposed to different light intensities, there will be a current of given polarity representing the difference between the light intensities. This will drive the outputs of the inverters in anti-phase, and currents well into the sub-microampere range could be detected. $V_0 \approx 20M\Omega \times I_{diff}$. The inverter can be used in the see-saw mode with resistor values of megohms if required.

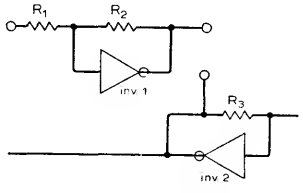
The voltage gain can be set to between −1 and −10 with good accuracy, with a second inverter to provide an artificial ground point. Both input and output voltages are then referred to this point. For constant supply voltages, the inverter can also be used as a comparator since its input threshold voltage varies little with temperature (<1mV K^{-1} for some gates i.e. <0.01% of the supply voltage at V_s = 10V). A zener diode placed in the feedback has a current forced in it of $\approx V_s/2R_1$ and the gate output voltage is raised by V_z over its normal threshold. This can be used to define the compensation current fed into other stages used as d.c. amplifiers etc.

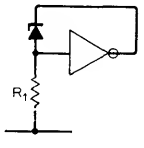
Further reading
McMOS Handbook, Motorola 2nd edition 1974, p. 8-15.

Cross references
Set 27, card 1.
Set 11, cards 5, 6.
Set 20, card 8.
Set 9, card 11.

Circuit modifications

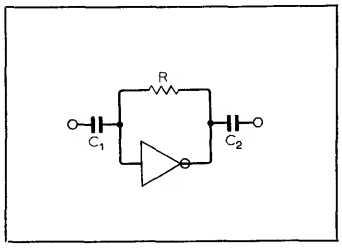


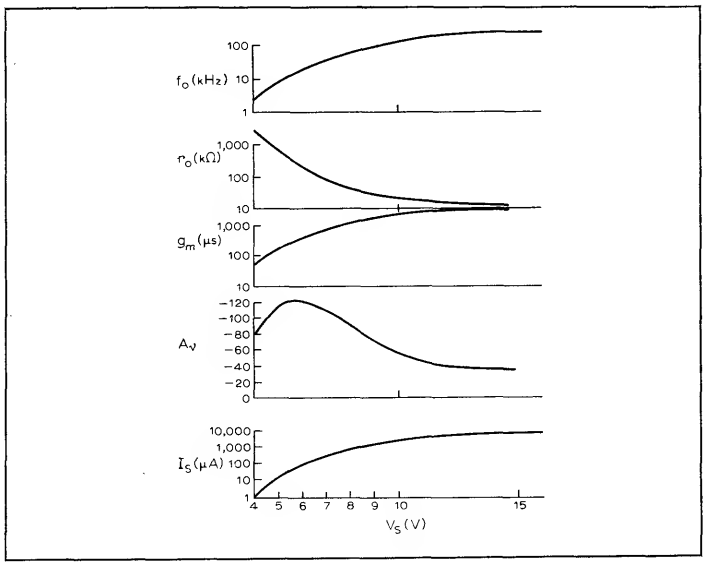




A C amplifiers

Typical performance
IC ¼×CD7001AE
Supply +10V
Quiescent current 1.9mA
Output resistance 25kΩ
Voltage gain −53
Transconductance 2.1mS
Upper cut-off frequency 130kHz
R 6.8MΩ
C_1, C_2 100nF



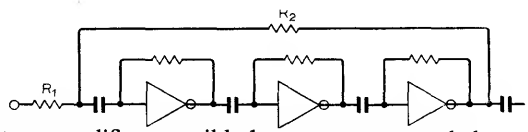


Circuit description
The basic open-loop behaviour of an amplifier can be predicted from its internal structure fairly readily in cases as simple as a c.m.o.s. inverter. For the resistive feedback bias as shown, the input and output potentials are equal. Hence each device operates with equal gate and drain potentials. This introduces opposing effects on the voltage gain as the supply voltage increases. First the increase in operating current which is very marked leads to an increase in the transconductance (g_m). At the same time the output resistance is markedly reduced because each device is operated on or below the knee of its output characteristic. The net effect is that the overall voltage gain is relatively constant varying by only 10dB over a 1,000:1 range in currents. The measurements were all made with a probe having an input resistance of 10MΩ and with a total input capacitance and strays of about 18pF. The high voltage gain at the lower supply voltages is hard to make use of, since even the high feedback resistance contributes to the loading effect. The increase in cut-off frequency as the current rises, can be explained if we assume a total output capacitance which is constant. If the output resistance is r_o, the cut-off frequency f_o and the shunt capacitance C, then $f_0 = 1/2\pi R_0 C$ would be the appropriate relationship if the transconductance is assumed to contribute nothing to the frequency dependence. This implies $f_0 R_0$ should be a constant. Comparison of the data shows a variation of around 2:1 over a 1000:1 range of currents. On these figures, the output capacitance would be around 20pF.

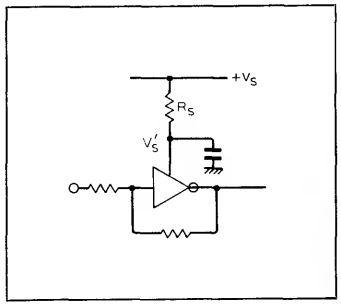
Circuit modifications
- Multi-stage amplifiers are possible, but since c.m.o.s. stages give sufficient gain/accuracy for routine functions, the additional complexity of the compensation networks would appear to be a bad bargain. With d.c. coupling, the low-frequency time constants are eliminated and over-all feedback can hold all three stages within their linear range.
- An inverter can be operated at low current from a high-voltage supply by adding a series resistor in the supply line and decoupling the inverter supply pin. N.B. The supply rejection ratio is only 6dB since the output of a device with feedback biasing is always of order $V_s/2$. If the series resistor is chosen so that the quiescent current is only a few microamperes, the devices must settle at V_{GS} values close to the device thresholds. This sets the effective supply voltage V_s to about the sum of the threshold voltages i.e. 3.6V.
- In devices with access to the sources (CD4007, CD3600 etc) resistors may be added as shown to define and reduce the g_m values while increasing the output impedance.

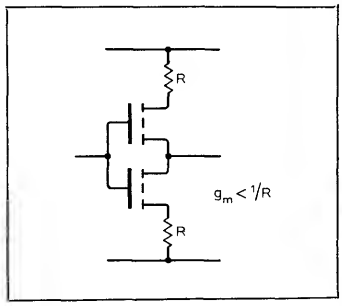
Further reading
McMOS Handbook, Motorola pp. 8.3-8.15, 3.13-3.18, 2nd Edition, 1974.
Fitchen, F. C. and Ellerbruch, V. G., Linear operation of the m.o.s.f.e.t. complementary pair, *IEEE J. Solid State Circuits*, SC-6, 1971, Dec. pp. 422-423.
Santoni, A. & Trolese, G. Design ideas with COS/MOS, *New Electronics*, April 30, 1974, pp. 27-34.

Cross references
Set 27, cards 1, 4, 6.
Set 27, cards 4, 6, 8.
Set 12, card 1.

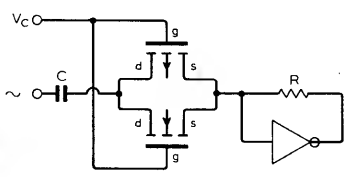


Multistage amplifier: possible but not recommended as accumulated phase shifts make it difficult to apply sufficient feedback without oscillation and input stage noise can saturate the output stage.



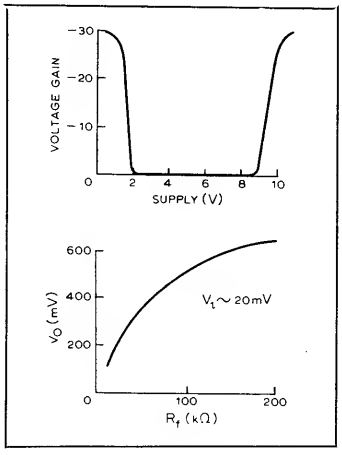


Gain-controlled amplifiers

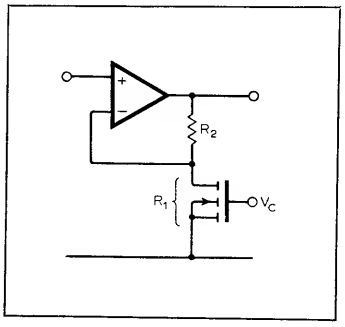


Typical performance
IC 2/3×CD4007
Supply 10V
R 220kΩ
C 1μF
Control V_c 0 to 10V voltage

Circuit description
A more familiar method of using a m.o.s.f.e.t. as part of a gain-controlled amplifier is to use it as the lower section of a potential-divider in either the forward or feedback paths of an amplifier. This allows the m.o.s.f.e.t. to operate with source grounded and makes it easier to apply a control voltage to the gate. If the source is connected to any other point at a constant potential then a control signal may be applied, but it must be sufficient to take V_{GS} above its threshold value V_T. In the circuit shown, either or both of a complementary pair can be used with gates, sources and drains commoned, provided these are not already grounded internally. If the control voltage V_c is in the mid-range of the supply there is insufficient V_{GS} to bring either device into conduction and the voltage gain→0. When the control voltage is very low, the p-channel device is brought into its conducting state and the gain sharply increases. For $V_c \rightarrow V$, the n-channel device has a low slope resistance and the gain increases. The graph shows that either characteristic can give a voltage gain which can be controlled from zero up to −30. At the low values of gain the control action is rather sharp. The amplifier is another c.m.o.s. pair used as an inverter with R providing shunt feedback defining the input potential by the virtual earth action.

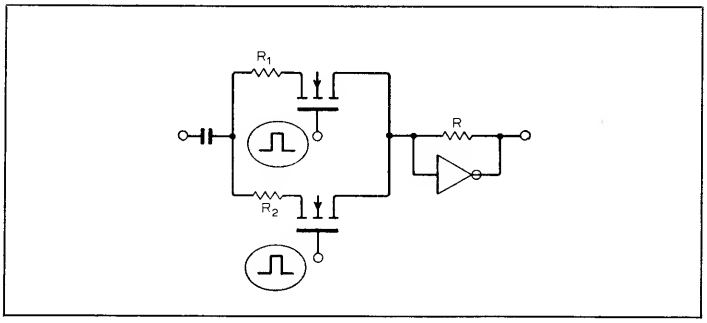


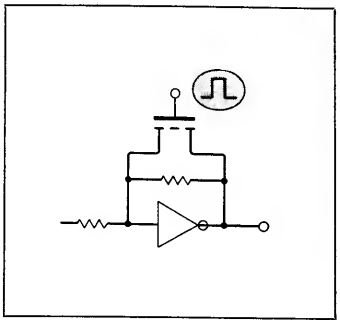
Component changes
IC: Any single m.o.s.f.e.t. either p- or n-channel may be used.
Supply voltage: since each f.e.t. receives a gate-source voltage which is $< V/2$ the supply voltage has to be $> 8V$ in this circuit.
R_f: 10k to 1MΩ
C: not critical. Determines l.f. response. 0.1 to 10μF.



Circuit modifications
- A conventional op-amp circuit can be used as a virtual earth amplifier with the f.e.t. in the forward or reverse paths. Because the f.e.t. has a variable resistance, this complicates the design of the system unless the source has a very low internal resistance By placing the f.e.t. in the series feedback path, the loading affects the output of the amplifier which can tolerate it.
- If two or more f.e.ts are placed in parallel paths they may be gated on or off. This offers a simple alternative to a separate analogue gate i.c. if the performance requirements are not too critical. Both the gates and the inverting amplifier can be derived from a single low cost CD4007 or similar. If the gates of the m.o.s.f.e.ts are paralleled the gain is switched between $-R/R_1$ and $-R/R_2$ provided the on-resistances are low compared with R_1, R_2. It is suitable for gains in the region −1 to −25.
- The f.e.t. can also be placed across the feedback path provided the voltage swing is small enough to prevent non-linearity from producing excessive distortion. One or more devices can be used across both input and feedback paths. Non-linear elements or reactive components can also be placed in series with the f.e.ts. The on-resistance is high compared with devices designed specially as analogue gates.

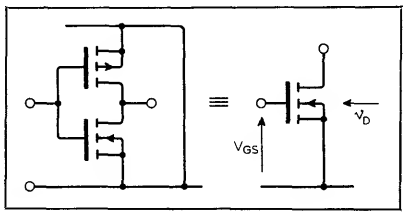
Cross references
Set 27, cards 1, 5, 7.
Set 20, card 8.
Set 21, card 4.
Set 22, card 7.
Set 16, card 10.



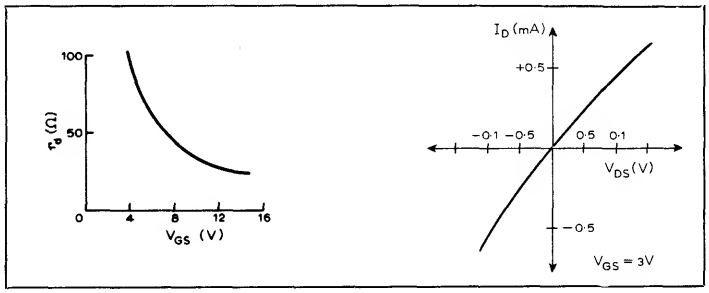


wireless world circard

Controlled resistances



Typical performance
IC CD4049
V_D 50Ω at V_{GS} of 7V for n-channel device



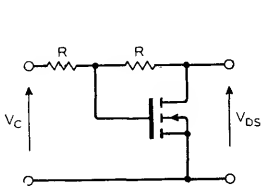
Circuit description
Some i.cs contain multiple inverters e.g. CD4049 hex buffer. Consideration of their internal structure shows that if the V_{DD} line is shorted to the V_{SS} and then used as the common line, then a positive control voltage on any input varies the slope resistance of that output as if it were a single n-channel f.e.t. If the p.d. across the drain source path is less than 0.5V the internal diodes are not brought into conduction. Hence the package is equivalent to six independent well-matched n-channel enhancement mode f.e.ts. These can be used separately or in combinations in any circuits where voltage-controlled resistors are required. The slope resistance at the origin is controllable over a 10:1 range though the resistance becomes non-linear at a progressively lower drain-source voltage as the gate voltage approaches the threshold value. The non-linearity is indicated for V_{GS} of 3V. The devices match to within 5% with the samples tried but this is not covered by the package specifications since these were designed for digital applications. The resistance is non-linear. As the forward voltage drop across the drain-source path is increased, the value of V_{GD} is reduced, this reduces the forward bias and decreases the channel conductivity. Conversely, a negative current in the drain increases V_{GD} and increases the channel conductivity. When V_{GS} is large the contribution due to the small values of V_{DS} (0 to 200mV) is negligible and the on-resistance can be assumed linear for most applications. The example shown represents the lower limit of V_{GS} at which use as a controlled resistance might be acceptable. The non-linearity is predictable from the basic device equation (Set 27, card 2) $I_D=k[(V_{GS}-V_T)V_{DS}-nV_{DS}^2]$ This theoretical equation represents a wide variety of devices over a range of currents and voltages, and it is common to assume $n=\frac{1}{2}$. Where this is true it leads to a particularly simple technique for removing the non-linearity from the on-resistance.

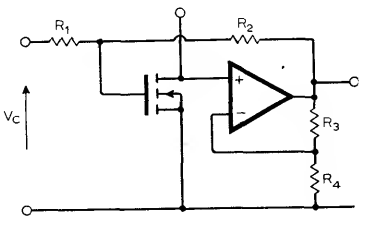
Circuit modifications
- Assume equation to be valid for $n=\frac{1}{2}$. If $V_{GS}=(V_C+V_{DS})/2$ achieved by using equal value resistors as shown, then substituting into the first equation gives $I_D=k[(V_C/2+V_{DS}/2-V_T)V_{DS}-\frac{1}{2}V_{DS}^2]=k(V_C/2-V_T)V_{DS}$ i.e. V_{DS} is a linear function of I_D for all values of I_D within the device limits, but the slope is controlled by the direct voltage V_C. The resistors attenuate the control action and V_C has to have twice the value it had in the simple circuit overleaf. Tests with devices from c.m.o.s. packages suggest that in this application considerably more feedback is needed to linearize the characteristic, though some improvement is offered. To test the principle the drain-source voltage has to be amplified before deriving the feedback.
- If the gain is made > minimum required to achieve compensation (e.g. $R_3=9R_4$ giving a gain of +10) then compensation is achieved with $R_1 \ll R_4$ i.e. the control voltage reaches the gate with little attenuation. With $R_2=7R_1$ and the above ratio for R_3/R_4 the on-resistance of a CD4049 n-channel device was controllable from 25 to 200Ω with characteristics matched in the positive and negative quadrants to better than 0.5% and a non-linearity of less than 1.5% (less than 0.5% up to 100Ω). The range of control voltages required was from 3.4V (200Ω) to 16.5V (25Ω). These resistor values feed back a portion of V_{DS} to the gate given by $[V_{DS}R_1/(R_1+R_2)][(R_3+R_4)/R_4]=1.25V_{DS}$. This suggests using $n=1.25$ for these devices to determine the necessary compensation. Unless $n<1$ it would seem to be necessary to use an amplifier with each device to obtain accurate linearization.
- An alternative circuit combines the resistive networks to apply a voltage to the gate of $V_C/4+1.25V_{DS}$. Though simpler, this version requires a larger range for V_C.

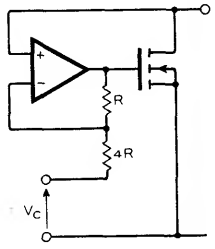
Further reading
Santoni, A. & Trolese, G. Design ideas with COS/MOS, *New Electronics*, April 30, 1974, pp. 27-34.

Cross references
Set 27, cards 1, 6.
Set 22, card 7.

Circuit modifications





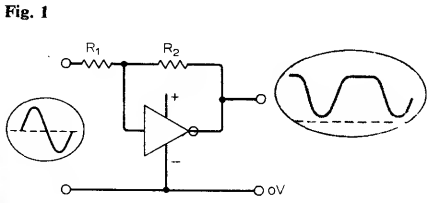


wireless world circard

Set 27: C.m.o.s.—8

Non-linear circuits I

Fig. 1



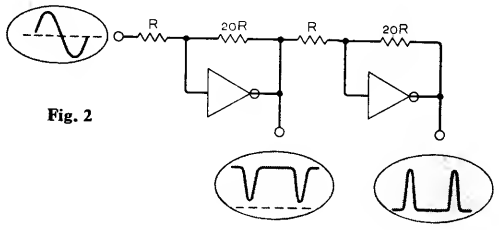


Fig. 2

Circuit description 1
The inverter transfer function is such that the output changes rapidly only when the input is close to a threshold voltage of about 45% to 55% of the supply. If the circuit is fed from ground-referred sine-wave with no d.c. blocking capacitor then the output will be severely distorted in most cases. As an example consider a device with threshold 50% of supply and with $R_1 = R_2$. When the input is at zero, the output must be at +V since there will be equal p.ds across R_1, R_2. For all negative inputs the output holds constant at +V. For all positive inputs the change in the output is equal and opposite i.e. the positive half-cycle of input is reproduced as a negative half-cycle with respect to the positive line. The amplifier gain falls as the swing approaches the supply lines so that perfect half-wave rectification is not possible.

If the circuit is followed by an identical second stage, the output is inverted and approximates to a non-inverted half-wave rectified version of the input. In each case the peak input has to approximately equal the supply for the output to swing through the whole supply range.

Circuit description 2
The resistors are made unequal to give an inverting gain to −10 to −20 depending on the open-loop gain. In this case the output remains at +V until the input approaches very closely to the inverter threshold voltage. It is only the positive peaks of the input signal that cause any change in the output. The output then consists of short-duration negative going swings coinciding with the positive peaks of the input. If a second identical stage follows it, the peaks are further sharpened up and inverted. The result is a highly amplified version of the extreme positive peaks of the input. The threshold voltage of a given device is a well defined fraction of the supply and varies little with temperature. Thus each device would respond to a particular peak input but once adjusted the response could be maintained.

Circuit description 3
If the original waveform is unimportant, negative-feedback need not be used. The input is biased up to the supply rail and the output consists of negative-going pulses coinciding with the positive peaks of the input (the pulse width increases as the input-amplitude increases since the waveform lies above the threshold for a longer fraction of the cycle). If the output is applied directly to a second inverter the output is re-inverted and is sharpened into an almost rectangular pulse equal in height to the supply.

Circuit description 4
The output pulse from such a system can also be sharpened by introducing non-linear elements into the forward or feedback paths. As an example, a pair of parallel-connected back to back diodes limit the output swing to 1V peak to peak since the currents are small. Further, this swing is centred on the threshold voltage which can assist in direct coupling to other stages.

Circuit description 5
A simple frequency-doubler uses a NOR gate together with a peak-selector circuit. If either of the NOR gate inputs goes above its threshold, the output goes to logic 0. This happens on positive peaks of the input via R (which serves to limit any input current for negative inputs). On negative peaks, the input of the inverter is pulled below its threshold and its output goes high. This again drives the NOR gate output to logic 0. Thus there are two negative peaks to the output during one cycle of the input, representing frequency doubling. In principle the circuit could be followed by an active filter to retrieve a sine-wave which would be available for further frequency doubling.

Further reading
Dean, J. A. & Rupley, J. P., Astable and monostable oscillators using RCA COS/MOS digital integrated circuits, RCA app. note ICAN-6267.

Cross references
Set 27, card 9.

Fig. 3

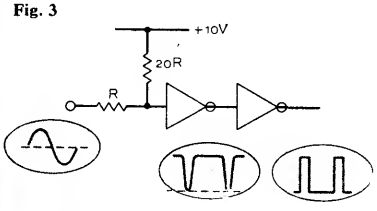


Fig. 4

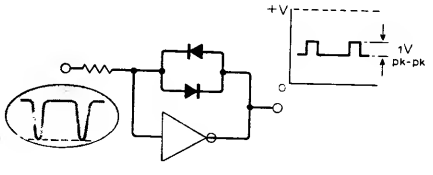
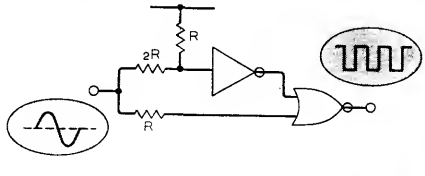
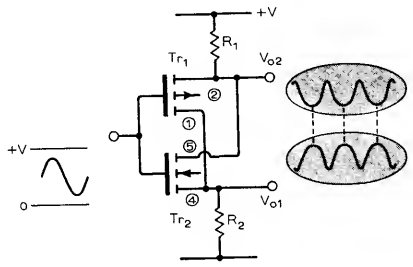


Fig. 5

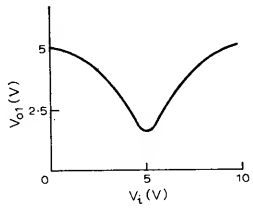


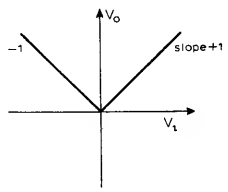
wireless world circard

Non-linear circuits II



Typical data
IC 1/3×CD4007AE
Supply +10V
R_1 10kΩ
R_2 10kΩ
Output ≈ $V/2$ at $V_i=0, V$ and $V/4$ at $V_i=V/2$.





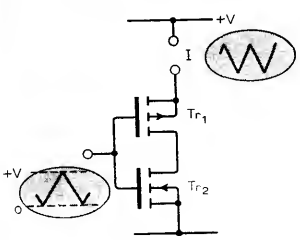
Circuit description
The circuit exploits the non-linear characteristics of c.m.o.s. pairs by cross-coupling sources and drains of a single pair having a common gate. This produces the novel transfer function shown. When the input voltage is high, the p-channel device Tr_1 is non-conducting and the output voltages are determined only by the current in Tr_2. This has resistor R_2 in its source making the transfer function somewhat less than unity but with a linear slope. At all times the currents in R_1, R_2 are equal making the slopes inverse. As the input is low the reverse occurs with Tr_1 conducting, Tr_2 off. If the devices are truly complementary the output voltage would be the same at two values of input voltage, V_i and $V-V_i$. The minimum current and hence the minimum value of V_{01} occurs for $V_i \sim V/2$. If the input is biased to this value and a sine-wave superimposed then the circuit behaves as a full-wave rectifier. This can be seen from the transfer function of an ideal full-wave rectifier in which $V_o = |V_i|$. Any other waveform can be applied, with bias offset if desired to further modify the output waveform. The output for a triangular wave input is a triangular wave of twice the fundamental frequency. In principle the process can be repeated by a.c. coupling into an identical second stage but waveform deterioration limits it to two or three stages at most.

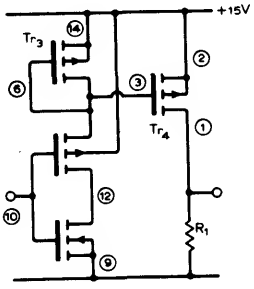
Component changes
For anti-phase outputs $R_1=R_2$. Values not critical and similar shape of transfer function obtained for R_1 1k to 100kΩ. Supply voltage: 5 to 15V. IC: the circuit depends on having access to both sources and drains of a complementary pair and can only be implemented with CD4007 and similar devices.

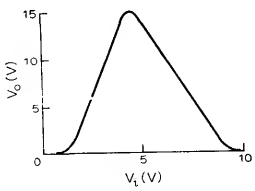
Circuit modifications
- If the current in a c.m.o.s. pair is monitored, it is found to pass through a maximum value at $V_i \approx V/2$ i.e. when both devices are about equally forward biased. At the two extremes $V_i \to 0$, $V_i \to V$ the current falls to zero. This gives a similar non-linear relationship to the previous circuit. To exploit this shape, the current can be fed to a current mirror composed of Tr_3, Tr_4. Output current flowing in R_1 passes through a peak on each excursion of V_i through the supply mid-point (with considerable variation from device to device in the actual values but all with a similar shape of transfer function). The value of R_1 depends on the supply as well as the devices but is typically 1k to 10kΩ.
- A triangular wave input gives a somewhat rounded wave output, there being no negative feedback in this circuit to linearize the transfer function.
- In addition to the above, there are a number of circuits that use the characteristics of the individual m.o.s. devices. By cancelling the threshold voltage, a close approximation to a square-law can be obtained. These will be covered in a later series of Circards.

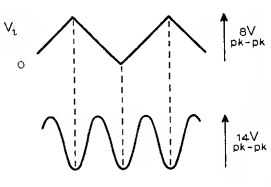
Cross references
Set 27, cards 2, 8.

Circuit modifications



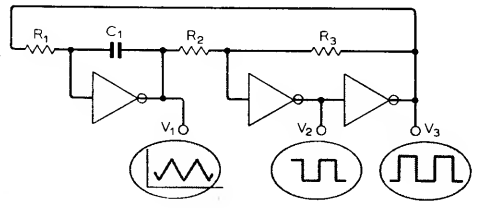




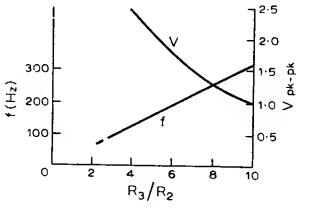


wireless world circard

Square-triangle generator



Typical performance
IC CD4007AE
Supply +10V
R_1 100kΩ
R_2, R_3 50kΩ
C_1 3.3nF



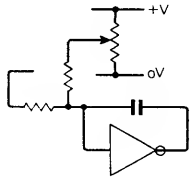
Circuit description
Since a c.m.o.s. inverter has a voltage gain of between −20 and −100 it can be employed for many of the functions usually associated with op-amps. An integrator fed with a constant direct voltage delivers a constant current to the capacitor. The output is then a linear ramp. When the gain of the amplifier is finite, the current changes with output amplitude leading to non-linearity. Even the limited gain of these inverters is sufficient to hold the non-linearity to within one or two per cent. A second limitation, that of finite input current, is not a problem with c.m.o.s. devices and the resistor values are limited only by the effects of stray capacitance on the waveforms. To make a free-running generator the ramp waveform is applied to an amplitude sensing switch—a pair of inverters with overall positive feedback suffices. The output of this switching circuit is a square-wave whose transitions coincide with the peaks of the triangular wave. Because the threshold voltage is not precisely 50% of the supply the positive and negative slopes are unequal as are the on-and-off periods of the square wave. This can be corrected as shown overleaf. There is a second square-wave in antiphase to the main output, while the frequency can be controlled without change in triangular wave amplitude by varying R_1 or C_1. Changing the ratio R_3/R_2 changes the amplitude of the triangular wave as well as the frequency. Since the slope remains the same under this change, the frequency is inverse to the amplitude.

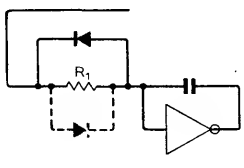
Component changes
IC: any set of three inverters (or a single non-inverting buffer may replace the switch pair if available). NAND or NOR gates may be used with inputs paralleled.
Supply: +5 to +15V. At low voltages the rise in output impedance restricts the resistances to high values.
R_1: 10k to 10MΩ.
R_2, R_3: 10k to 10MΩ.
Triangular wave output should not exceed say 50% of the supply if waveform distortion is to be minimized. Hence $R_3/R_2 > 2$ is required. If the ratio is too large, the triangular wave amplitude may be too small for convenience, and switching transients more troublesome.
C_1: as low as 100pF with high values of resistance but generally 1n to 1μF. Very low-frequency triangular waves possible with this circuit.

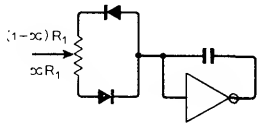
Circuit modifications
- Many op-amp techniques can be adapted to improve or modify the output waveforms. N.B. The triangular wave has a large d.c. content being roughly centred on $V_S/2$. To change the slope a single fixed resistor may be taken from the integrator input to zero or $+V_S$. For controlled compensation, a potentiometer across the supply can be used.
- A good approximation to a sawtooth waveform follows, when R_1 is shunted by a diode. With the cathode driven by the trigger circuit, the output positive ramp is greatly speeded up while the negative ramp remains under the control of R_1. Reversing the diode gives a sharp negative edge followed by a controlled positive ramp.
- Replacing R_1 by a potentiometer and a pair of diodes, the charge and discharge cycles are varied. For equal voltage swings, one part of the cycle is proportional to xR_1 and the next to $(1-x)R_1$. The total period remains broadly constant though there are second-order effects that prevent this from being completely achieved. It gives a variable mark-space ratio to the square-wave with a reasonably constant frequency.
- The triangular wave can be shaped into an approximate sine wave in a number of ways. An amplifier can be added with non-linear elements in the forward or feedback paths. An alternative is to use a second integrator with decoupled d.c. feedback. This converts the ramps into parabolic sections which match a sine-wave reasonably well (as little as 4% t.h.d.).

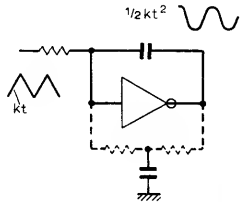
Further reading
Santoni, A. & Trolese, G. Design ideas with COS/MOS, *New Electronics*, April 30, 1974, pp. 27-34.

Circuit modifications









wireless world circard

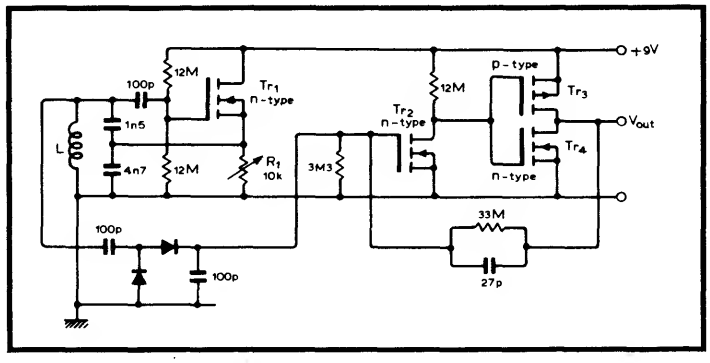
Set 27: Up-date

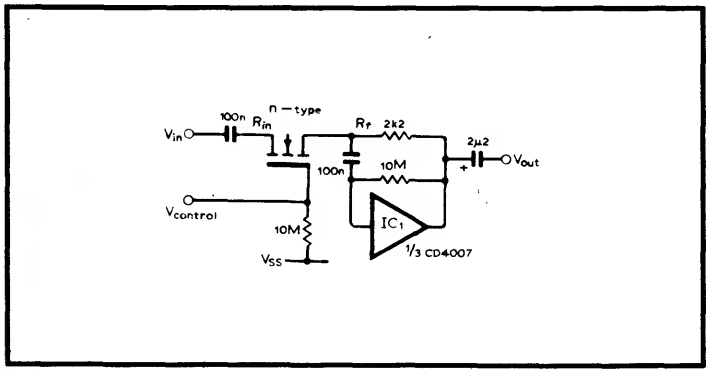
Inductive proximity detector

This employs a CD4007 package to provide an oscillator and Schmitt trigger circuit. The inductor L comprises 150 turns 34 gauge (USA) enamelled wire within half of a Ferroxcube 1811-P LOO-3B7 pot core set, giving around 2mH. The oscillator, operating normally with its high-Q coil at a frequency around 100kHz, drive circuit which maintains transistor Tr_2 on, the input to inverter Tr_3, Tr_4 is low and hence the output high. When a metallic object is close to L, the Q of the coil drops, the oscillator output falls, causing the Schmitt circuit to go off and hence the output rises. Sensitivity is controllable via resistor R_1.

Reference

Fichtenbaum, M. L. *Electronics*, January 22, 1976, p. 112.





This voltage controlled amplifier is derived from a CD4007 package. IC_1 inverter is biased into its linear region by the 10MΩ resistor, and one of the n-type f.e.t. is used as a voltage variable resistor. Control voltage range is dependent on $|V_{DD} - V_{SS}|$. With above network gain is claimed variable from zero to just over unity.

Reference

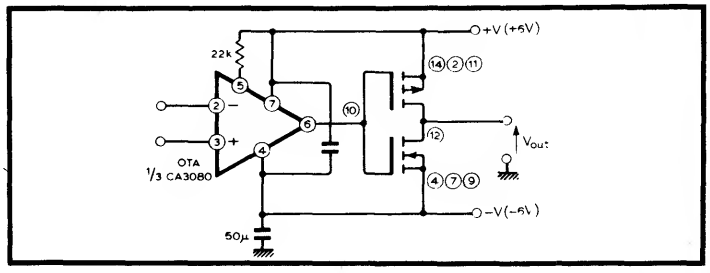
Electronics Today International, October 1976.

CA3600E: This is a m.o.s. transistor-array package configured like the CD4007, but characterized for linear operation.

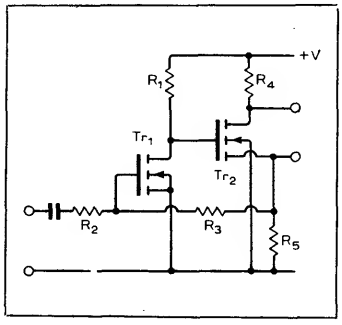
A typical application is a post-amplifier for op-amps, where the high input impedance of an inverter-pair means that the op-amp is buffered from finite loads. This is shown for a CA3080 transconductance amplifier, where the overall gain is 130dB (30dB for the transistor-pair). Each transistor-pair can sink or source 10mA, but for greater current output, the two remaining pairs can be connected in parallel with the output stage.

Reference

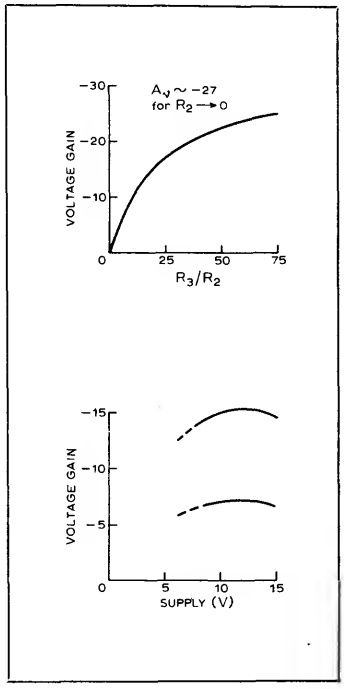
RCA Integrated Circuit Data Book, 1976.



D.C. feedback pair



Typical performance
IC CD4007AE
2 n-channel devices
Supply +10V
R_1 1.2MΩ
R_2 470kΩ
R_3 5.6MΩ
R_4 10kΩ
R_5 4.7kΩ
C 100nF
Voltage gain output 1 −10.7
output 2 −21.8



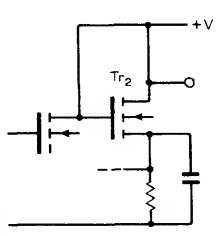
Circuit description
This classic form of circuit has proved so flexible in bipolar designs that it is worthwhile to consider its behaviour in m.o.s. form. It can be constructed using either n-channel or p-channel devices, and complementary forms are also possible. If R_1 is large, the current in Tr_1 is low and it will require a V_{GS} little more than its threshold voltage i.e. around 2V. Input current is negligible and hence the p.d. across R_3 is zero. This defines the p.d. across R_5 and the corresponding current in Tr_2 and R_4. This in turn fixes the V_{GS} of Tr_2 and the drain potential of Tr_1 ($V_{GS1}+V_{GS2}$). Provided the supply voltage is much greater than this value the current in R_1 is well-defined. For a.c. signals the gate of Tr_1 is an imperfect virtual earth—the open-loop voltage gain is around −20 to −40 and so closed-loop gains of −5 to −10 can be defined with moderate accuracy. The input impedance is then $\sim R_2$ and as R_3 and R_2 can be very large, loading of any preceding stage is small. Outputs from source and drain of Tr_2 are anti-phase and can be equal in magnitude or in any desired ratio, since the currents in R_4, R_5 are almost identical (differing only due to the small current in R_3). The frequency response is controlled by shunt capacitance across R_1 (internal plus strays).

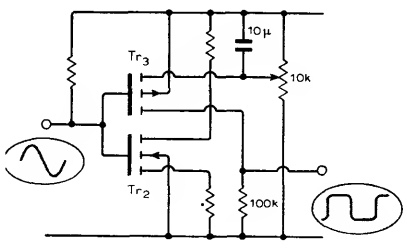
Component changes
IC: Access needed to individual devices—hence CD4007, CD3600 or equivalents.
Supply: +5V to +15V. Gain and output swing fall sharply below 7.5V.
R_4, R_5: 1k to 100kΩ. Compromise between output capability and quiescent current.
R_2, R_3: Ratio sets gain, R_2 defines input impedance. Typically 100k to 10MΩ.
R_1: sets current in Tr_1. If R_1 is too high voltage gain increases but at expense of bandwidth. 10k to 1MΩ.

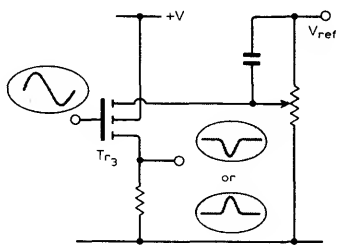
Circuit modifications
- To increase the voltage gain, the source of Tr_2 may be decoupled to ground, removing the a.c. negative feedback. Stray coupling between output and input can cause instability because of the high input impedance. Frequency dependent networks may be used in parallel with or replace resistors in the system to produce a controlled frequency response provided d.c. feedback path remains.
- If the complementary transistor to Tr_2 has its source taken to a decoupled potential divider across the supply, then its output current changes sharply at a particular level of the a.c. signal. Biasing it as shown can produce an approximate square wave without disturbing the normal operation of the amplifier or requiring an extra stage. Because the gate voltage of Tr_2 is defined in potential with respect to the ground line, the squaring action can be made almost independent of supply by deriving the voltage from (or replacing it by a separate stabilized reference voltage). Care is needed to minimize overall feedback when switching stages are operated close to a.c. amplifiers. If the reference voltage is raised or lowered the output transitions occur near to the negative or positive peaks of the input giving pulsed outputs as shown.

Cross references
Set 27, cards 3, 4, 5, 6
Set 20, card 10
Set 12, cards 7, 9

Circuit modifications



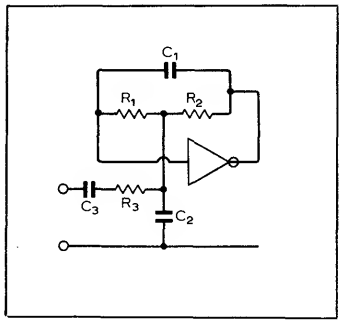




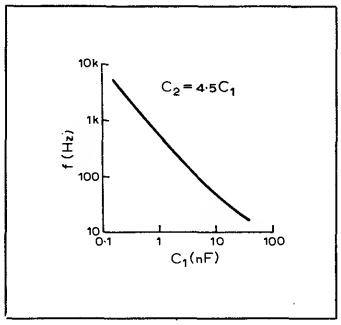
wireless world circard

Set 28: C.M.O.S.-II—2

Low-pass/high-pass filters



Typical performance
IC $\frac{1}{4}\times$CD4001AE
Quad NOR gates
Supply +10V
C_1 1nF
C_2 4.7nF
C_3 100nF
R_1, R_2, R_3 100kΩ
Cut off frequency $\approx$750Hz
$Q\approx 0.7$
i.e. Butterworth response low-pass filter.



Theoretical relationships
$f_0=1/2\pi\sqrt{C_1C_2R^2}$
where $R_1=R_2=R_3=R$ and f_0 is the cut-off frequency of the resulting low-pass characteristic. Damping factor ζ is related to Q by $Q=1/2\zeta$ and Q is controlled by the ratio of C_2 to C_1. Accurate control is not possible because of low amplifier gain but $C_2=C_1\times 9Q^2$ i.e. for $Q\sim 1/\sqrt{2}$, $C_2\sim 4.5C_1$.

Circuit description
Low-pass filters normally have a flat response up to a given frequency, a rapid fall-off at much higher frequencies, and very little if any increase in amplitude during the transition from the pass-band to the stop-band. This corresponds to damping-factors of the order of unity and Q-factors which are normally equal to or less than one ($Q=1/\sqrt{2}$ is the condition for one standard filter the Butterworth type). Such a characteristic places no great demands on the amplifier used to implement it unless the accuracy required is high as in multi-order filters. For routine attenuation of hum, noise, and other unwanted signals a voltage gain of -20 to -100 is more than adequate, and c.m.o.s. inverters can be used. In the circuit shown, C_3 is a large value coupling capacitor that allows the d.c. feedback via R_1, R_2 to provide self-bias for the inverter. It rolls off the response at low frequencies but can easily be set to a value that does not affect the normal pass-band. By keeping the resistors constant, the cut-off frequency is inverse to the product C_1C_2, while the Q is controlled by the ratio C_2/C_1. The very high impedance of the c.m.o.s. input makes it possible to use very large values for R_1, R_2 and hence drop the cut-off frequency below, say, 50Hz while using small capacitors. The output has a d.c. content that would make a coupling capacitor necessary in most cases.

Component changes
C_1: 47p to 10μF
C_2: Typically 4 to 5$\times C_1$ or can be varied to change the Q.
R_1, R_2, R_3: 10k to 10MΩ.
C_3: Must be large enough to avoid attenuating lowest frequency signal. 100n to 10μF.
IC: Any c.m.o.s. inverter, gate.
Supply: +5V to +15V

Circuit modifications
- By transposing all the capacitors into resistors and vice versa, the circuit is converted into a high-pass filter. The input capacitor C_3 automatically blocks d.c. and this reduced the component count by one. If a high Q is required, then the ratio R_1/R_2 has to be increased. For $C_1=C_2=C_3=C$, the cut-off frequency is $f=1/2\pi\sqrt{R_1R_2C^2}=1/2\pi C\sqrt{R_1R_2}$ The value of Q is given by $R_1/R_2=4Q^2$ for an amplifier with infinite gain. In practice it would be difficult to obtain a Q of more than 5 while the usual range of Q-values needed in high-pass filters (say 0.5 to 1) is achieved with reasonable accuracy. Higher order filters can be constructed by cascading individual second-order filters. The presence of C_3 at the input simplifies the coupling because each inverter is then self-biasing. It is unlikely that high-order filters would be sufficiently accurate and independent of supply etc to be worth designing by this technique.

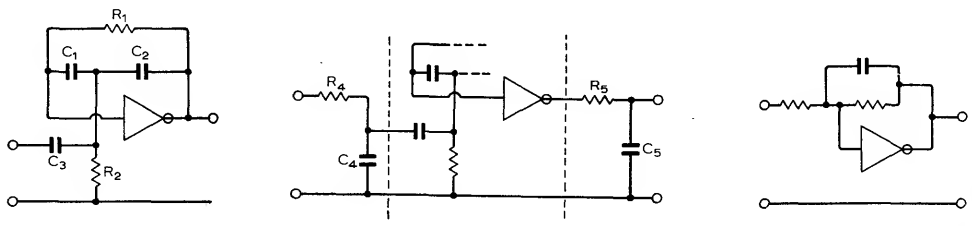
- If precise control of the form of filter characteristics is not needed (i.e. Butterworth, Bessel etc) the order of the filter can be increased by adding separate RC sections at input and/or output.

- Any separate inverter in a system may have a lag introduced into its response by the addition of a capacitor or a series CR network across the feedback resistor. The noise characteristics of c.m.o.s. gates are poor compared with those of low-noise bipolar or f.e.t. discrete circuits, but acceptable results are obtainable for signals well above the millivolt level.

Further reading
Sedra, A. S., Generation and classification of single amplifier filters, *Circuit Theory and Applications*, vol. 2, 1974, pp. 51-67.

Cross references
Set 1, cards 4, 5
Set 16, card 9

Circuit modifications

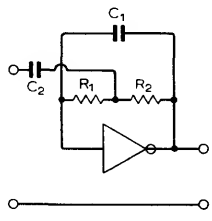


wireless world circard

Set 28: C.M.O.S.-II—3

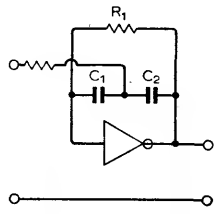
Band-pass/notch filters

Band pass 1



Typical performance
IC ¼×CD4001
(quad NOR gates)
Supply +10V
C_1 100pF
C_2 10nF
R_1 R_2, 100kΩ
f_0 1490Hz
Q 2.5
(For an ideal inverter, $C_2/C_1=4Q^2$ but with the very limited gain the theoretical Q of 5 is reduced to 2.5, see Ref. 1.)

Band pass 2



Typical performance
IC ¼×CD4001
(quad NOR gates)
Supply +10V
R_1 220kΩ
R_2 2.2kΩ
C_1 15nF
C_2 15nF
f_0 460Hz
Q 2.1
$f=1/2\pi\sqrt{R_1R_2C_1C_2}$
& $4Q^2=R_1/R_2$.
In practice $Q>5$ difficult to achieve.

Circuit description
Band-pass filters commonly require differential input amplifiers or multiple amplifiers. This remains true if high Q is needed, particularly if sensitivity to gain and passive component changes is to be minimized. Where a low value of Q is sufficient then simple band-pass filters can be based on single inverting amplifiers. At very low frequencies, the impedance of $C_2\rightarrow\infty$ and the gain $\rightarrow 0$. At very high frequencies the impedance of $C_1\rightarrow 0$ and the gain$\rightarrow$0. At some intermediate frequency, the gain has a maximum value. The theoretical centre-frequency is $1/2\pi\sqrt{R_1R_2C_1C_2}$ and commonly, $R_1=R_2=R$ giving $f=1/2\pi R\sqrt{C_1C_2}$. Considerable departures from the predicted Q-values occur because of the low gain of the amplifier. The centre frequency lay within the tolerance range of the passive components in the samples tested. At the centre frequency, the output is anti-phase to the input. This leads to a simple means of obtaining a notch-characteristic as indicated over. The high values of resistors that can be used make it easy to obtain a very low-frequency band-pass characteristic, while on the high-frequency side operation to beyond 100kHz is possible.

Alternative circuit
The second form of the band-pass filter has comparable performance, and no significant differences were observed. The input impedance will presumably differ from the first circuit, but both impedances can be made high enough for differences to be unimportant.

Component changes
IC: Any c.m.o.s. inverter, buffer, gate.
Supply: +5 to +15V. At low voltages the available voltage gain is too far reduced by loading effects.
R_1, R_2: 10k to 10MΩ. Lower values possible if source impedance is low.

Circuit modifications
The third band-pass filter is based on that of Sallen & Key and the equations given in Ref. 1 are =(4.41 Q^2-1).

$$T_v=\frac{sb\omega_0/2\cdot 2Q}{s^2+s\omega_0/Q+\omega_0^2}$$

where $s=j\omega$

Notch filters are often based on band pass networks, in which a bridge or other balancing system is arranged such that the output tends to zero at the centre-frequency of the band pass. In this case, taking the first circuit overleaf, the input and inverted output are applied to the ends of a potentiometer. As the potentiometer setting is varied, a point is reached where the two signals exactly cancel at the original centre frequency. The principle can be extended to obtain a low impedance output by applying the signals via two resistors to the summing junction of a second inverter as shown. The overall transfer function is then of the form

$$T_v=\frac{H_2s}{s^2+s(\omega_0/Q)+\omega_0^2}-H_1$$

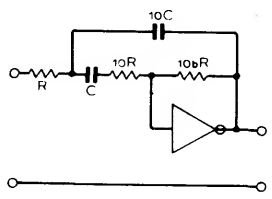
allowing for the inversion due to the second amplifier. ($H_1\propto 1/R_4$, $H_2\propto 1/R_5$)

$$T_v=\frac{H_2s-H_1[s^2+s(\omega_0/Q)+\omega_0^2]}{s^2+s(\omega_0/Q)+\omega_0^2}$$

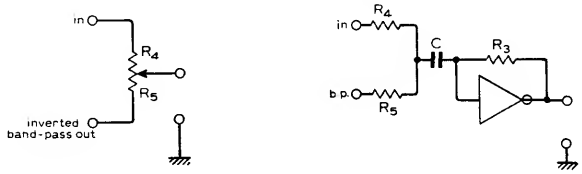
$$=-H_1\left[\frac{s^2+s\left(\frac{\omega_0}{Q}-\frac{H_2}{H_1}\right)+\omega_0^2}{s^2+s(\omega_0/Q)+\omega_0^2}\right]$$

For a notch characteristic, there must be a frequency at which the output goes to zero. This is achieved for $H_2/H_1=\omega_0/Q$ at $s^2+\omega_0^2=0$ i.e. at the same frequency as the peak of the original bandpass function.
For C_2 47nF, C_1 100pF the notch was obtained at $R_5/R_4\sim 33$.
An all pass filter (constant amplitude varying phase shift) follows when the coefficients of in numerator and denominator are equal and opposite. This implies $2\omega_0/Q=H_2/H_1$ and corresponds to $R_5/R_4\sim 16$.

Band pass 3



Notch/All pass filters



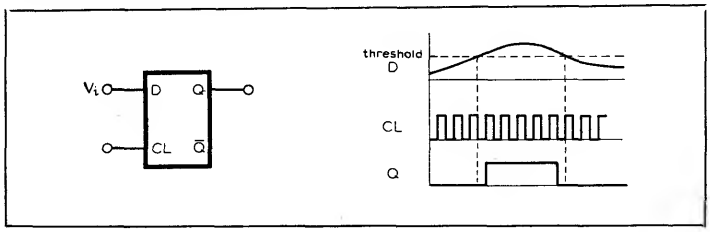
Further reading
Sedra, A. S. Generation and classification of single amplifier filters, *Circuit Theory and Applications*, vol. 2, 1974, pp. 51-67.

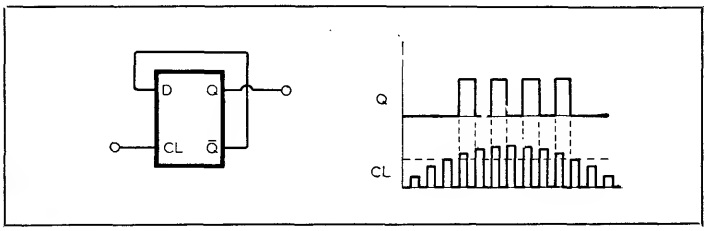
Cross references
Set 1, card 8
Set 16, cards 7, 8

wireless world circard

Set 28: C.M.O.S.-II—4

D-type analogue circuits-1





D.C. level sensing
The D-type flip-flop has a data input which responds to a 0 or 1 input by transferring these to the Q output when the device is clocked. The threshold between these two regions varies from device to device, but varies little with temperature. For moderate variations in supply voltage it is also a fixed fraction of that voltage and the transition between regions is sharp. If a varying d.c. voltage is applied to the data input, and the flip-flop is continually clocked, then each time the voltage passes through this threshold region, the output changes state on the next clock-pulse. The threshold remained between 44.7% and 45.0% of the supply voltage for V_s 4 to 7V and the effect of temperature was of the order 1mV K^{-1}. If the unknown voltage is derived from a common supply rail regulation would not be required since both it and the device threshold would vary together. The output is 1 for $V_D > V_T$ and 0 for $V_D < V_T$.

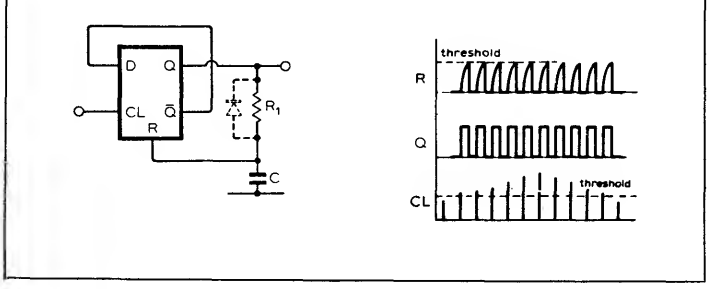
Pulse height detector
The flip-flop is set up as a $\div 2$ circuit by returning the data input to the $\overline{Q}$ output. For each normal clock pulse the Q output is thus set to the previous state held on the $\bar{Q}$ output i.e. the state of Q (and hence of $\bar{Q}$) is reversed. If the clock pulses fall below the threshold value of the C_L input they are ignored and the output retains its previous state. This threshold level is controlled by gates similar to those at the D input and hence the threshold level is of the same order —45/55% of the supply, but with the same well-defined characteristics for any given device. The output is a square wave of half the input frequency for $V_{CL} > V_T$ and either 0 or 1 for $V_{CL} < V_T$. A small amount of inherent hysteresis appears to exist in such applications as these. The input amplitude has to reverse itself by up to about 1% after effecting a change in the output in order to reverse that change.

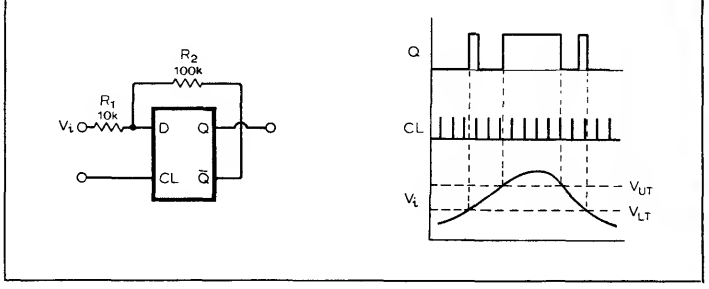
Pulse-height-sensing monostable
The Q output is returned by a short time-constant circuit composed of R_1C_1 to the re-set input. If the input pulse rate becomes too rapid, an additional diode across R_1 shortens the recovery time of the monostable and allows the output pulse-width to remain independent of pulse-rate. Provided the input pulses, applied to the clock input exceed the threshold then the circuit attempts to toggle. The rest state of the system must be $Q=0$, since for $Q=1$ the reset input would be activated after a short charging period and Q would return to 0. Every time a clock-pulse sets Q to 1, this is what happens, and Q remains on for the time it takes the reset input to reach its threshold value via the charging of C_1 through R_1.

There is one output pulse of defined height and width for every input pulse exceeding the threshold voltage. If a further clock pulse is received during the on-period, the output pulse is terminated. If this is not desired, the D input can be returned directly to logic 1 when such pulses are ignored.

Window comparator
Assume the input voltage is low and that $R_2 \gg R_1$. The D input is below its threshold, and on the next clock pulse, Q is driven to (or held at) 0, and $\bar{Q}$ to 1. This change is insufficient to shift the D input above its threshold and Q stays permanently at 0. Conversely if V_i is high, Q is held permanently at 1. When V_i is close to the threshold, each transition of $\bar{Q}$ shifts the D input across the threshold and the circuit toggles. There are now two effective threshold points V_{LT} and V_{UT}, the lower and upper thresholds, separated by $V_S R_1/(R_1+R_2)$.
For $V_i < V_{LT}$ Q is 0.
For $V_i > V_{UT}$ Q is 1, and for $V_{UT} > V_i > V_{LT}$, Q toggles at $f/2$. For a steady clock rate (f constant) the output mark-space ratio is unity.

A moving-coil indicator at the Q output would read zero, $V_s/2$ and V_s respectively for V_i below between and above the thresholds. Alternatively a l.e.d. would be off, flashing at $f/2$ or permanently on for these three ranges of input volts (this would require a slow-speed clock if the flash rate is to be visible).

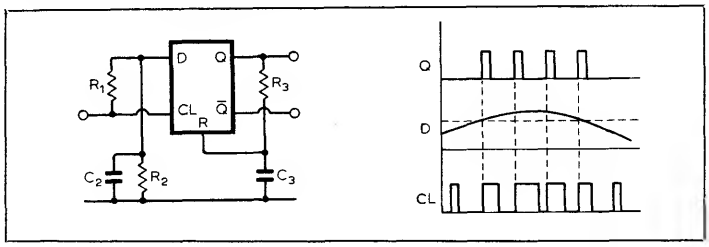




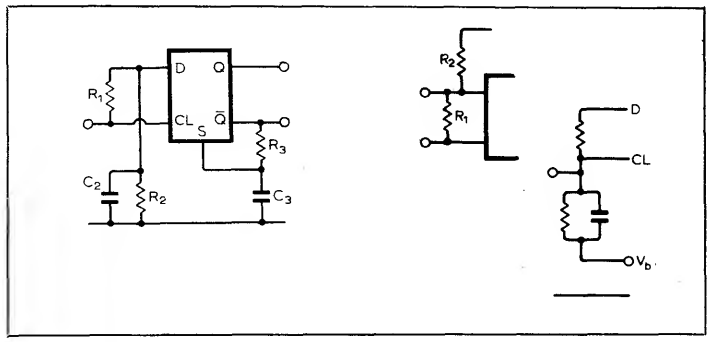
wireless world circard

Set 28: C.M.O.S.-II—5

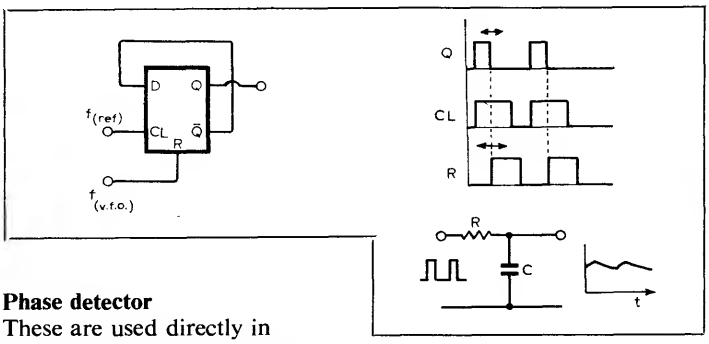
D-type analogue circuits-2



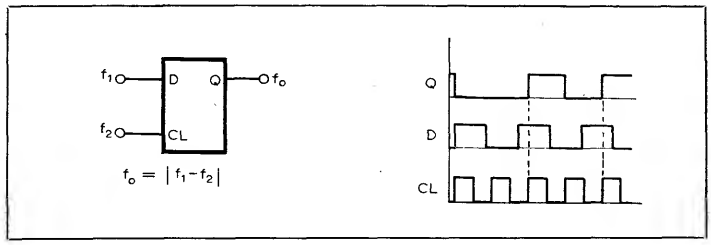
Marks-pace detector
If the input pulse-train has a large mark-space ratio, its mean value may be > 50% of V_S, provided the input pulse height is equal to V_S. If the voltage at D is smoothed by C_2 across the potential-divider formed by R_1, R_2, the threshold will be exceeded and an output pulse-train is obtained. When the mark-space ratio falls below the critical level, the monostable relaxes into its quiescent state with $Q=0$. The circuit basically detects the mean level of the input pulse train and can be used to detect any of the separate variables that affect the area provided that all the others remain constant. Thus for height and frequency constant the circuit detects pulse-width, for height and pulse-width constant it detects a rise in frequency and so on. The pulse-height is well-defined if the previous stage is a c.m.o.s. gate/inverter.



Space-mark detector
The complementary nature of the circuit allows the reversal of the outputs, letting $\bar{Q}$ activate the set input. In each of these circuits the monostable period has to be less than the period of the incoming pulses. As shown, the output at $\bar{Q}$ remains low until the mean value on the D input falls below its threshold, when the $\bar{Q}$ output becomes a pulse train. To adjust the range of mark-space ratios that can be dealt with, a bias current can be provided from the supply or the CR network can be returned to a variable bias voltage. This would need to be supply proportional is using an unregulated supply for all other functions.



Phase detector
These are used directly in determining the phase difference between two signals of the same frequency. The signals are converted into pulses/square waves and the zero-crossings activate a switching circuit such that an output is on only for the interval between the zero-crossings of the two signals. If the output is filtered by an RC circuit the resulting direct voltage is a measure of the phase difference. Assume that the D-type flip-flop is clocked at an instant when $Q=0$. This causes Q to go to 1, a state it retains until the reset goes to 1. The following clock pulse again drives Q to 1 with the period that Q remains at 1 varying as the positive going input at R varies in the delay with respect to the C_L input i.e. according to their phase-difference. The unit is one example of phase-detectors used in phase-locked loops. As the variable frequency oscillator drifts it causes a progressive change in the phase difference between it and the reference oscillator. The resulting change in the mean output is used to control the v.f.o. returning it into synchronism with the reference oscillator.



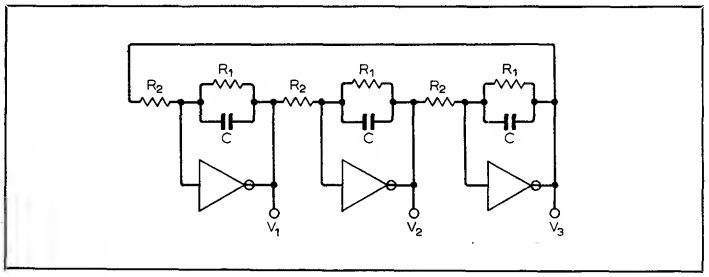
Frequency differencer
Two signals at different frequencies are fed into the D and C_L inputs of a D-type flip-flop. At each clock instant the D input may have either 0 or 1 and hence the output state may or may not change depending on its previous state. When the frequencies are very close it takes a large number of cycles, before a clocking instant coincides with a different value on the D input, i.e. the output rarely changes. When the frequencies are identical the D input always has the same value at the clocking instant and the output never changes. These results are consistent with the claim that the output pulse train has a frequency equal to the difference in the input frequencies. This can be very convenient in measuring small changes in a high frequency signal. It is compared by such a flip-flop with a stable frequency close to its value, and the result can be monitored on simple counters, or analogue frequency meters, on audio frequency amplifiers or displayed on an oscilloscope.

Cross references
Set 28, card 4
Set 19, card 8
Set 21, card 7

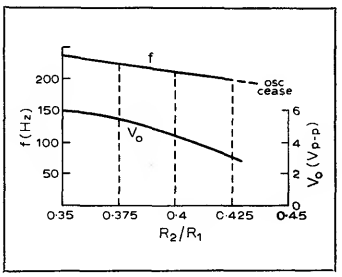
wireless world circard

Set 28: C.M.O.S.-II—6

Three-phase oscillator



Typical performance
IC $\frac{3}{4}\times$CD4001AE
quad 2-input NOR gates
Supply +10V
R_1 100kΩ
R_2 40kΩ
C 15nF
f 213Hz
Amplitudes 3.6, 3.4, 3.5V pk-pk
Distortion 2.2%, 0.4%, 1.1%



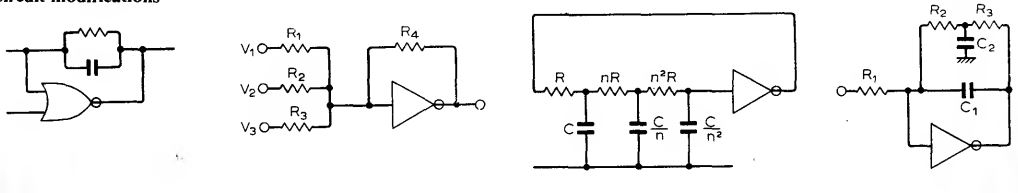
Circuit description
Each inverter has a high input impedance and an inverting voltage gain of magnitude $\gg 1$. The CR network in the feedback path introduces a lagging response. If the system is to oscillate, the loop phase shift must be zero while the overall gain should just exceed unity. If the system is to be symmetrical then each stage must contribute the same phase shift and must separately have unity gain. If the inverter gain is large then with the three inversions, the sum of three equal phase shifts must equal 180° to meet the overall phase condition. This requires a 60° lag from each of the sections. To maintain the magnitude condition at unity, the magnitude of the impedance of R_1 in parallel with C must equal the resistance of R_2. This gives $R_2 = R_1/2$ as the maintaining condition with $f = \sqrt{3}/2\pi CR_1$.
In the practical case the amplifiers have gains ranging from 10 to 50, inverting and with little phase-shift in the audio band. The inherent matching of these inverters because they are formed on a common chip means that provided the resistors R_2 are reduced by the same amount to accommodate this finite gain, then the phase relationships between the outputs are maintained. Non-linearity of the gain provides a coarse form of amplitude limiting. Two effects stem from any change in supply voltage, each controlling the voltage gain of an inverter. The trans-conductance of each device increases as the current increases, while its output slope resistance falls. The voltage gain into open-circuit is higher at low supply voltages making it easier to define the required ratio of resistances; the increased output impedance makes it necessary to use higher value resistors to prevent loss of voltage gain under these circumstances. The output voltage and frequency are also supply dependent but oscillations can be sustained over the range 5V-12V with a broad peak in the output in the 7 to 10V region with the samples used. The phase differences are held to 120° with a deviation of only one or two degrees except where distortion is severe. With R_2 increased to 42.5kΩ, the point at which oscillations are just sustained, one output had a t.h.d. of 0.18%.

Component changes
IC: Any set of three matched inverters: CD4007, $\frac{1}{2}\times$CD4049, $\frac{3}{4}\times$CD4001 with unused inputs taken to '0', $\frac{3}{4}\times$CD4011 with unused inputs taken to '1'.
Supply: In theory any supply voltage within device rating. In practice, at high voltages the open-circuit voltage gain falls; at low voltages the output impedance becomes too high. Best range 5 to 10V.
R_1: Circuit requires relatively high resistance values to reduce loading on output—typically 10k to 10MΩ.
R_2: $R_1/2$
C: can be relatively small even for low frequencies since R large—100p to 1μF.

Circuit modifications
- If the inverters are replaced by logic gates using one input for feedback, then the other input can be used to gate the oscillator. Using NOR gates, a logic '0' leaves the oscillator running, logic '1' drives the output of that gate low i.e. to logic '0'. This via the inverting action of the following stages drives their outputs to '1' and '0' respectively. If all free inputs are taken to '1' all outputs are driven to 0. The converse is true when using NAND gates.
- Most see-saw amplifier circuits can be implemented though at reduced performance because of the low open-loop gain. The outputs of the three-phase oscillator can be summed in any desired proportion by scaling R_1, R_2, R_3, R_4 to give an output at any other phase angle. Note that all outputs are at the same d.c. potential, which will vary from device to device but will be about 50% of the supply.
- A single-stage phase-shift oscillator requires a gain of -8 if the components are graded as shown and n is large. Restricting n to 10, and operating the inverter in the range 6 to 10V comfortably exceeds the condition for sustained oscillation, allowing non-linearity to limit the amplitude. Other combinations of networks and inverting stages can be used (see Set 26).
- An approximately 90° phase-shift can be introduced by passing the signal through the circuit shown. Provided $R_2, R_3 \gg R_1$ and $R_3C_2 \gg R_1C_1$, the circuit approximates to an integrator. If all the inverters are well matched, R_2, R_3, C_2 can be omitted.

Cross references
Set 26, cards 3, 4
Set 21, card 5

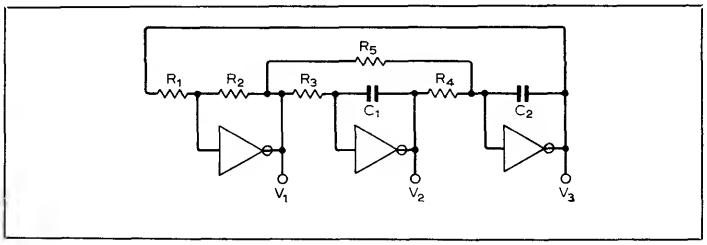
Circuit modifications



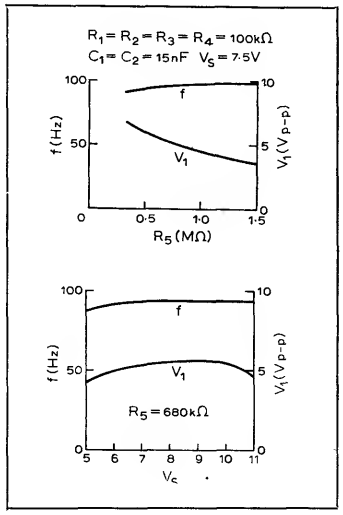
wireless world circard

Set 28: C.M.O.S.-II—7

Two-integrator oscillator



Typical performance
IC ¾ × CD4001AE
NOR gates
Supply +7.5V
R_1, R_2, R_3, R_4 100kΩ
C_1, C_2 15nF
R_5 1.5MΩ
Amplitudes
V_1 3.5V pk-pk 1.1% t.h.d.
V_2 3.6V pk-pk 0.6% t.h.d.
V_3 3.9V pk-pk 0.75% t.h.d.



Circuit description
Assume initially that the inverters have a high voltage gain and that the network impedances are high enough to avoid significant loading of the inverter outputs. The system is then a two-integrator oscillator (as described in Set 26). The integrators produce a total phase shift of −180° which combined with three inversions gives an overall phase shift of zero. The finite gains and output impedances of the inverters reduce the effective Q of the system, and a separate positive feedback path is introduced via R_5 to initiate oscillation. Amplitude control is via the non-linearity of the inverters—as R_5 is reduced in value, the amplitude increases until distortion reduces the average loop gain over the cycle to accommodate the increased feedback. An alternative method of controlling the oscillation is to increase the ratio of R_2: R_1 while maintaining R_5 constant (or omitted in some cases). The three outputs are of different phase and somewhat different amplitude. The phase differences are of the order of ±90° with V_1 lagging and V_3 leading on V_2 (strictly these voltages lead and lag but with an additional inversion in each case). The resistor values may be large without the inverter inputs loading the network; the values should be large to minimize loading on the amplifier outputs. N.B. The low distortion obtained above is because only a small amount of positive feedback was used i.e. the output was not driven into its very non-linear region. For guaranteed oscillation more distortion would have to be accepted.

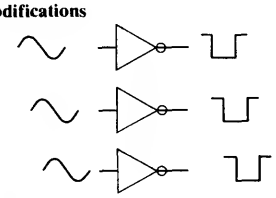
Component changes
IC: Any c.m.o.s. device containing at least three inverters, NAND or NOR gates.
Supply: Will not oscillate satisfactorily at either very high or very low voltages unless excessive feedback used. 5 to 10V is suitable range for most i.cs.
R_1 to R_4: Normally equal; variation of any one changes f with relationship $f \propto 1/\sqrt{R}$. For continuous variation in frequency with less change in amplitude, replace R_3 and R_4 by a twin-gang pot. Range of values for R_1 to R_4 typically 10k to 10MΩ. With high values it is more difficult to provide controlled positive feedback.
$R_5 \gg R_1$ etc typically $R_5/R_4 \approx 5$ to 20.
C_1, C_2: 1n to 10μF.
(To obtain very low frequencies use large capacitors but not polarized units. The leakage currents may restrict the Q and inhibit oscillation.)

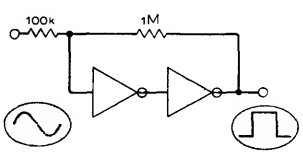
Circuit modifications
● Spare gates/inverters can be used to provide anti-phase outputs. If used with a pair of resistors as in the first amplifier overleaf an inverted sine wave output can be obtained from any of the three outputs. If the outputs are fed directly to the gates of three inverters, then three square-waves are obtained with 120° phase differences. The rise and fall times are not very fast and Schmitt triggers using two inverters with overall positive feedback give a sharp switching action. All of these outputs are compatible with normal c.m.o.s. logic circuits operated from the same supplies.

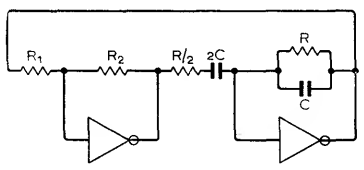
● Most other RC oscillators based on inverting amplifiers, op-amp see-saw circuits etc can be constructed using c.m.o.s. gates/inverters. Because the gain is already low any further losses at high frequency worsens the performance, increasing the distortion to unacceptable levels. Nonetheless oscillation to beyond the audio band is possible. As an example consider the Baxandall version of the Wien-bridge oscillator. As with the previous circuit, using more than one amplifier helps to offset the limited gain of each stage. The RC values are scaled so that the outputs are antiphase and approximately equal in value. The maximum gain of the frequency-dependent stage is a little less than unity. Hence $R_2 > R_1$ is needed.

Further reading
Good, E. F. Two-phase low-frequency oscillator, *Electronic Engineering*, vol. 29, 1957, pp. 164-9 and 210-3.

Circuit modifications



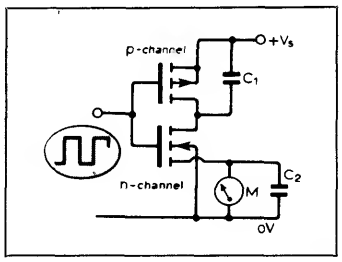




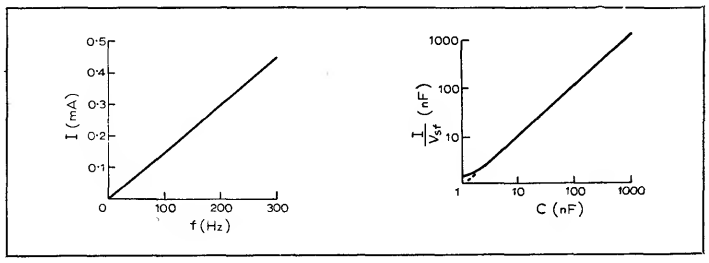
wireless world circard

Set 28: C.M.O.S.-II—8

Frequency-voltage converter

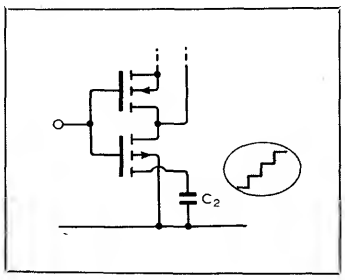


Typical performance
IC $\frac{1}{3} \times$ CD4007AE
Supply +10V
C_1 0.1μF
Meter 500μA, 200Ω
Input Logic level pulse train
0 to 300Hz
C_2 100μF
I fC_1V_s

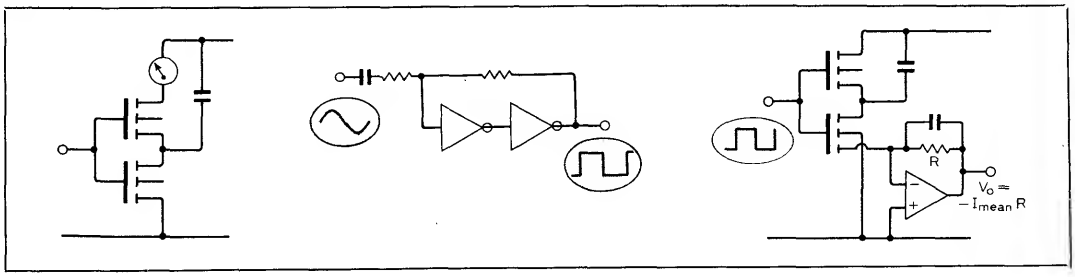


Circuit description
The circuit is simple in concept and exploits the characteristics of c.m.o.s. very well. The two devices are switched alternately in and out of conduction. When the p-channel device conducts it completely discharges the capacitor provided that it is left in conduction for a long enough period. When the n-channel device conducts, it charges the capacitor fully to the supply voltage. The current flows through the meter with the shunt capacitor limiting transient effects due to meter inductance. The total charge flow per pulse is C_1V and if this occurs at a frequency f, the charge per second is fC_1V. This is by definition the mean current flow, the parameter to which the moving-coil meter responds. A small non-linearity occurs when the meter p.d. increases, since this reduces the p.d. to which the capacitor charges on the following pulses. The effect at these levels is to reduce the full scale value by less than 1%. In addition to the external physical capacitance, various strays internal and external to the circuit add to the meter reading. For a 15V supply and a meter full-scale sensitivity of 1.5mA, the meter reading was 9% high at 100kHz with a 1nF capacitor. Removal of that capacitor confirmed the presence of strays by leaving a meter reading of just over 9% of full-scale at the same frequency. The full-scale frequency range is then inverse to the value of capacitance used. This is verified up to 1μF, where the full-scale reading corresponds to 100Hz. Using a 10V supply, a 1mA movement gives the same overall sensitivity.

Component changes
IC: Any pair of complementary enhancement mode m.o.s.f.e.ts. Other manufacturers equivalents of this i.c. may vary in respect of minimim/maximum supply voltage, frequency range cost etc but the same principles apply.
Supply: 3 to 15V. At low voltages meter sensitivity needs to be increased to 100μA. At high voltages a limiting resistor in series with the capacitor minimizes the peak current.
C_1: 1n to 10μF. For low values, a smaller capacitance than indicated in simple theory will be needed to allow for strays. At very low frequencies additional smoothing of the output is needed to reduce meter fluctuations.
C_2: Used to suppress transients and/or reduce meter fluctuations at low frequencies. Not critical —may be omitted.
Meter: 50μA to 5mA depending on supply voltage and range required.



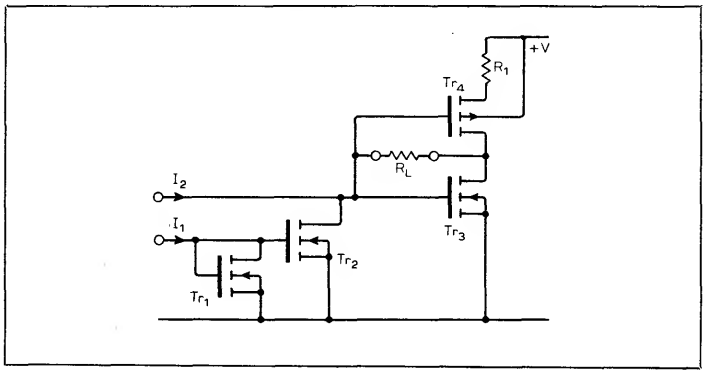
Circuit modifications



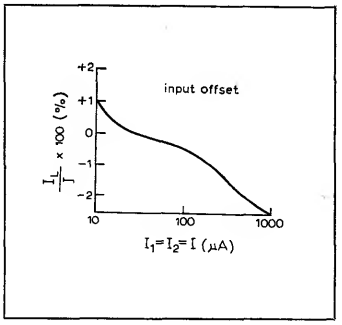
Circuit modifications
Omitting the meter and any other resistive load, produces a simple staircase generator. The output becomes non-linear as it becomes a significant fraction of the supply. A simple threshold detector using a D-type flip flop (see card 4) operated from a lower supply voltage, could be used to discharge the capacitor and restart the cycle after the end of the monostable period. The high impedances would allow a simple pulse-counting approach to be implemented at low frequencies since there would be negligible capacitor discharge. The locations of meter and capacitor can each be altered to either of the supply lines i.e. the meter can be used to measure the mean current of either charge of discharge cycles. The mark-space ratio of the input should not deviate too far from unity since the charge and discharge times of the capacitor should each be long enough for the action to be effectively completed before the changeover.
The i.c. contains two other complementary pairs that can be used as a Schmitt trigger for converting smaller sinusoidal or other inputs into a logic-level output. Alternatively if the input pulses are very narrow, they could be used as a monostable or triggered astable. If the frequency range becomes too great, this creates problems with the mark-space ratio.
The output can be converted, into a large linear voltage swing by feeding the current pulses into the virtual earth of an op-amp. Smoothing is eased by virtue of the high feedback resistor e.g. 100kΩ if a 10V output is required from an input averaging 100μA.

Further reading
Johnson, P. A. Complementary MOS Integrated Circuits, *Wireless World*, 1973, pp. 395-400.

Current-differencing amplifier



Typical performance
IC CD4007 (Tr_{1-4})
Supply +15V
R_1 100kΩ
R_L 1kΩ
I_1, I_2 100μA
I_L ±1μA
$I_L = I_1 - I_2$
Output resistance > 100MΩ
at $I_L = 10\mu A$
Max. $R_L \approx 0.5M\Omega$
at $I_L = 10\mu A$ for good linearity



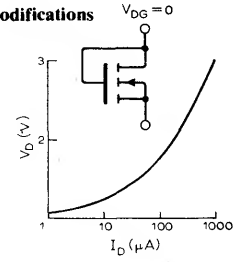
Circuit description
It is possible to duplicate bipolar circuits in m.o.s. form, but a flexible approach is needed if existing c.m.o.s. packages are to be adapted. As an example, consider the current-differencing amplifier (c.d.a., or Norton amplifier). In bipolar form this uses a current-mirror at the input such that the first transistor of the amplifier proper is fed with a current equal to the difference between the input currents. Substituting a pair of n-channel transistors the current-differencing action is still obtained but the p.d. is larger. Assuming the drain-source voltage on Tr_2 is above the pinch-off level, its drain current is comparable with I_1 (net current in R_L is then $I_1 - I_2$). If R_L becomes too large, the output stage saturates and a large voltage change at the gate of Tr_3 disturbs the relationship. The inverting amplifier, Tr_3 has a constant-current load provided by Tr_4 and R_1, since the small voltage swing at the commoned gates of $Tr_{3,4}$ produces a very small fractional change in the p.d. across R_1. Thus R_1 reduces the quiescent level of current and makes the system operate as a defined transconductance (Tr_3) operating into the feedback resistor R_L. This gives the very high output resistance indicated above. The current transfer-ratio of the current mirror remains close to unity over a wide range of currents—a total change in the imbalance of 3% over a 1000:1 range. The absolute accuracy cannot be expected to be better than one or two percent even under favourable circumstances, but the circuit is capable of resolving minute changes in current i.e. with I_2 as the unknown current, I_1 is adjusted until the output voltage is at some reference level. Any change in I_2 produces an output voltage swing $\Delta I_2 R_L$. Alternatively R_L may be a meter, reading the current difference directly.
The p.d. across Tr_1 is more strongly dependent on current than the V_{be} of a bipolar transistor, but at low currents the rate of change for a given fractional change in current is low enough to allow the assumption of a constant p.d. ($\Delta V \approx 80$mV for a 2:1 range of currents). Hence the current can either be derived from a true current source or from a voltage source and a high series resistance.

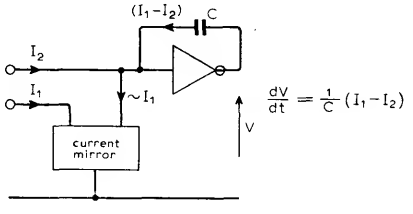
Component changes
IC: Requires access to individual devices
Supply: +10 to +15V
R_1: 10k to 220kΩ

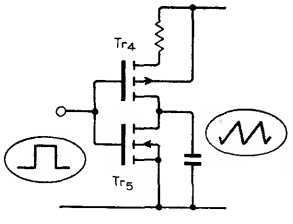
Circuit modifications
- The circuit can be used with any feedback element to define its overall transfer function. For example, with capacitive feedback an integrator results. If either or both of I_1, I_2 are switched in value then the magnitude or direction of the slope of the output waveform can be changed. This allows various triangular and ramp waveforms to be generated. When $I_1 = I_2$ the net current is zero and the output voltage holds its last value.
- Because the currents can be extremely small, long integrating periods can be controlled and it could be the basis of a simple long-period timer. Tr_3 can conduct heavily if overdriven so the output can be rapidly reset to a low value.
- The output stage alone can be gated by a logic level pulse, such that when the input is low Tr_4 conducts as a low-current source and produces a linear ramp (Tr_3 is off). When the input goes high Tr_4 is cut-off and Tr_3 rapidly discharges the capacitor to ground. A source-follower could be used to buffer the resulting triggered ramp.

Cross references
Sets 16, 17, 18

Circuit modifications

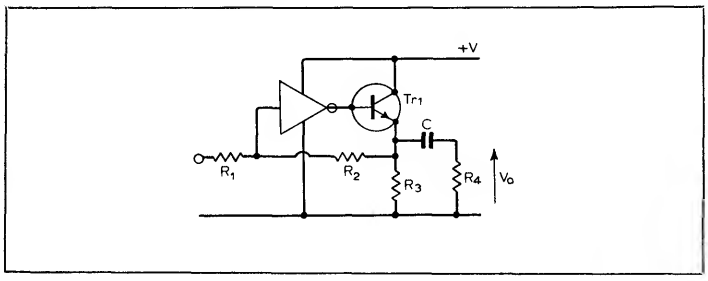




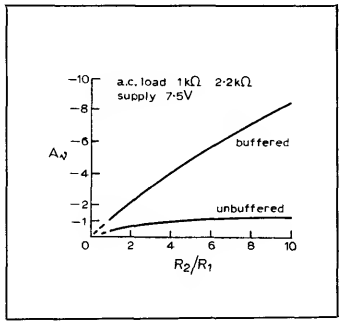


wireless world circard

Transistor outputs



Typical performance
IC ¼ CD4001AE
(quad NOR gates)
Supply +5V
R_1, R_2 100kΩ
R_3 100Ω
R_4 100Ω
C 100μF
V_0 2V pk-pk without heavy distortion
Tr_1 BFR41
Supply current 20mA



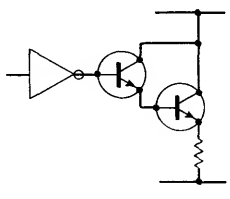
Circuit description
At low supply voltages the c.m.o.s. inverter carries a low current and has a high output resistance. Each of these facts restricts operation to high load resistances. By adding an emitter follower, the effective output impedance can be reduced and the output current increased, both by a factor of 100 or more with a suitable transistor. In the example shown, a peak current of up to 10mA was available for the load while the normal inverter quiescent current under these conditions would be ≪ 1mA. To demonstrate the effect the resistor ratio defining the gain was varied from 1:1 to 10:1 with the c.m.o.s. device driving a 1kΩ load (i) with d.c. coupling to the load i.e. unbuffered (ii) with a transistor having R_3=2.2kΩ, circuit diagram as above. In the unbuffered case, the maximum value of voltage gain obtained was almost independent of the feedback values. This showed that the 1kΩ load was an effective short circuit i.e. that the gain without feedback would have been restricted to −1.3. This corresponds to a g_m of 1.3mS, while the presence of the transistor would increase this to 130mS assuming a current gain of 100. This is enough to allow a practical gain of −8.3 for a resistive ratio of 10:1 even with the a.c. load being represented by R_3 in parallel with R_4.
Another advantage is that the c.m.o.s. output is buffered from the shunt-capacitance of the load plus strays, and the gain-bandwidth product is increased.

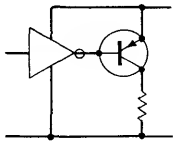
Component changes
IC: Any c.m.o.s. inverter, gate
Supply: +5 to +15V
Because of the current boosting of the output transistor, the c.m.o.s. stage can be operated at lower voltages than is usual for linear operation.
R_1, R_2: Not critical as R_2 no longer loads the output.
R_3, R_4: For class A operation, R_3 has to carry a quiescent current equal to or greater than the peak current required by R_4. This may be up to 100mA with a power transistor.
Tr_1: Current/power rating to suit load. Not critical.

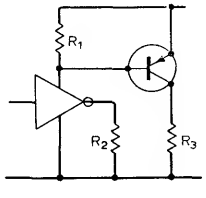
Circuit modifications
As usual, any compound pair of transistors may be added to increase gain-complementary versions if load is to be referred to positive supply rail.
An alternative configuration is to drive the base of a common emitter amplifier (a base limiting resistor may be added at higher voltages). The output is now in phase with the input and the combination is not suitable for the direct application of overall negative feedback. Shunt feedback over the inverter together with series feedback in the transistor (emitter resistor) would be another possibility with overall feedback from the emitter to the input—a form of d.c. feedback pair.
If the inverter supply current is monitored it can be used to switch an output stage; R_2 limits the peak current in the c.m.o.s. stage while R_1 holds the transistor off at lower inverter quiescent currents. In addition to the load current, the c.m.o.s. pair pass through a peak of current as the output swings through its linear region and this complicates the calculations.
Over a large part of the range, the n-channel device can be assumed to be non-conducting particularly when R_2 is low. This leads to the simplified form of circuit shown, where the circuit may be seen as a form of Darlington pair with a p.m.o.s. input stage. Overall negative feedback is possible as shown since the complete stage remains an inverter albeit with a higher output current.

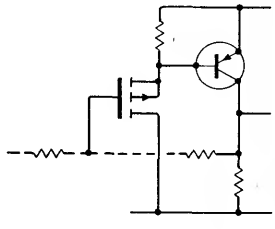
Cross reference
Set 27, card 5

Circuit modifications





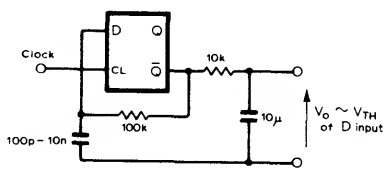


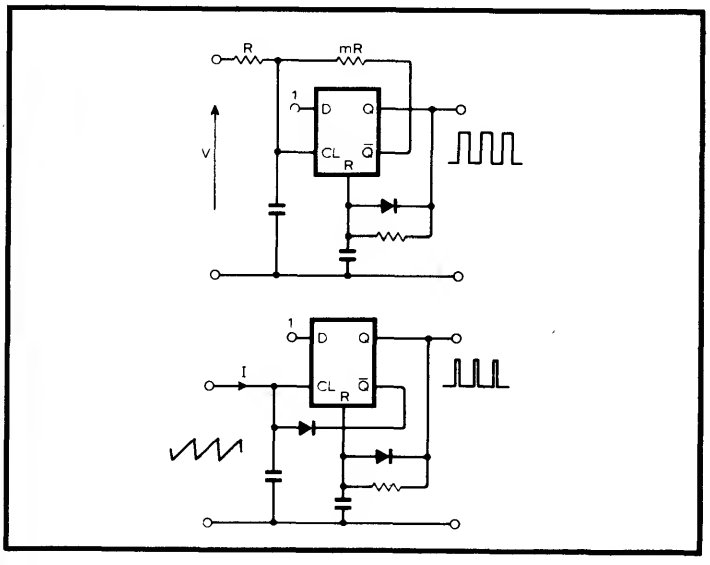


wireless world circard

Set 28: Up-date

These notes offer some novel applications of D-type flip-flops within analogue systems. Where a number of c.m.o.s. devices are to be used for sensing, amplifying etc it can be very convenient to have a reference voltage close to the threshold values of these devices. Such a voltage automatically tracking with any supply or temperature changes by using one D-type flip flop as shown. When it is clocked the Q output switches either to 1 or 0 depending whether the D-input is above or below its sharply defined threshold. The inverted Q output attempts to return the D-input to the opposite state. By choosing the capacitor value in conjunction with the clock frequency, the ripple at the D-input is small and centred about its threshold. The almost-zero input current ensures that the *mean* voltage at Q equals that at D. If the output is smoothed a low-ripple direct voltage results with $V_O \sim V_{TH}$ of the D-input.





By using the other terminals that may be available such as the R and S inputs novel functions are possible. Monostable action has been noted in previous sets, and it can be combined with feedback to the D-input as above. For a low input voltage, then at switch on either Q or Q may go to 1. Assume the former: at some later instant R is driven high driving Q high until the CL input is raised above its threshold and Q goes high again. A pulse train is developed in which the mean value at Q is a function of V. If the monostable action ensures pulses of constant height and width then the pulses rate is a linear function of V. If the output is taken from Q then by adjusting the value of m about unity it is possible to obtain a pulse rate that tends to zero for V = O and to some full-scale value as V approaches V_s.

A ramp generator results if a current is fed to the capacitor at the clock input with a periodic discharge via the diode from Q. Resetting is again a function of the monostable that determines the output pulse width.

Several of these actions can be combined to provide complex functions using the bare minimum number of active devices. The circuit shown is a level-sensing, latching audible alarm. It is easiest to follow by assuming that at some point the input V has exceeded the CL threshold and that the alarm has been initiated. Diode D_4 acts as a half-wave rectifier charging the 15µF capacitor almost to supply level. This constant voltage attempts to raise CL input via D_2. Each time it does so, triggering the flip flop, Q goes high and Q low. The CL input is rapidly returned to zero via D_1 while the monostable action via the R input defined the output pulse width. After resetting D_1 is reverse-biased and the cycle restarts. The Q output is an audio-frequency pulse train whose frequency is only marginally affected by any further changes in V. Until V first exceeds the CL threshold, the circuit remains in a quiescent state with Q low Q high.