THE VERSATILE 4007

Need a versatile CMOS building block for a one-of-a-kind application? Then the 4007 is for you. Find out how to use it here.

RAY MARSTON

THE 4007 IS THE SIMPLEST IC IN THE CMOS line. It contains just two pairs of complementary MOSFET's and a CMOS inverter. However, each element is independently accessible, so the elements can be combined in a great variety of ways. In fact, the 4007 is sometimes known as the "design-it-yourself" CMOS IC, as it can function as a digital inverter, a NAND or a NOR gate, or an analog switch. It can also function as a linear device.

Therefore, not only is the 4007 the simplest CMOS IC, but it is also the most versatile. And that makes it an ideal device for demonstrating the principles by which CMOS devices operate to students, technicians, and engineers. In this article we'll examine the 4007 from both theoretical and practical points of view, and we'll include many circuits that you can use as-is in your next design.

Basic digital operation

The guts of the 4007 are shown in Fig. 1. All MOSFET's in the 4007 are enhancement-mode devices; Q1, Q3, and Q5 are p-channel, and Q2, Q4, and Q6 are n-channel types. The drains and sources of MOSFET's Q1–Q4 are independent; the drain of Q6 is connected to the drain of Q5, so those two MOSFET's compose the inverter mentioned above. Each pair of transistors is protected by a network like the one shown in Fig. 2.

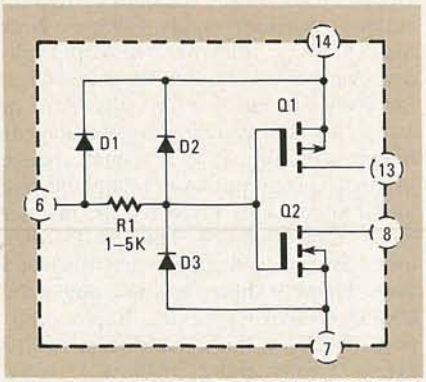

FIG. 2—INPUT PROTECTION CIRCUITRY R1,D1–D3) of each pair of MOSFET's is shown here.

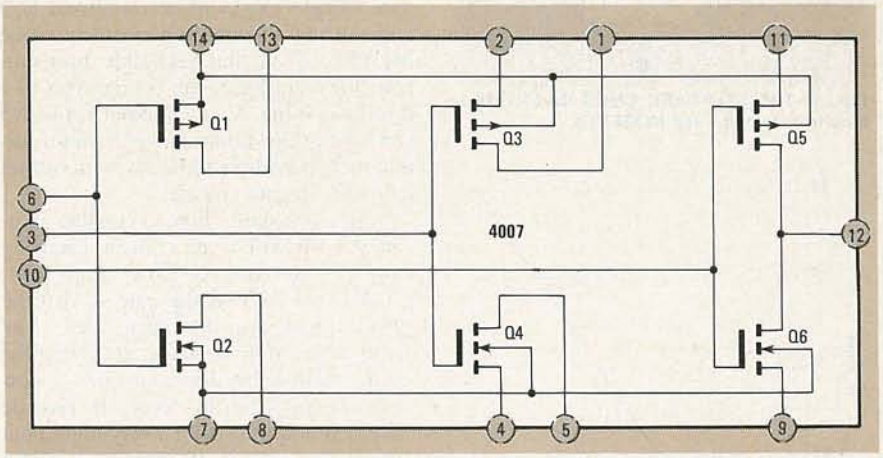

FIG. 1—THE 4007 IS COMPOSED OF three pairs of complementary enhancement-mode MOSFET's.

As you recall, the term *CMOS* is an acronym for *C*omplementary *M*etal *O*xide *S*emiconductor; it is fair to say that most CMOS IC's are designed around CMOS devices like those that compose the 4007. Therefore it is worthwhile to get a good understanding of how those elements work. Let's look first at their digital characteristics; later we'll examine them in light of their analog capabilities.

The two fundamental characteristics of a MOSFET are as follows. First, the gate, or input terminal, of a MOSFET has a near-infinite impedance. Second, the magnitude of the voltage applied to the gate controls the magnitude of drain-to-source current flow.

In an enhancement-mode *n*-channel MOSFET the drain-to-source circuit is a high impedance when the gate is at the same potential as the source. However, that impedance decreases as the potential applied to the gate becomes positive with respect to the source. So an n-channel MOSFET can be used as a digital inverter by wiring it as shown in Fig. 3-*a*. With a low applied to its input the MOSFET is cut off, so the output goes high. With a high applied to its input the MOSFET saturates, so the output goes low.

In a *p*-channel enhancement-mode MOSFET the drain-to-source circuit is also a high impedance when the gate is at the same potential as the source. But, unlike the n-channel device, that impedance decreases as the potential applied to the gate becomes *negative* with respect to the source. So a p-channel MOSFET can be used as a digital inverter by wiring it as shown in Fig. 3-*b*.

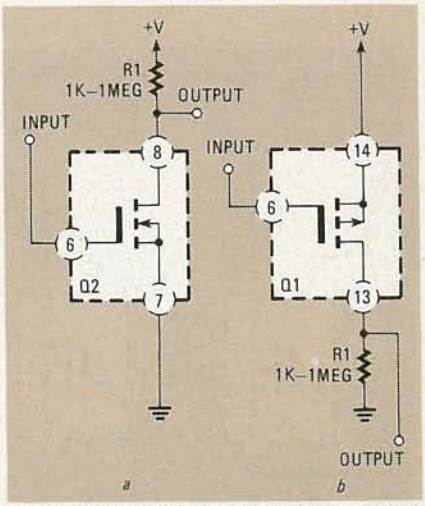

FIG. 3—A DIGITAL INVERTER can be built from either an n-(*a*) or a p-channel MOSFET (*b*).

In both n- and p-channel inverters, the amount of current that flows through the device is limited by the value of R1. And both circuits draw a finite quiescent current in the on state. However, quiescent current drain can be reduced to almost zero by connecting a pair of complementary MOSFET's as shown in Fig. 4.

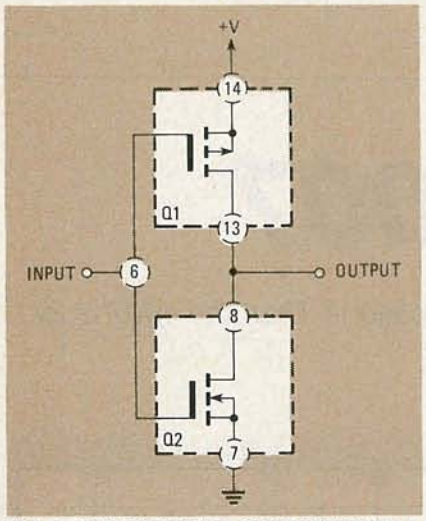

FIG. 4—THE STANDARD CMOS INVERTER is built from two stacked MOSFET's.

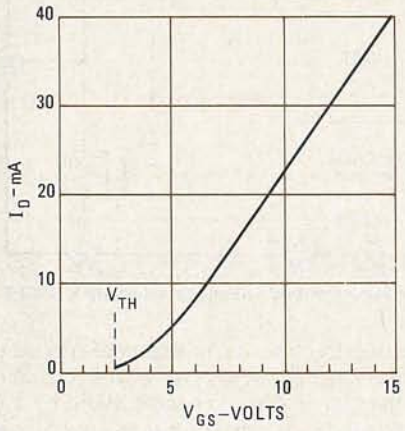

FIG. 5—THE N-CHANNEL MOSFET conducts almost no current until V_{GS} exceeds about 2 volts.

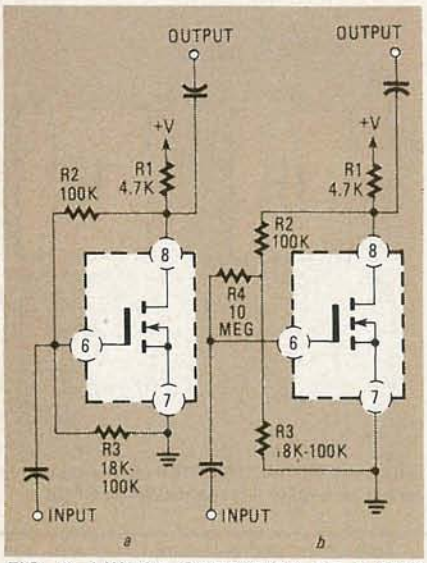

FIG. 6—LINEAR OPERATION OF A 4007 MOSFET requires simple biasing (*a*); very high input impedance is achieved by the addition of R4 (*b*).

In that configuration, which is standard for many CMOS inverters and buffers, with a low applied to the input, Q1 is on, so the output is high. However, Q2 is off, so no quiescent current can flow. With a high applied to the input, Q2 is on, so the output is low. In that case Q1 is off, so quiescent current flow is still nil. Of course, there is no requirement that the MOSFET's be operated solely in the digital mode; let's find out how they can be used otherwise.

Basic linear operation

To understand the operation of CMOS circuitry, it is essential to understand the linear characteristics of the basic MOSFET. Figure 5 shows the typical gate-voltage (V_{GS}) to drain-current (I_D) curve of an n-channel enhancement-mode MOSFET. Note that negligible drain current flows until the gate votage rises to a threshold value, V_{TH}, of about 1.5 to 2.5 volts. After that point, however, drain current increases almost linearly with further increases in gate voltage.

Figure 6-*a* shows how to connect an n-channel MOSFET as a linear inverting amplifier. Resistor R1 is the drain load, and R2 and R3 bias the gate so that the device operates in the linear range. The value of R3 must be selected to give the desired quiescent drain current; it normally ranges from 18–100K. To provide the linear amplifier with a very high input impedance, wire a 10-megohm resistor (R4) as shown in Fig. 6-*b*.

Figure 7 shows typical VI characteristics of an n-channel MOSFET at various fixed values of V_{GS}. To understand that graph, imagine that, for each curve, V_{GS} is fixed at V_{DD}, but that V_{DS} can be varied by altering the value of the drain-load resistor. The graph can then be divided into two characteristic regions, as indicated by the dotted line: the ohmic region and the pinch-off region.

For each curve shown in Fig. 7, the beginning of the pinch-off region—the point where the dashed line crosses the solid line—is called the pinch-off voltage, or V_P, which is the value of V_{DS} above which I_D increases little, if at all, for further increases in V_{DS}.

When the MOSFET is in the pinch-off region and V_{DS} is more than 50% of V_{GS}, the drain functions as a constant-current source. The amount of current that flows is controlled by V_{GS}. A low value of V_{GS} gives a low current flow, and a high value of V_{GS} gives a high current flow. Those saturated constant-current characteristics protect CMOS devices from short-circuit failure and also determine operating speed at various supply voltages. Both current-drive and operating speed increase in proportion to the supply voltage.

When the MOSFET is in the ohmic region and V_{DS} is less than 50% of V_{GS}, the drain functions as a voltage-controlled resistance. That resistance increases approximately as the square of V_{GS}.

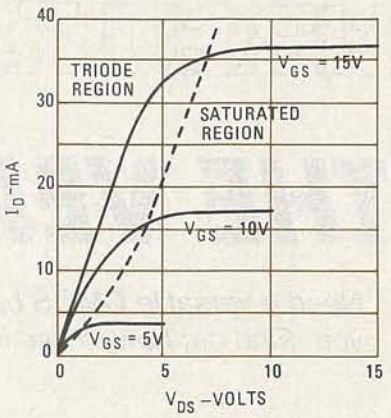

FIG. 7—AN N-CHANNEL MOSFET operates linearly in the ohmic region above the dashed line and digitally in the pinch-off region below the dashed line.

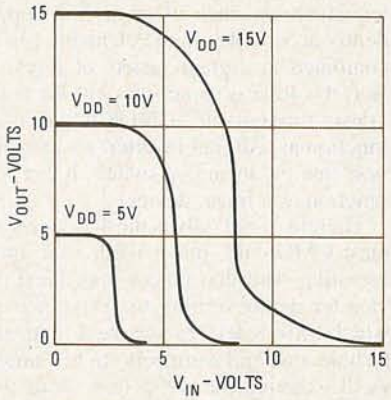

FIG. 8—VOLTAGE-TRANSFER characteristic of the CMOS inverter (Fig. 4) reveals that, for inputs near ground and V_{DD}, output changes very little.

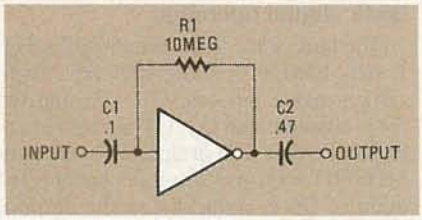

FIG. 9—LINEAR OPERATION of the inverter (Fig. 4) is possible, as shown here.

Figure 8 shows typical voltage-transfer characteristics of the standard CMOS inverter at different supply voltages. Note that when V_{DD} is 15 volts, the output voltage changes a very small amount when the input voltage is near either zero or V_{DD}. However, when the input voltage is biased at roughly $V_{DD}/2$, a small change in input voltage produces a large change in output voltage. Typically, the inverter has a voltage gain of about 30 db when used with a 15-volt supply, and 40 db at 5 volts. Figure 9 shows how to connect the CMOS inverter for use as a linear amplifier; the circuit has a bandwidth of 710 kHz at 5 volts, and 2.5 Mhz at 15 volts.

We can wire three simple CMOS inverters (like the one shown in Fig. 4) in series

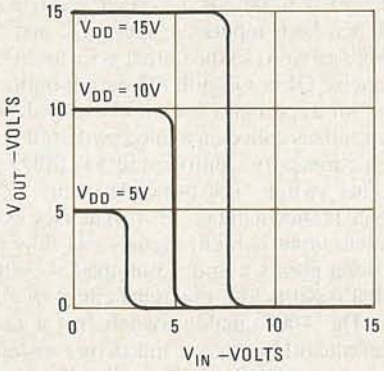

FIG. 10—VOLTAGE-TRANSFER characteristic of a B-series CMOS inverter is similar to that of the simple inverter.

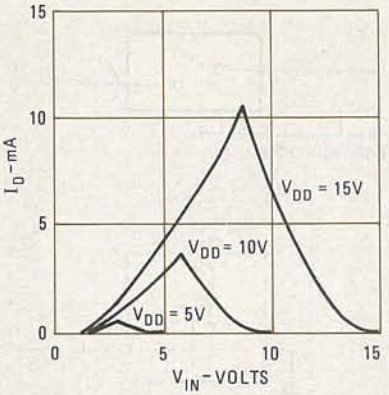

FIG. 11—DRAIN CURRENT of the simple inverter peaks at an input voltage just over $V_{DD}/2$.

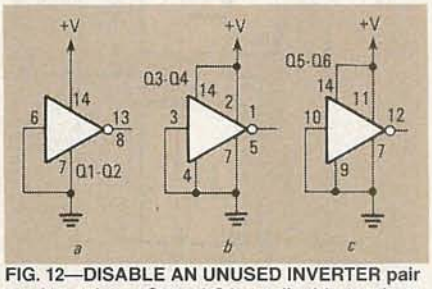

FIG. 12—DISABLE AN UNUSED INVERTER pair as shown here; Q1 and Q2 are disabled as in *a*; Q3 and Q4 as in *b*; Q5 and Q6 as in *c*.

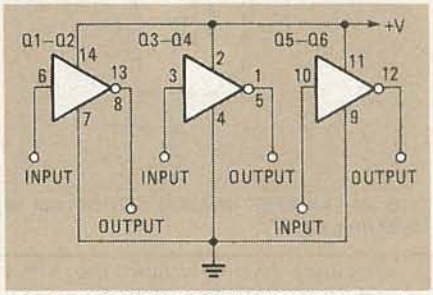

FIG. 13—EACH PAIR OF TRANSISTORS may be used independently as an inverter.

to obtain the direct equivalent of a modern "buffered" B-series inverter, which has the overall voltage transfer curve shown in Fig. 10. A B-series inverter typically gives about 70 db of linear voltage gain, but it tends to be quite unstable when used in the linear mode.

To finish up our discussion of basic operation, take a look at Fig. 11. Shown there is the drain-current transfer characteristics of the simple (non-buffered) CMOS inverter. Note that drain current is zero when input voltage is zero or V_{DD}. However, in the middle range, current rises to a maximum value when the input is at approximately $V_{DD}/2$, at which point both MOSFET's are on. That on current can be reduced by wiring resistors in series with the source of each MOSFET. We'll use that technique in the "micropower" circuits discussed below.

Basic rules

There are a few basic rules to follow in order to use the 4007 successfully. First, you must ensure that all unused elements of the devices are disabled. A pair of MOSFET's can be disabled by connecting them as an inverter and grounding their inputs. As shown in Fig. 12-*a*, to disable the Q1-Q2 pair, just ground pin 6. To disable the other pairs, in addition to grounding the inputs, the sources and drains must be connected to ground and +V as shown in Fig. 12-*b* and Fig. 12-*c*.

In use, the input terminals must not be allowed to rise above V_{DD} (the supply voltage) or below ground. To use an n-channel MOSFET, the source must be tied to ground, either directly or through a current-limiting resistor. To use a p-channel MOSFET, the source must be tied to V_{DD}, either directly or through a current-limiting resistor.

Digital circuits

A single 4007 can be configured as three independent inverters, as shown in Fig. 13. In that figure, and in others that follow, we won't necessarily show all details of how to wire the circuit under discussion. Also, multiple pin connections that terminate in a single function will be shown as in Fig. 13. For example, the output of the Q1-Q2 inverter in that figure is obtained by connecting pins 13 and 8 together.

Figure 14 shows how to connect the 4007 as one inverting and one non-inverting buffer. In the non-inverting circuit, the Q1-Q2 and Q3-Q4 inverters are simply wired in series to provide two stages of inversion—which provides a non-inverting buffer.

The maximum source (load-driving) and sink (load-absorbing) currents of a simple CMOS inverter are about 10—20 mA when either output MOSFET is fully on. To increase that sink current, several n-channel MOSFET's can be connected in parallel in the output stage. Figure 15 shows how to configure the 4007 as a high sink-current inverter. Similarly, Fig. 16 shows how to configure the IC as a high source-current inverter. Last, Fig. 17 shows how to connect all the elements of a 4007 in parallel to produce a single inverter that will both sink and source three times the current of a standard inverter.

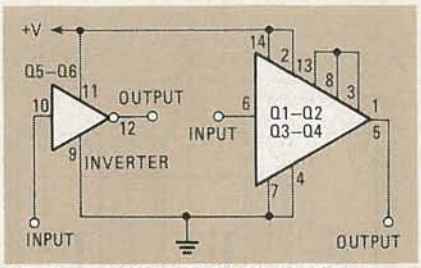

FIG. 14—A NON-INVERTING BUFFER is composed of two inverters connected in series (Q1–Q4). The other inverter (Q5 and Q6) can be used independently.

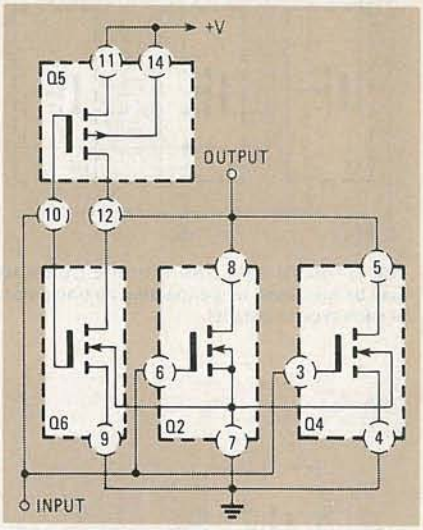

FIG. 15—SINK CURRENT may be increased by connecting the n-channel MOSFET's in parallel.

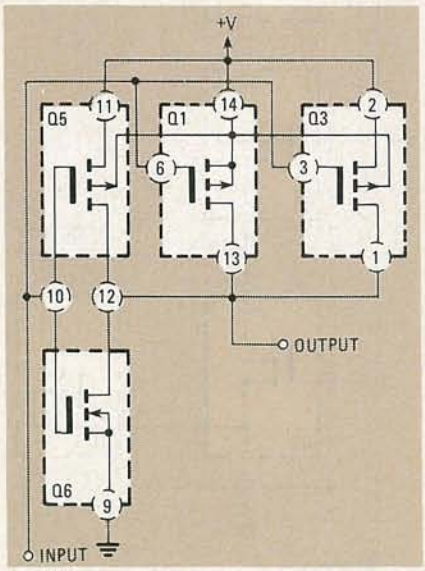

FIG. 16—SOURCE CURRENT MAY BE INCREASED by connecting the p-channel MOSFET's in parallel.

Logic circuits

The 4007 is well-suited for demonstrating the basic principles of CMOS logic

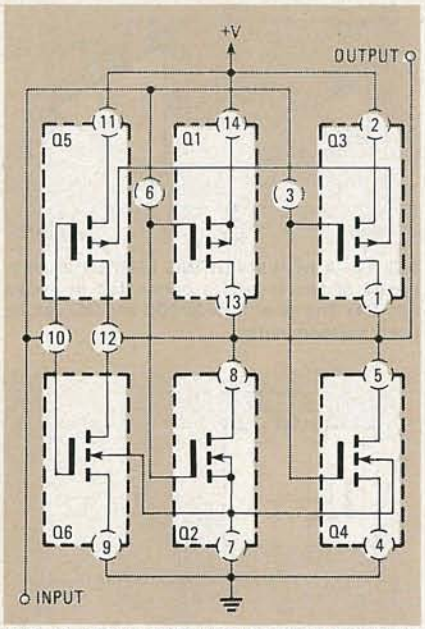

FIG. 17—BOTH SINK AND SOURCE CURRENT may be increased by connecting all transistors of each type in parallel.

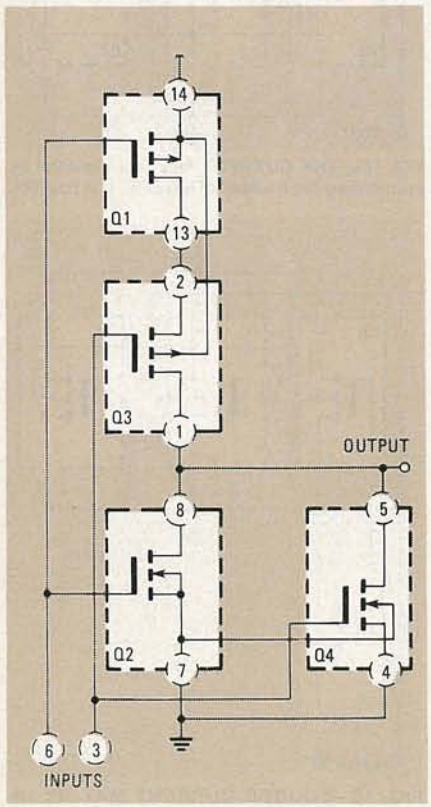

FIG. 18—A TWO-INPUT NOR GATE can be built from a 4007.

gates. Figure 18 shows how to configure the 4007 as a 2-input NOR gate. In that circuit two n-channel MOSFET's are wired in parallel so that either can pull the output to ground with a high input. Also, two p-channel MOSFET's are wired in series so that, with low inputs, both must turn on to pull the output high. Figure 19 shows how to wire up a 3-input NOR gate; it is composed of three series- and three parallel-connected MOSFET's, and its principle of operation is the same as the 2-input circuit. Figure 20 shows how to configure the 4007 as a 2-input NAND gate. When both inputs are high, Q2 and Q4 both turn on, so the output goes low. Otherwise Q1 or Q3 pull the output high.

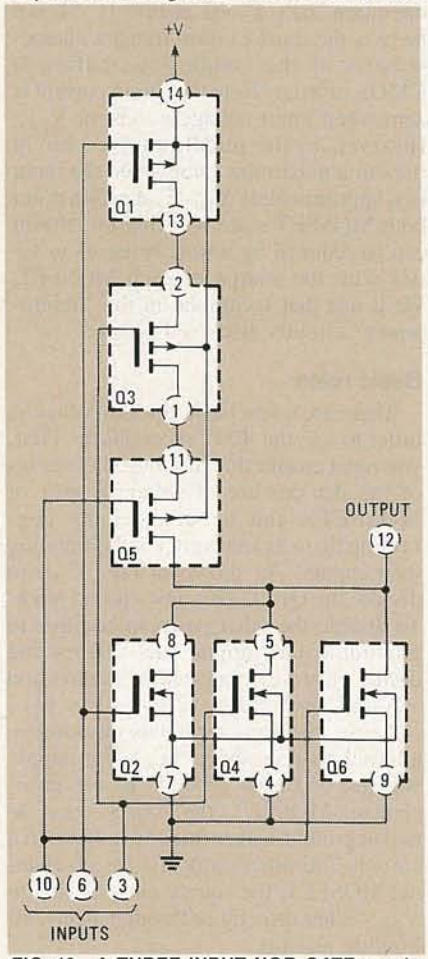

FIG. 19—A THREE-INPUT NOR GATE can be built from a 4007.

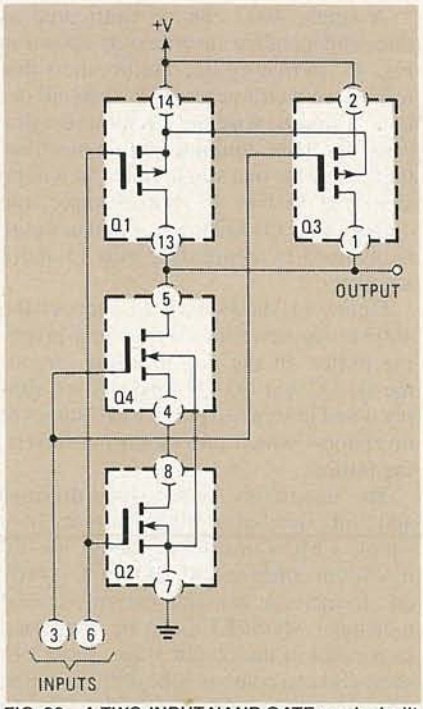

FIG. 20—A TWO-INPUT NAND GATE can be built from a 4007.

An important element of many digital circuits is called an analog switch. It is an electronically-controlled SPST, SPDT, or other switch. The principle of the SPST type is shown in Fig. 21-*a*. When the CONTROL input is high, signals can flow between points X and Y unimpeded. When that input is low, no signal can flow.

The 4007 analog switch has a near-infinite off resistance and an on resistance of about 600 ohms. It can handle signals between zero volts and the positive supply voltage. And since the gate is bilateral, terminals X and Y can function as either input or output.

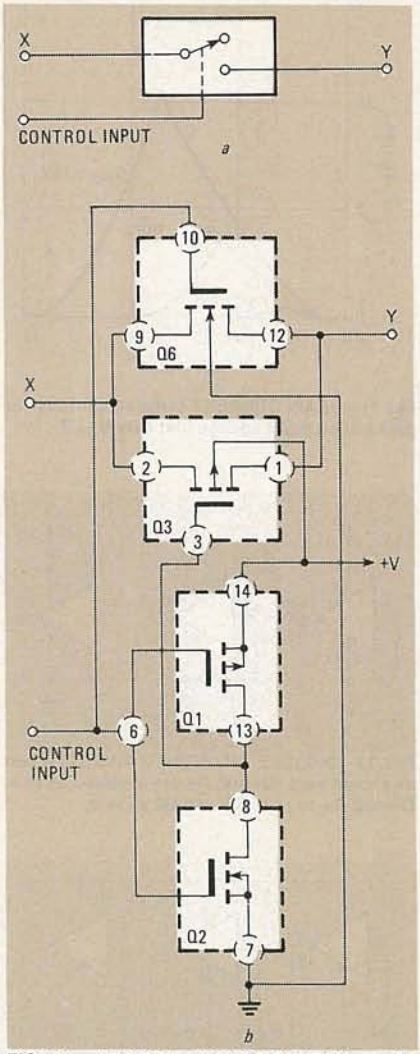

FIG. 21—AN SPST ANALOG SWITCH can be built from a 4007.

Circuitry to implement the SPST switch is shown in Fig. 21-*b*. An n-channel and a p-channel MOSFET are wired in parallel (source-to-source and drain-to-drain), but their gate signals are applied out of phase by means of the Q1-Q2 inverter. To turn the Q3-Q6 pair of transistors on, Q6's gate must be high, and Q3's gate

low; to turn the switch off, the opposite conditions must be present.

An SPDT analog switch is shown in Fig. 22-*a*; circuitry which accomplishes that function is shown in Fig. 22-*b*. Here two transmission elements are connected in parallel, but their control voltages are applied out of phase, so that one switch opens when the other closes, and vice versa.

We saw earlier that the 4007 can also be used in a linear mode; now let's look at how to do that, and at the sort of performance we can expect from a linearly-operated 4007.

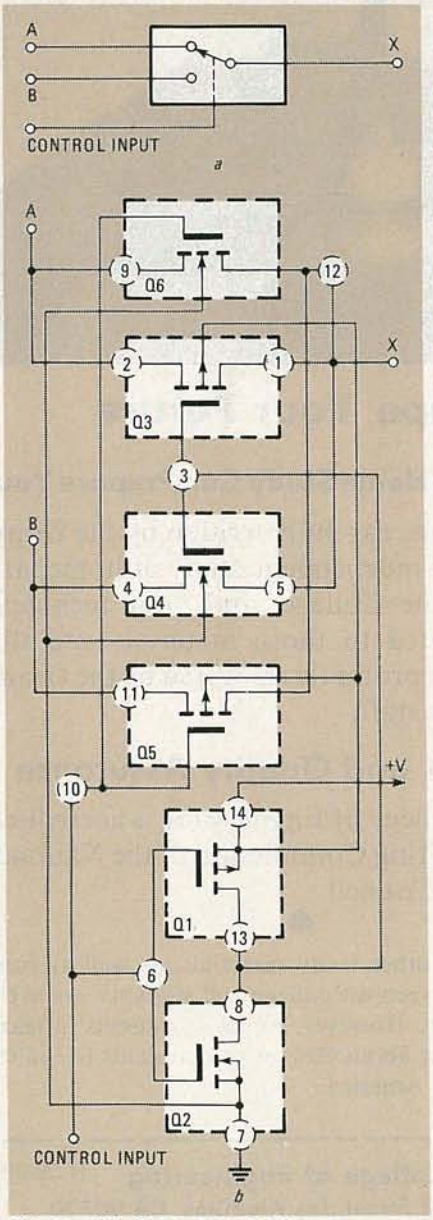

FIG. 22—AN SPDT ANALOG SWITCH can be built from a 4007.

Linear circuits

Figure 23 shows how voltage gain and frequency response vary according to supply voltage. The curves shown in that figure assume that the 4007 is driving a high-impedance (10 megohm), low-capacitance (15 pF) scope probe. The output impedance of the open-loop amplifier typically varies from 3K (at 15 volts) to 5K (at 10 volts) to 22K (at 5 volts). The product of the output impedance and the ouput load capacitance determines the circuit's bandwidth. Increasing either load capacitance or output impedance decreases bandwidth.

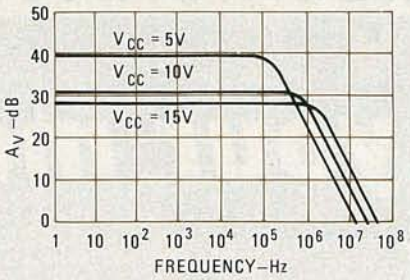

FIG. 23—FREQUENCY RESPONSE and voltage gain of a linear-mode CMOS amplifier is dependent partially on supply voltage.

As you can see in the voltage transfer curve back in Fig. 8, the distortion characteristics of the CMOS linear amplifier are not particularly impressive. Linearity is good for small-amplitude signals, but distortion increases progressively as the output swing approaches the upper and lower limits of the power supply.

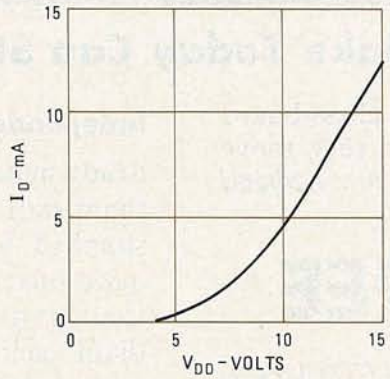

FIG. 24—VERY LITTLE CURRENT FLOWS until V_{DD} exceeds 5 volts.

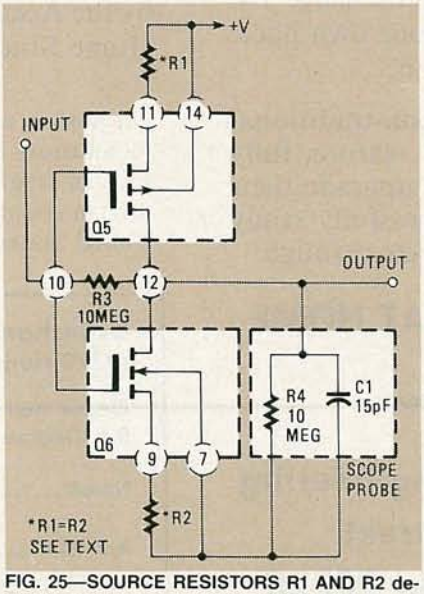

FIG. 25—SOURCE RESISTORS R1 AND R2 decrease current consumption drastically.

TABLE 1—
LINEAR-MODE PERFORMANCE

R1/R2	I_D	A_V	Bandwidth
0	12.5mA	20	2.7 MHz
100Ω	8.2mA	20	1.5 MHz
560Ω	3.9mA	25	300 kHz
1K	2.5mA	30	150 kHz
5.6K	600μA	40	25 kHz
10K	370μA	40	15 kHz
100K	40μA	30	2 kHz
1MEG	4μA	10	1 kHz

Figure 24 shows the typical drain-current versus supply-voltage charcteristic of the basic CMOS linear amplifier. Note that supply current typically varies from 0.5 mA at 5 volts to 12.5 mA at 15 volts.

As we mentioned above, in many applications, the quiescent supply current of a 4007 CMOS amplifier often can be reduced (at the expense of reduced bandwidth) by wiring external resistors in series with the source terminals of the two MOSFET's. In Fig. 25 we show how a micropower circuit would be configured.

It is important to understand that the source resistors increase the output impedance of the amplifier; output impedance is roughly equal to the product of R1 and A_V. That impedance, and the resistance and the capacitance of the load affect the circuit's gain and bandwidth.

Table 1 shows how supply current, voltage gain, and bandwidth vary with the value of those source resistors. As you can see, with 10K source resistors, bandwidth is about 15 kHz. However, by increasing load capacitance to 50 pF, bandwidth decreases to about 4 kHz; by reducing capacitance to 5 pF, bandwidth increases to 45 kHz. Similarly, reducing the resistive load from 10 megohms to 10 kilohms causes voltage gain to fall to unity. The conclusion is that, to obtain significant gain, load resistance must be large relative to the amplifier's output impedance.

An unbiased 4007 inverter has an input capacitance of about 5 pF and an input resistance near infinity. So, if the output of the circuit in Fig. 25 is fed directly to the input of another 4007 stage, the overall voltage gain will be about 30 dB, and the bandwidth will be about 3 kHz. Those values will be obtained when R1 has a value of 1 megohm. For extremely low current drain (.4 μA!), R1 could be increased to 10 megohms.

Now you can see why we said that the 4007 is the most versatile CMOS IC. With the ideas we've presented here, you should have no trouble thinking of many more applications for the 4007. **R-E**