## Design flaw in Ultrasonic Anti-fouling circuit

I worked at Electronics Australia in the early 1980s with Leo Simpson and the rest of the team. Recently, when looking through the September 2016 issue of SILICON CHIP, I saw that a reader had written in with an Ultrasonic Anti-Fouling unit (SILICON CHIP, September & November 2010) blowing fuses. I was asked to troubleshoot a [aycar kit of this project some time ago with an identical problem and discovered a design flaw.

After checking the assembly of the kit I powered up the first part of the circuit (5V supply and micro) and found it worked as per the article. I then powered up the second part (Mosfets) from a second (current limited) supply and found this worked as well. I then removed the second supply, fitted a fuse, and powered the entire project from a 12V, 3A limited supply. At turn-on the unit tried to draw a large current and would have blown the fuse if not for the current limiting.

After some investigation the cause became clear. At power-up the voltage at both Mosfet gates rose to almost 3V for 40ms, turning them both on and drawing a large current. After this, the micro woke up and took control, driving the outputs low and turning off the Mosfets. Fitting 100kΩ resistors between the gates of both Mosfets and GND (across the protection zener diodes) holds the gates low during power up and prevents the Mosfets turning on simultaneously and drawing large currents.

It's standard procedure to pull control signals from a micro to known states during power-up and while the processor is reset. Unfortunately, this one was missed. I expect there is the usual variation in Mosfet gate threshold voltages and this would have a significant effect on the size of the current spike and whether the fuse blew.

When I was looking at the problem I noticed there was a second design (Ultrasonic Cleaner, August 2010) that used a similar circuit and probably has the same issue.

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*Comment: We have had a close look at the circuit and we think your analysis is correct but fitting the gate pull-down resistors will not necessarily cure the problem. Although in the specific case mentioned in the September 2016 issue, it probably would be the solution.*

*Considering that the micro's output states are uncontrolled before power-on reset, the voltage at the Mosfet gates can rise to around 3V, as you say. The mechanism is due to the voltage divider from the 12V supply formed by the Mosfet drain-gate capacitance (typically 270pF) and the gate-source capacitance (typically 1.2nF). The capacitance of the reverse-biassed diodes D1 & D2 would add to this effect.*

*Gate pull-down resistors would fix the problem but we are inclined to specify 10kΩ rather than 100kΩ.*

*However, note that much of the initial surge current is due to the large low-ESR supply bypass capacitor. This was proved in the development of a later commercial version of the design, which had gate pull-down resistors.*

*We also note that this problem has been relatively rare, considering the large numbers of this unit which have been built over the last six years.*