Recommended modification for Pioneer DV45A SPDIF output

This work was done for Vinnie Rossi. The circuit has not been implemented or tested yet. The following data is predicted from the simulations. Real world data will be different, but the percent difference between the circuits should remain constant.

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Factory circuit: 0V to 880mV. Rise time (10% - 90%) = 25ns
Current draw: 1mA: 1mA at 50% duty cycle.

Factory circuit with 220 ohm base resistor: 0V to 2V. Rise time (10% - 90%) = 12ns
Current draw: 6mA peaks (7% duty cycle)+ 1mA at 50% duty cycle

Modified circuit: 0V to 900mV. Rise time (10% - 90%) = 9ns
Current draw: 5mA peaks at 7% duty cycle.

The modified circuit allows changing the 68 ohm series resistor with 10 ohms.
This will probably induce reflections, but the fact that the circuit is safe to
that level means the output resistor can be tweaked substantially to tune to the
transmission line. At 10 ohms output resistance:
0V to 1.5V. Rise time (10% - 90%) = 5ns
Current draw: 5mA peaks at 7% duty cycle.
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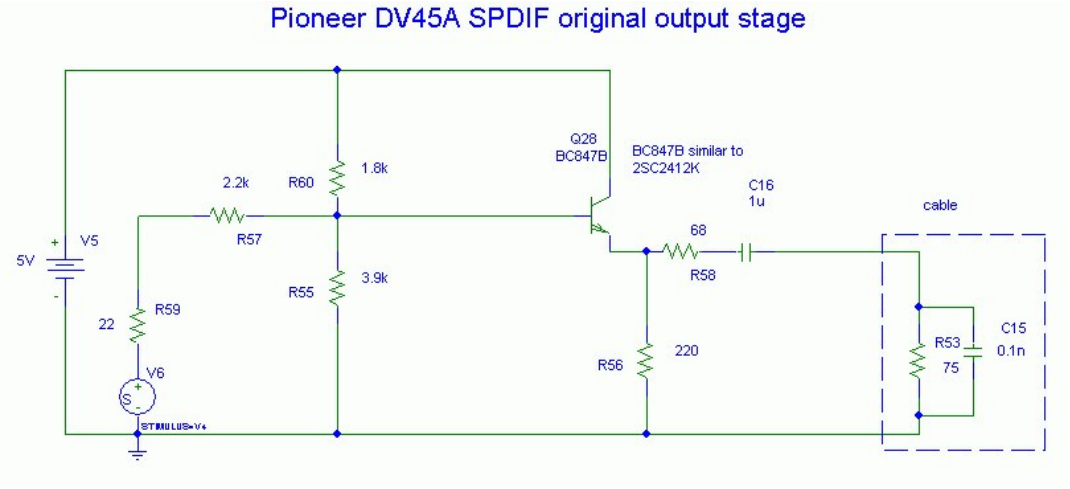
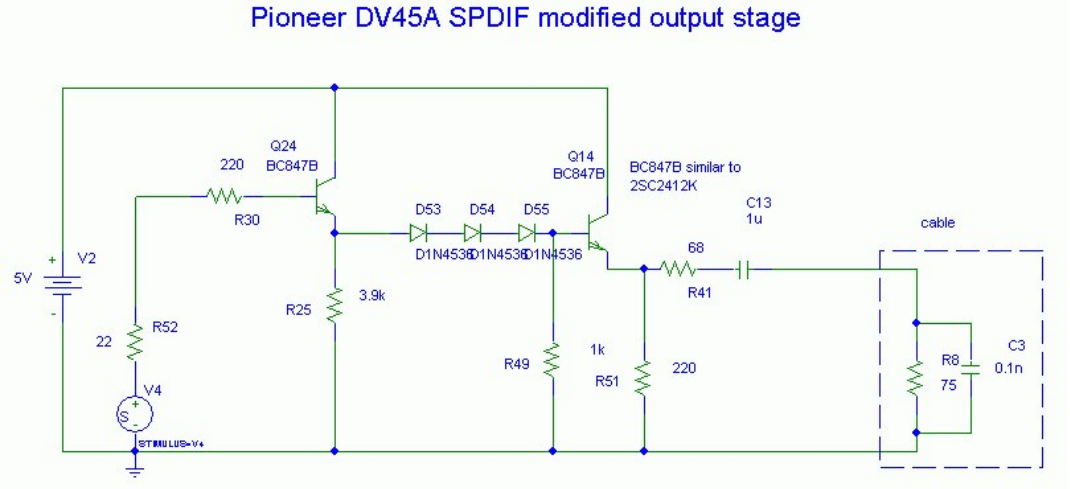


Schematic used to simulate original circuit. Ref designators are mine.

The goal of modifying an SPDIF output is increasing slew rate and eliminating noise on the pulse edges. High end CD transports have risetimes of less than 10ns into 75 ohms; this is not the only reason for good sound, but it is significant.

There are a few things one can do to the single-transistor output stage to improve the slew rate, but most of them ask too much of the IC driving the transistor. For instance, the simplest modification is to replace the 2.2k base transistor with a 220 Ohm resistor. This has the effect of increasing the slew rate, but there are problems with sourcing enough current at the IC.

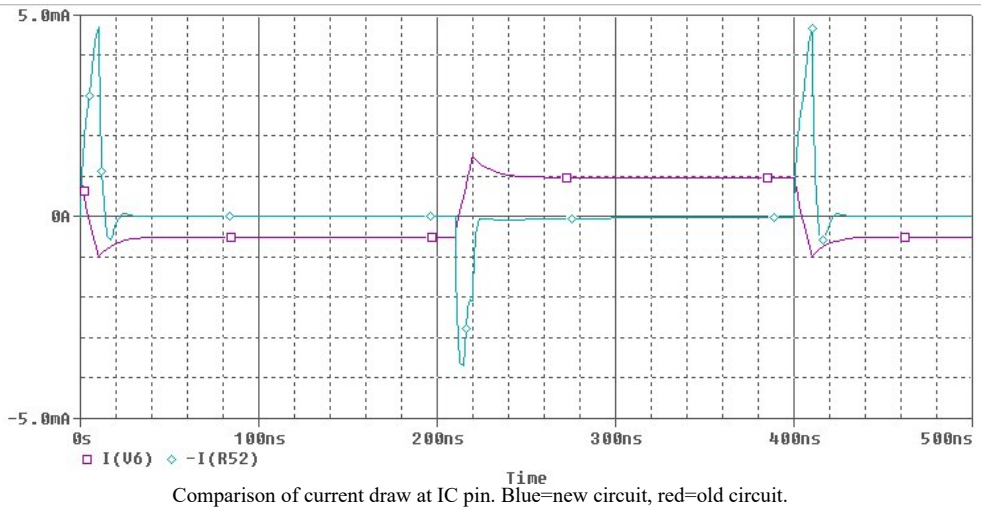
Even though the current at the base of the transistor is 1/B * the current at the emitter (output), the current required to charge the capacitance in the cable is significant, and a fraction of that appears at the transistor base. The only way to really improve the gain of the circuit without frying the IC is to add a buffering transistor.



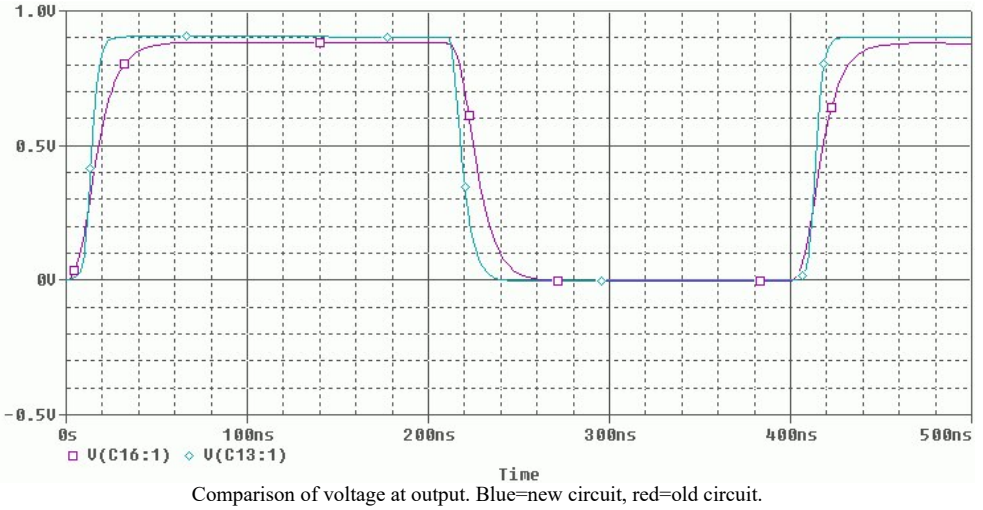
Schematic used to simulate modified circuit. Ref designators are mine.

The three diodes in series drop the voltage at the base of the second transistor so that the output voltage will be lower. If the output voltage is too high, there's a risk of transformer core saturation on the receiver, which would distort the edges. We could reduce the gain of the transistor but that would limit the slew rate.

Replacing the diodes with a resistor bias network slows the edges dramatically. The diodes could also be placed at the output, shunting excess voltage to ground, but this would be a lot of current, and therefore added noise in the local vicinity of the ground and power planes. The diodes are the best way that I could find to keep close to the original circuit. Diodes have a reputation for being noisy, but shot noise is white and gaussian and the high frequency component would be rejected by the receiver PLL; the low frequency component is very small. Plus, any noise we get from the diodes is still better in the end than the slow risetimes with resistors. Again, there are better ways that involve more transistors; I'm keeping it simple.



Comparison of current draw at IC pin. Blue=new circuit, red=old circuit.



Comparison of voltage at output. Blue=new circuit, red=old circuit.

[1] http://www.rohm.com/products/databook/tr/pdf/2sc2412k.pdf
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