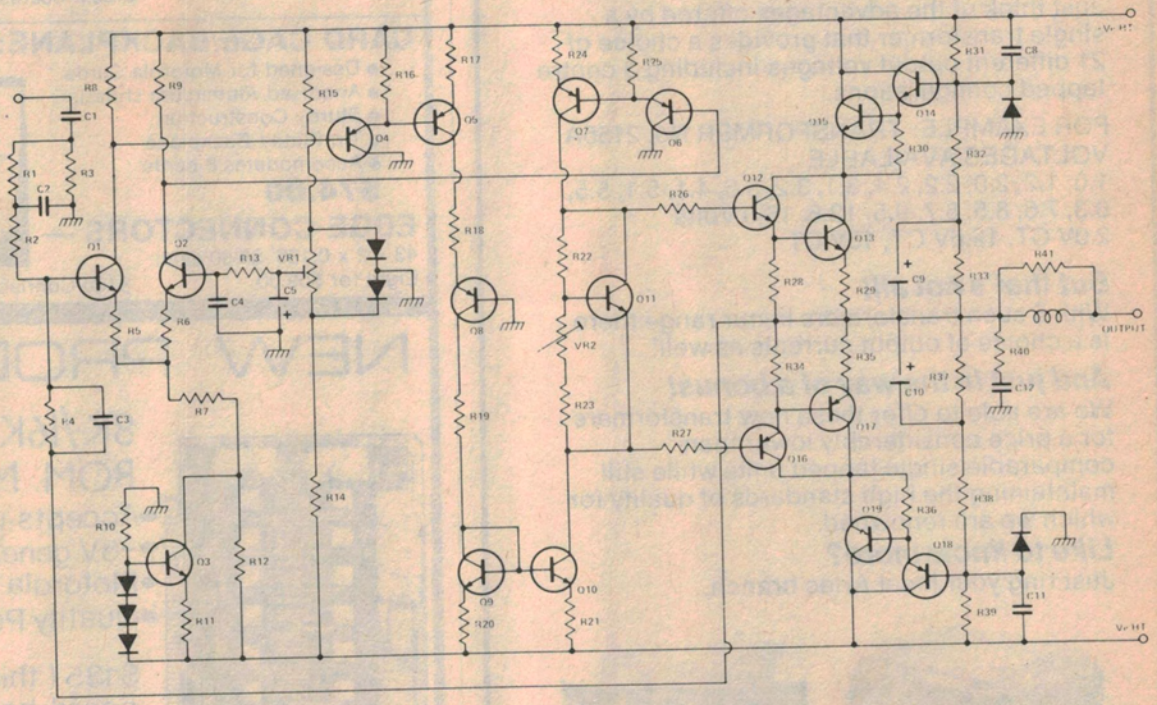

Full circuit diagram for the Lecson AP3 power amplifier design, producing around 150W.

HOW IT WORKS—Lecson AP3

Transistors Q1 and Q2 form a long-tailed pair differential amplifier with Q3 as the emitter current source. Local feedback is applied in the form of emitter resistors R5 and R6. The base of Q2, instead of being grounded, is connected to a potential divider RV1 which permits the DC offset at the output to be set to zero. The input signal to Q1 is passed through a low-pass filter (R1, C2) which sets the bandwidth to 22 kHz (i.e. below the open loop bandwidth for no TID effects). The bi-phase outputs of the long-tail pair feed a second differential amplifier Q5 and Q7. Transistor Q5 has a constant current load (Q8) whilst is terminated by a current mirror (Q9 and Q10). Transistor Q10 will always deliver the same current as transistor Q9 hence the term "Current Mirror" and the excellent symmetry and balance this stage achieves. Functionally, however, Q10 can be considered as an active load whilst Q7 is a voltage amplifier from whose collector the drive to the output stage is taken. Note that Q5 and Q7 both have local emitter feedback (R17, R24) and that both are buffered from the long-tail pair (Q4 and Q6 emitter followers).

Transistors Q12, Q13, Q16 and Q17 each form conventional Darlington emitter follower stages. Each stage is series connected to a further power transistor (Q14, Q15 and Q18, Q19 respectively) which is permanently biased ON. Their emitter potentials are determined by the ratio of the base potential dividers. This ratio was chosen such that Q13 and Q15 each has half the supply rail across them.

The whole amplifier is in the inverting mode with overall shunt feedback through R4 and C3.

This amplifier is quite fast having an open-loop bandwidth of about 27 kHz. The circuit is stable without the usual compensation capacitors within the loop. THD is low being typically (at 100 W into 8 Ohms) 0.004% at 1 kHz and 0.02% at 10 kHz. The HF distortion can be further improved by selection of transistor Q7 for a device with a low collector-base capacitance.

No conventional protection circuits are used as extremely high power transistors are fitted and these can survive a short-circuit condition in the time taken for the power supply to shut down.