Electronic Reverberation

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The second of two articles explaining the operation of electronic reverberation systems. In this article the author deals with digital and analog shift register techniques using integrated circuits.

There are currently three basic methods that can be used to provide an all electronic delay line. The first makes use of one of the properties of a filter that an electric signal takes a definite time to propagate through it. By using a filter made up of many elements, it is possible to obtain delays of the order of milliseconds over a reasonable audio bandwidth. The filter may be built from a series of L-C sections, or from a number of active sections which need no inductors. It has been said that this approach is prohibitively bulky and expensive, but modern materials and techniques have changed this, and one manufacturer uses this technique to produce a compact unit having a delay of 10ms over the audio band to 5kHz.

In the second method, the signal is first changed into digital form, the digital signals delayed by passing them through a series of shift registers, and the output of the shift register then converted back into an analog signal which is a delayed version of the input wave form.

Either pulse code modulation (PCM) or delta modulation may be used to convert the input signal into the digital form. In PCM, a brief sample is taken of the input signal at regular intervals, and then stored while the amplitude and sign of the sample is measured using a simple digital voltmeter called an encoder as illustrated in Fig 6.

The output from the encoder is a series of pulses which make up a code group representing the voltage of the sample, and usually consist of a sign pulse, and a series of pulses or absence of pulses representing the "ones" and "zeros" respectively of the binary value of the sample.

The successive groups of pulses can be combined into a single pulse stream having a uniform repetition rate, or clock rate, which will be an integral multiple of the sampling rate, and which will depend on the number of digits used in the code group. The pulse stream may be read into a chain of storage elements, so arranged that as each "1" or "0" is read in, the previous contents of that storage element is transferred into the next one in the chain.

These chains are called shift registers, and the information is shifted progressively through them under the control of the clock pulses. The information will be available at the end of the shift register after a delay of exactly "n" clock periods, where "n" is the number of stages in the shift register. Bipolar shift registers are limited to about eight or sixteen stages, but MOS devices are now readily available with 512, 1024 or 2048 stages in a single T099 or Dual-in-Line (DIL) package, so that reasonably long delays can be provided with a small number of packages.

At the output of the shift register, a digital-to-analog (D-A) converter generates a series of voltage pulses whose heights are determined by the received code groups. The pulses are passed through a low pass filter having a cut-off frequency slightly above the highest required frequencies in the input signal, to recover the original waveform. Fig 6(b) shows the "square" pulses out of the D-A converter, and the analog signal obtained after low pass filtering. Compare this output waveform with that of the input signal in (a).

The input waveform must be sampled at least twice as fast as the maximum frequency to be transmitted, and for a bandwidth of 200 Hz to 4kHz, the sampling rate will be typically 10,000 times per second. If the code group consists of 10 binary digits or "bits", ie the analog amplitude range has been divided into a total of 512 (-2^9) positive and 512 negative levels, the clock rate will be 100kHz and a single 1024 stage package will provide a delay of 10.24 ms.

Further packages can be added to increase the delay to the desired value, and shift registers containing a smaller number of stages can be used where shorter delays or finer tappings are required. Where there is more than one tapping, separate D-A converters may be used for each tap and the outputs combined in a common amplifier. The D-A converters are relatively expensive and if many taps are required it would be more economical to add the signals digitally and then use a single D-A converter. For this application the analog signals should be represented by a binary code.

A simple digital adder can be built from three type 7483 integrated circuits which will add together two 10 bit binary numbers (including the sign) in less than 80ns. The signal levels can be adjusted by multiplying the digital output from each tap by a binary number less than one, using repeated shifting and addition. (Appendix 1). Using the previous example, with a sampling rate of 10,000 per second, a period of 100us is available between samples to carry out the necessary additions. Only a single adder stage is required, and this can be time shared for the multiplication and addition of the outputs from the various taps.

A shorter shift register can be used by feeding part of the output back into the input (Fig. 5). The feedback can be in analog form by taking the output from the D-A converter, or in digital form in which case an adder and control unit can be used as above. A smoother frequency response may be obtained by taking the outputs from several tappings, combining these, and feeding the combined signal back into the input.

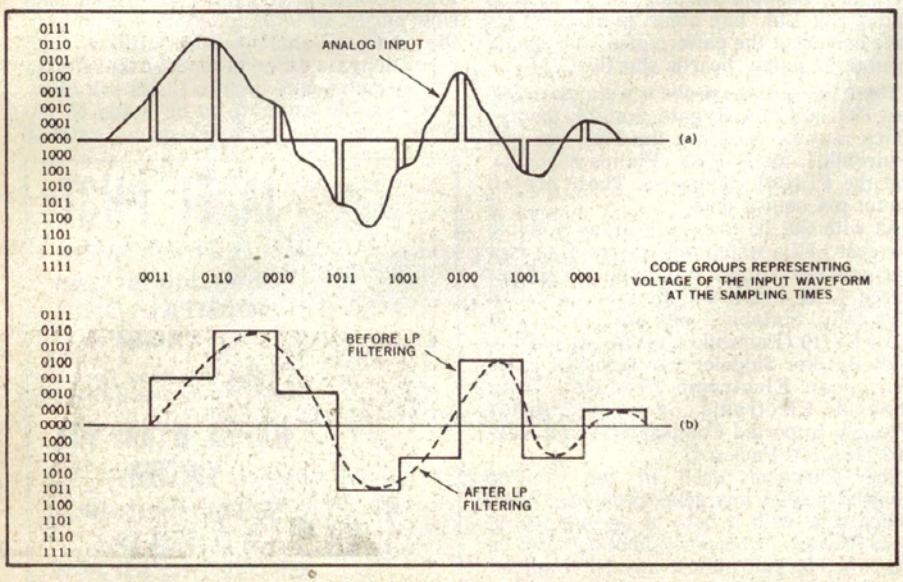

Fig 6. Digital transmission using code modulation; (a) input signal with samples, (b) decoded output before and after passing through a low pass filter.

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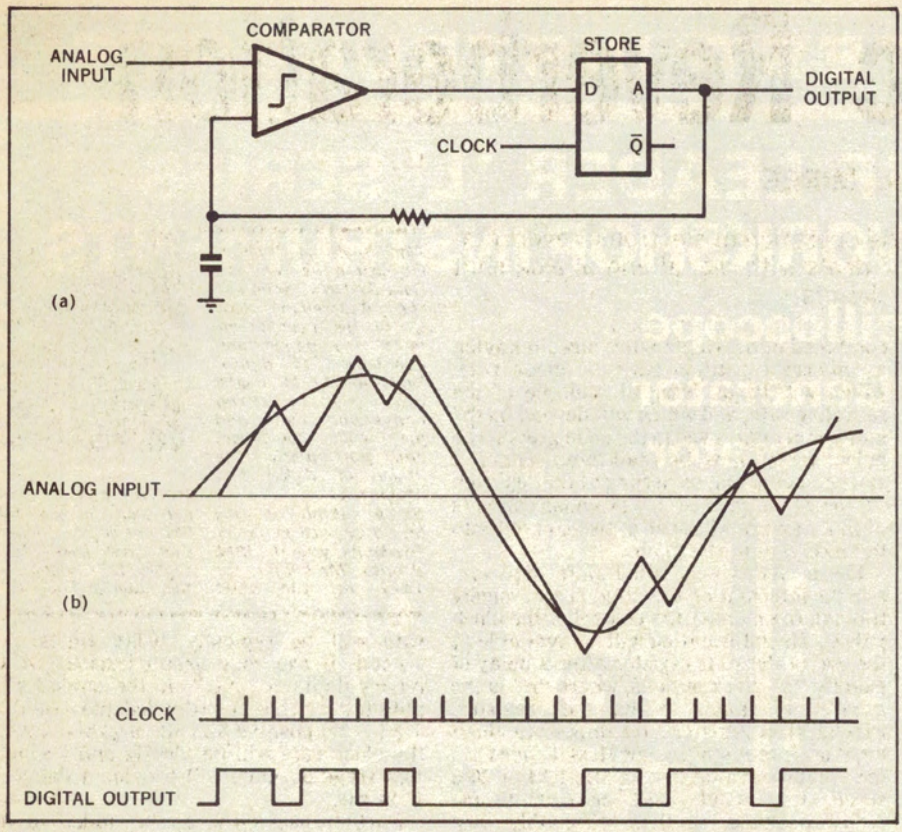

Fig 7. Digital transmission using delta modulation; (a) simple modulator, (b) waveforms.

An alternative digital approach is to use a delta-modulation encoder to generate the digital stream. The simple delta coder shown in Fig 7(a) uses a feedback loop to generate a voltage which tries to track the input waveform (Fig 7(b)). The comparator continuously compares the input signal with the feedback signal and its output goes high or low depending on which of the signals is more positive. This information is transferred to the store each clock period and is fed out to line as a series of ones or zeros. This same string of pulses is fed into the R-C network, and while a "one" is being transmitted the resistor will be connected to the positive supply and the capacitor will charge.

During a zero, the resistor will be connected to earth, and the capacitor will discharge. The time constant of R-C is made very long — about 100ms or more, so that it takes a long string of ones or zeros to fully charge or discharge the capacitor. With no input the coder will transmit alternate ones and zeros, and the capacitor will charge up to half the supply voltage.

With a simple encoder such as this, the signal can be reconverted to the analog form by using a single R-C network. Where a number of delays are required, the taps from the shift register can feed separate R-C networks, and the outputs of these combined. For some applications it may be convenient to use a single capacitor with a resistor to each tapping point on the shift register. The level of each echo can be adjusted by varying the value of the appropriate resistor.

Both the PCM and the delta-modulation system are capable of very good performance, but both introduce a new type of distortion, called quantizing distortion. The PCM encoder divides the total signal range up into a number of discrete levels. In Fig 6(a) there are a total of sixteen levels, eight positive and eight negative. A signal having any value between two successive levels will be represented by the lower of the two levels, and for a number of successive samples the output of the decoder will be a series of steps instead of a continuous wave.

For signals having a value in between the quantizing levels the output will be in error by an amount of up to the difference between successive levels. This error voltage is nearly random in nature, and sounds very much like noise. It is, however, a distortion, as its mean level is related to the signal level, and it is not present when there is no signal. The error can be made very small, by using a large number of ranges — and by decoding in such a way that the maximum error can only be plus or minus half the difference between successive levels.

For an encoder having 1024 levels (total) the error at the top of the range will produce a distortion of 0.1%. This will rise at low levels, until on the lowest step in the range it will be 50%. The total range of levels which may be represented is 54dB ($= 20 \log_{10} 512$) and at mid range (27dB) the distortion will be about 4.5%. The distortion, and dynamic range can be improved by increasing the number of levels. For instance with $2^{14} = 16{,}384$ levels, the above figures would be divided by a factor of 16. The penalty here is that the shift registers must be increased in length and more complicated and expensive encoders and decoders are required.

Delta modulation also suffers from quantizing distortion due to the error voltage between the original signal, and the feedback signal which is trying to track it. There is a further form of distortion that

occurs when the analog signal rises or falls at a rate too fast for the feedback signal to track. This generates large error signals and is known as slope overload distortion. Again, the effect of both of these can be reduced by using a higher clock frequency and the penalty is again the need to provide longer shift registers to handle the greater number of bits for the same delay.

Simple delta modulation encoders such as this have a limited dynamic range. The threshold level or the minimum signal which may be transmitted is constant at all frequencies over the band, but the maximum amplitude which may be transmitted falls at 6dB per octave due to slope overload. For a sine wave signal, the maximum slope occurs at the zero crossings. As the frequency is increased, the amplitude must be reduced to keep this slope constant. For the simple coder described, the range between maximum and minimum signal will be about 30dB at 1kHz for a 100kHz clock frequency.

The performance of both the PCM and delta modulation systems can be improved by some form of companding — i.e. compression of the analog signal before or during encoding, with a corresponding expansion during the decoding process. In PCM the output of a linear coder having 2^{12} = 4096 levels may be compressed to eight bits per sample, i.e., a reduction of one third in the number of shift register stages required, without seriously degrading the performance.

Both forms of digital system suffer from the effects of quantizing the analog signal into a number of discrete levels. An alternative approach is to sample the signal at regular intervals, but keep the samples in analog form and pass them consecutively along an analog shift register.

An analog shift register may be made from a series of sample and hold circuits as shown in Fig 8. The odd numbered stages are driven directly from the square wave clock, and the even numbered stages from the clock through an inverter. While the clock is high the voltage on each of the even numbered capacitors remains constant, while the odd numbered ones are charged (or discharged) to the voltage on the preceding one. While the clock is low the voltage on the odd numbered stages remains constant, while the even numbered ones are charged to the new value.

The chain therefore acts as a series of master-slave stages, and by analogy with the old fire fighting method where the buckets of water were passed from hand-to-hand along a chain, is sometimes called a "bucket-brigade delay line".[4] F.J.L. Sangster[5] of the Philips Research Laboratories in Eindhoven, Holland, has recently developed such a delay line in integrated circuit form.

Sangster has developed a simple but elegant solution which only needs a single transistor and capacitor for each half stage. In the circuit in Fig 9(a), the transistors are all identical, and all the capacitors have the same value. The operation starts with all capacitors charged to voltage V, except Cin which is charged to Vs1, the value of the first sample. At time t1 the base of TR1 is raised to voltage V by the clock, and this

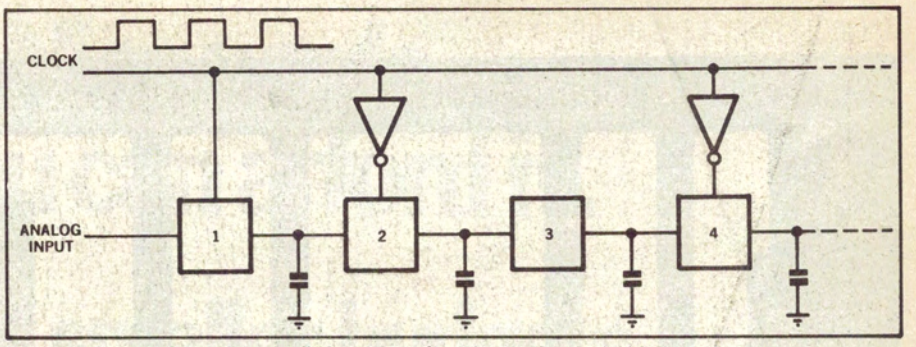

Fig 8. Analog shift register built from a series of sample and hold stages.

will add to the voltage across C1 raising the collector of TR1 2V volts above earth. Cin will charge to V volts, and as the base-emitter junction of TR2 is reversed biased, and we assume that TR1 has a very high β, the current to charge Cin must come from C1.

The net results will be that C1 will be discharged to Vs1. At time t2 clock 1 drops to zero volts and clock 2 goes to V volts, C1 will be charged to V volts and C2 discharged to Vs1. At the same time we arrange for Cin to be discharged to the next sample Vs2. In successive clock periods, the samples will propagate down the line to the right, which is the desired result. The input voltage must always be positive, so that a suitable DC bias must be added to the input signal.

There are several minor problems in this approach, firstly the capacitors do not charge to the full value V of the clock voltage, but to a value of about 400 to 600mV less due to the forward drop across the base-emitter junctions. Secondly, the base-emitter current, although small, cannot be ignored, and the effect of both of these is to cause a small loss of signal in each stage and this loss becomes greater at higher frequencies. The loss can be overcome by including an amplifier stage at regular intervals, but the high frequency loss sets an upper limit to the operation of the system.

One of the advantages of Sangster's approach is that the capacitors need not all be exactly equal in value. What is really transferred between stages is a charge, not a voltage, and as the charge is related to the product of the voltage and the capacitance, it is only necessary for the input and output capacitors to be the same value for an overall unity gain. The capacitors need only be very small, a few pF is sufficient, and these may be easily included in the integrated circuit.

A shift register built to this design will

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operate at clock rates up to 30 MHz, so that it may be used to transmit signals up to 15MHz and is very useful as a variable delay line in TV applications. The lowest clock rate at which it can work is limited by leakage currents in the transistors to a few tens of kHz.

A similar design has been built using MOS techniques, which overcomes the problems of the base-emitter current in the transistors. The MOS version has a lower maximum clock rate, and can be used over a range of 100Hz to 3MHz. It can handle higher voltages than the bipolar version, and is particularly suited to audio applications.

All of the techniques described, both mechanical and electronic, have some shortcomings, and no one approach will be best for all applications. The most suitable method will depend on whether reverberation or separate echoes are required, and the minimum bandwidth, distortion and signal to noise ratio which may be tolerated, together with the cost of providing the system.

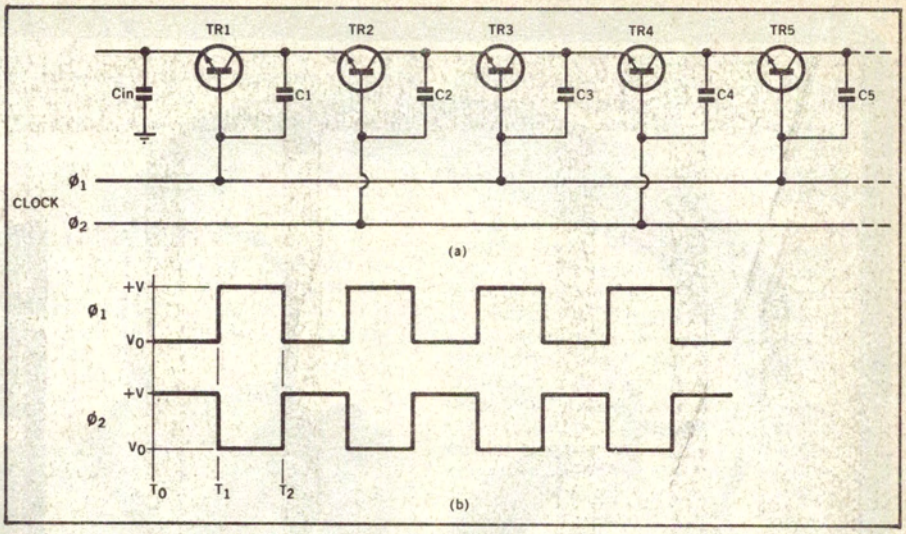


Fig 9. (a) "Bucket Brigade" analog delay line; (b) clock waveforms and timing.

APPENDIX

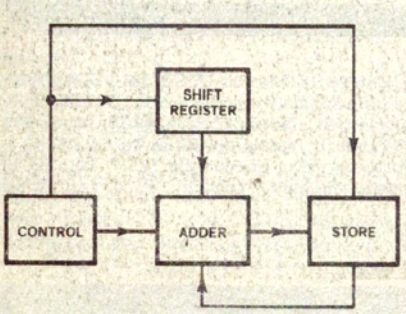
Binary Multiplication

To multiply 1010 (—10)
by 0.1011 (— 11/16)

```
  1010
   0.01011
 -------
  101.0
   00.00
    1.010
    0.1010
 -------
  110.111
```

∴ 1010 x 0.1011 = 6⅞

Store the value 1010 in the shift register, and the multiplier 0.1011 in the control, clear the store (set to 0). Taking the multiplier one digit at a time, (a) Add the value of the Multiplicand to the present value in the store, and store, if the digit is a one, or (b) do nothing if a zero, then move the contents of the shift register one place to the right. Continue the adding and shifting till all digits have been used.



Earlier in these articles it was shown that to provide a complete simulation of the reverberation characteristics of a particular room, it was necessary to use a separate reverberation generator for each frequency band. This approach would only be necessary for very accurate work, and for many purposes an adequate reverberation effect may be obtained by assuming that the reverberation time is constant over the band from say 200Hz to 4.5kHz and drops to zero at other frequencies, so that only a single reverberation channel is required.

For home use, the spring type units are the cheapest, ranging from $5 to $20 for the unit, and need little auxiliary equipment. The acoustic line approach would also be in the same order of cost, and both are capable of good results if only reverberation is required. The tape recorder is capable of excellent results and the costs will range from $100 for a simple machine with a fixed delay to $5000 or more for a machine with several adjustable heads and wow and flutter performance suitable for professional applications.

The costs of integrated circuits are still falling, and digital shift registers can be bought for 1 to 2 cents per stage, so that a delay unit using a 250kHz clock rate will cost between $2.50 and $5.00 per millisecond. There are now commercially available A — D and D — A converters using a 10 bit code, and which operate at 25,000 samples per second. A pair of these plus a suitable sample and hold unit costs about $200. A delta modulation system having a similar performance will be about the same order of cost.

One of the most promising approaches to date is Philips' M31 analog shift register. Amperex Electronic Corporation recently announced the development of the M31, a thirty-two stage analog shift register which they expected would sell in the USA for less than $10 each. Although described as a thirty-two stage register, two stages are required for each master-slave pair and each M31 introduces sixteen clock periods delay. It is understood that these integrated circuits are made by Philips of Eindoven and only a few laboratory made prototypes have been available so far for evaluation.

At this stage there is no guarantee that the M31 will go into commercial production. Based on the Amperex expected price of $10 per unit, and using a clock rate of 10kHz, the cost will be almost $6 per millisecond of delays for a signal bandwidth of 4kHz. The method is so promising that it is likely that the M31 or an integrated circuit based on it will become readily available in the next year or so, and it could be expected that the price will drop as the demand rises.

With present day costs, the use of the all electronic system is likely to be restricted to the recording studio, and the serious amateur. It has been predicted that the costs of shift registers and other forms of memory will fall by a factor of ten by 1975, and therefore it is more than likely that suitable electronic reverberation equipment will become readily available at a reasonable price in the next few years.

The permission of the Senior Assistant Director-General, Australian Post Office Research Laboratories, to publish this article is hereby acknowledged.

REFERENCES

4. J. M. L. Janssen, Discontinuous Low Frequency Delay Line with Continuous Variable Delay," Nature, 169, 1952, pp. 148-149..
5. F. L. J. Sangster, "The Bucket Brigade Delay Line — A Shift Register for Analogue Signals," Philips Technical Review, Vol 31, N0 4, 1970, pp 97-110.
6. Electronic Design Vol 19, N0 24, Nov 25, P 34.