# Electronic organ tone system — 2

## Frequency generation and keying matrix

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The previous article gave details of the reference generator and its construction on a Veroboard. This month's article describes the gate cards which are based on specially designed printed circuit boards.

One gate card is needed for each of the 12 notes in the scale. The d.c. signals from the playing keys are brought in, either directly or via the coupling circuits, through edge connections at the front. Output connections are made via the rear edge-connector which also carries supply rails, the reference signal and, if used, the vibrato signal.

Outputs of, for example, the C card are square-wave signals at multiples of 32.7Hz, the fundamental of the lowest C used. These are collected onto a set of square-wave buses (SQB) which are common to all 12 gate cards and form the inputs to the three filter cards. There are seven sinewave harmonic pitches for each department, 21 in all, which are the outputs of the filter cards. To ease filter design, the fundamental SQBs are each divided into three sections, and the rest into two, so that in all there are 45 gate card outputs. The cards also provide a spare SQB for each department so that there are a further six output lines which can be used for the various options to be described later.

The functions of each gate card are thus the local generation of the required frequencies, tied to the incoming reference, and the gating of these selectively to the square-wave buses under the control of key signals. In addition, the cards carry circuits for shaping the keying envelope, and can accept a signal for vibrato.

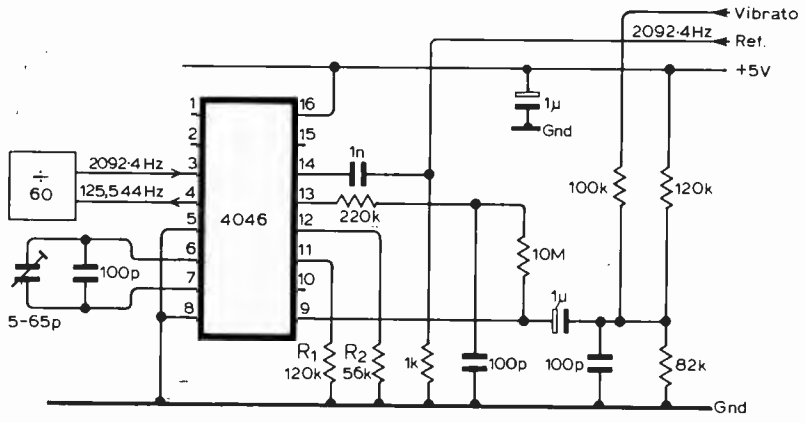



**Fig. 10.** *Phase lock loop for C card. This circuit multiplies the reference frequency by 60.*

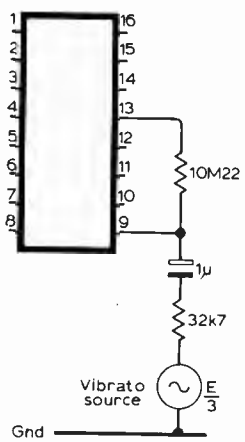
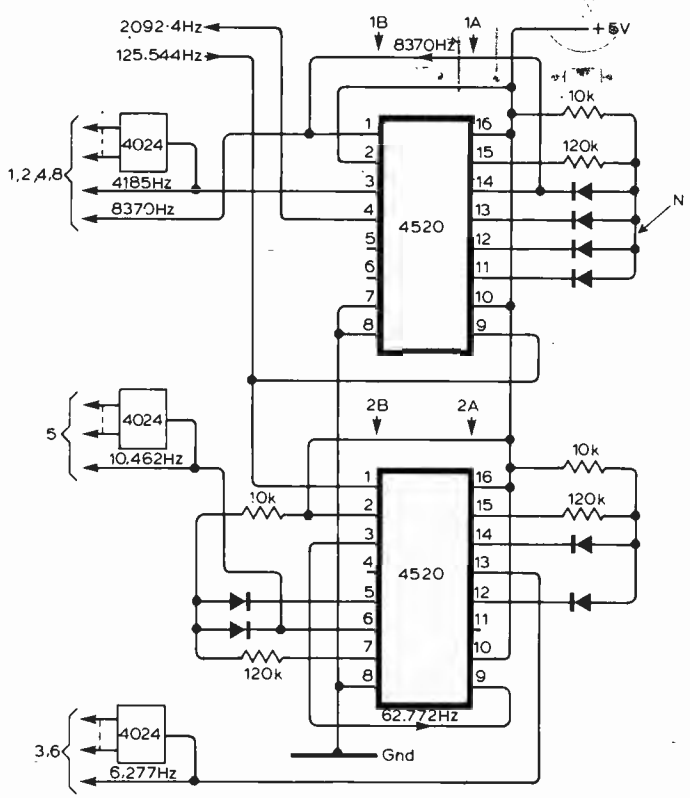



**Fig. 11.** *Feedback loop of p.l.l. at low frequencies.*

**Fig. 12.** *Frequency derivation on C Card. All diodes are general purpose devices such as the 1N4148.*




### Frequency generation

The circuit in Fig. 10 shows how a 4046 p.l.l. is used to derive a frequency of 60 times the reference. Except for $R_1$ and $R_2$, which decrease with increasing frequency, this circuit applies to all 12 gate cards. The reference input at pin 14 is a.c. coupled, and the 1kΩ resistor,

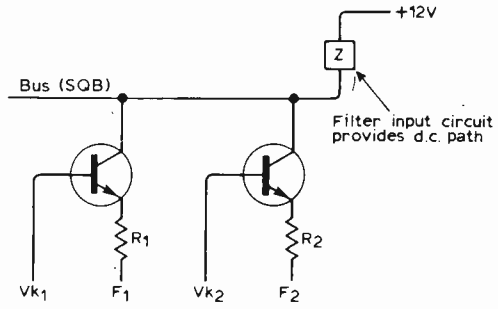



**Fig. 13.** *Common-base transistor gates. Input signals $F_1$ and $F_2$ are square-wave divider outputs.*

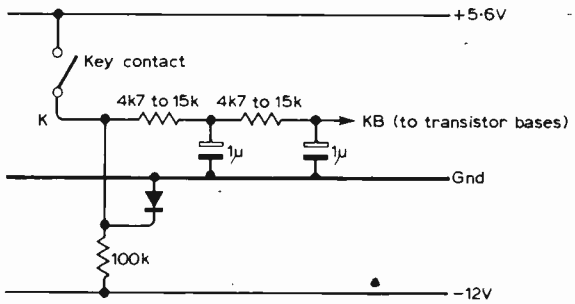



**Fig. 14.** *Keying circuit. The double integrating network is used to control a d.c. output component by shaping the keying envelope.*

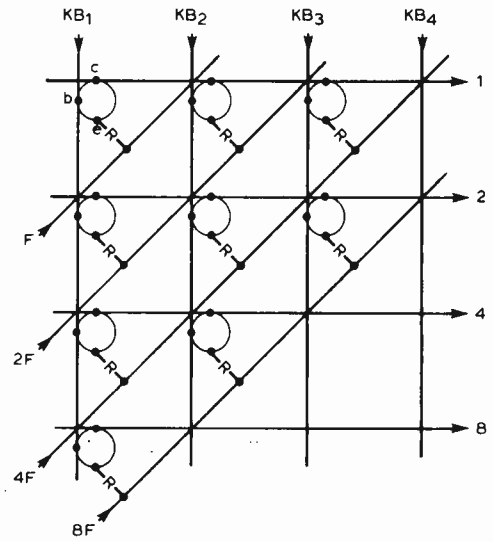
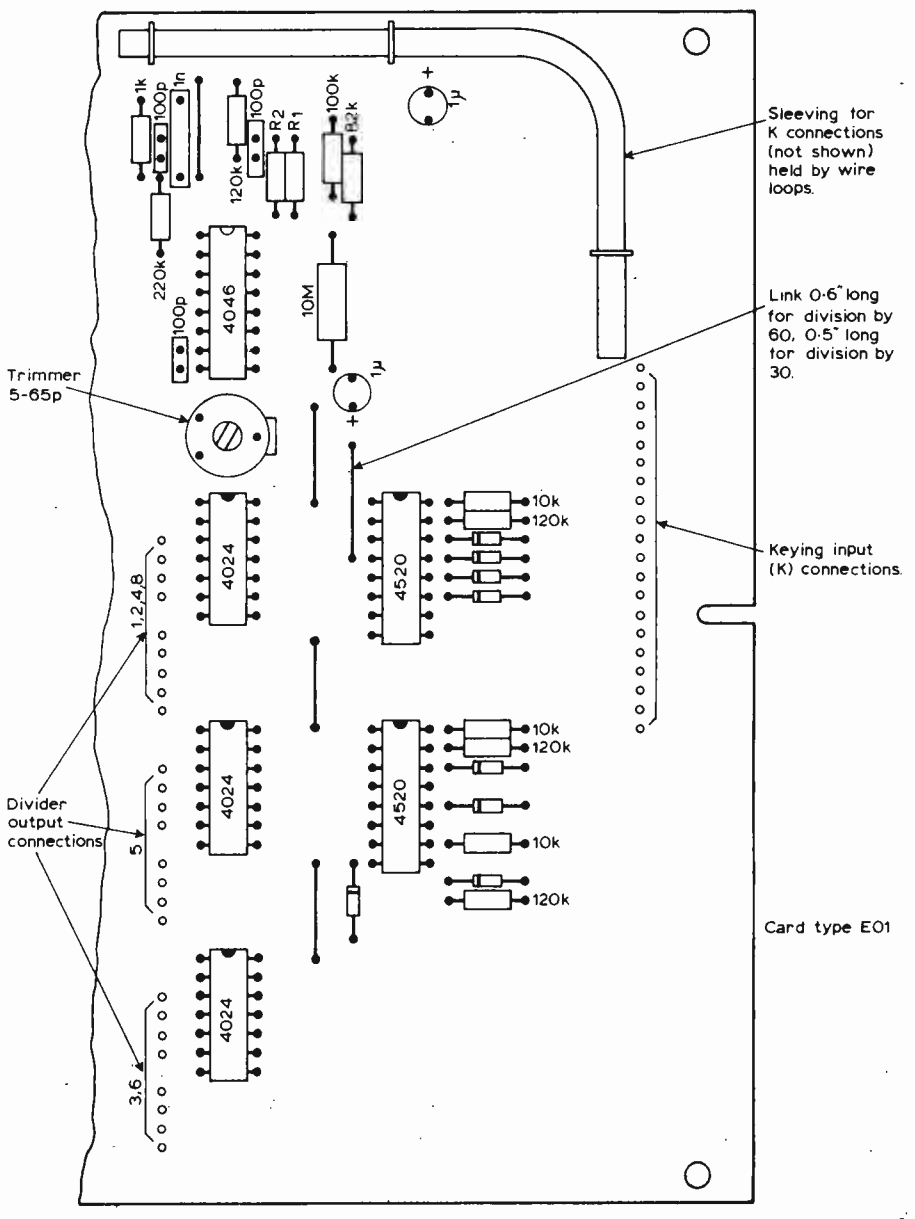



**Fig. 15.** *Portion of the three-way matrix. This layout is roughly the same as the p.c.b. viewed from below.*

**Fig. 16.** *Component layout of the frequency generating section on EO1 cards.*




together with the 22kΩ buffer in Fig. 4 control the reference level. A divider is connected between the v.c.o. output and the comparator input, and the digital phase-comparator output at pin 13 is used for control. This comparator has a switching action which reduces the settling time for a given feedback time constant. The control signal at pin 9 must have an in-phase component for stability, which in turn makes h.f. filtering desirable to minimise output jitter. Fig. 11 shows the circuit at l.f. where the lower network is the parallel combination of 82kΩ, 120kΩ and 100kΩ. Returning the capacitor to about 2V reduces the charging time at switch-on.

When a vibrato signal of 4 to 8Hz and amplitude E is applied, the amplitude at pin 9 is roughly E/3. The frequency deviations cause an antiphase square-wave signal at pin 13 which swings between about +1.25 and +3.75V. Except for very low values of E, this has negligible effect on the extent of frequency modulation. However, the mean voltage at pin 9, if not initially 2.5V, will tend to this figure, assuming symmetrical modulation, so that the mean frequency will drift slightly, though the original frequency will always lie within the modulation range. The trimmer allows initial setting-up for 2.5V. Generation of the vibrato signals is considered in a later article. Table 4 shows some frequencies used on the 12 gate cards.

## Frequency dividers

In Fig. 12, each 4520 i.c., which contains two independent 4-stage dividers, has

the enable inputs connected to the positive supply rail. Non-binary counts are achieved by premature reset. Counter 1A, for example, divides its input at pin 9 by 15 because the four outputs represent counts of 1, 2, 4 and 8. The diode AND connection allows line N to go high on reaching the count of 1 + 2 + 4 + 8, i.e. 15. The 120kΩ resistor in series with the reset input at pin 15, together with the input capacitance, provides a short delay to avoid switching ambiguities. The 1 output appears eight times in the cycle, the last time briefly. The 8 output has a frequency of 60ref/15 i.e. 4ref, which in this case is 8370Hz, and a mark to space ratio of approximately 7/8.

Counter 1B is used without reset, pin 7 grounded, so that the overall division to pin 4 is 60, as required for Fig. 10. The pin 3 output, at 2ref, is taken to a 4024 7-stage counter so that a total of 9 octavely-related C frequencies, the unisons, are available down to 32.7Hz.

Counter 2B is connected to divide by 12, 8 + 4, and produces an output of 5ref, again extended by a 4024 to give eight 5th harmonic pitches. As this is an even division, the 1 output at pin 3 is a square wave at 30ref, which is divided by 10 in counter 2A. Here the 4 output has the same frequency of 3ref as the 8 output, but a mark to space ratio of nearer unity. This output is used with another 4024 to provide eight 3rd and 6th harmonic pitches.

As already noted, the lowest pedal frequency is 32.7Hz, and the lowest manual is 65.4Hz. These correspond to 4ref/256 and 4ref/128 respectively. The 3rd harmonic of 32.7Hz, 5⅓ft, is 3ref/64, and the 5th, 3⅕ft is 5ref/64, so that in the basic system, neither of these buses requires the lowest output from its 4024 i.c.

The fundamental of the highest manual key, CK6, is 2093Hz, therefore the highest unison at 4ref, 8370Hz, provides only the 4th harmonic at this level. A frequency of 8370Hz is the normal limit for the fundamental of an organ pipe. With the next highest key, BK5, 4ref at 15,794Hz would provide the 8th harmonic but, as table 5 shows, the various pitches are discontinued at about 10kHz, and at CK6, the 5th is the highest provided.

Although CK6 is the highest key, the gate cards carry K6 circuits up to G, to operate with octave couplers if used. The frequency limits are noted in table 5. The highest pedal key is GK3 which has a fundamental of 196Hz and an 8th harmonic at 1568Hz. A complete K4 octave is provided for the pedal department, which extends to 3135Hz.

## Alternative reference set

As noted in the previous article, the clock input to the multiple divider may be at various frequencies. For example, at 1MHz instead of 943.7kHz, the C reference is 4186Hz as shown in table 2. This is accommodated by taking the comparator signal from pin 3 of counter

**Table 4. Some gate-card frequencies using the tunable reference source set to zero beat**

| Note | Nominal ref frequency (Hz) | Actual ref frequency (Hz) | 60 ref | 4 ref | 5 ref | 3 ref |
|---|---|---|---|---|---|---|
| C | 2093.0 | 2092.4 | 125,544 | 8370 | 10,462 | 6,277 |
| C' | 2217.5 | 2215.2 | 132,912 | 8861 | (11,076) | 6,646 |
| D | 2349.3 | 2347.4 | 140,844 | 9390 | (11,737) | 7,042 |
| D' | 2489.0 | 2489.9 | 149,394 | 9960 | (12,450) | 7,460 |
| E | 2637.0 | 2635.9 | 158,154 | 10,544 | (13,180) | 7,908 |
| F | 2793.8 | 2791.9 | 167,514 | (11,168) | (13,960) | 8,376 |
| F' | 2960.0 | 2958.2 | 177,492 | (11,833) | (14,791) | 8,875 |
| G | 3136.0 | 3135.1 | 188,106 | (12,540) | (15,676) | 9,405 |
| G' | 3322.4 | 3322.8 | 199,368 | (13,291) | (16,614) | (9,968) |
| A | 3520.0 | 3521.1 | 211,266 | (14,084) | (17,606) | (10,563) |
| A' | 3729.3 | 3729.9 | 223,794 | (14,920) | (18,650) | (11,190) |
| B | 3951.1 | 3948.4 | 236,904 | (15,794) | (19,742) | (11,845) |

The brackets indicate frequencies not used directly.

**Table 5. Upper frequency limits**

| Harmonic no. | 1 | 2 | 3 | 4 | 5 | 6 | 8 |
|---|---|---|---|---|---|---|---|
| Highest key | GK6 | GK6 | GK6 | EK6 | CK6 | GK5 | EK5 |
| Frequency | 3135 | 6270 | 9405 | 10,544 | 10,462 | 9,405 | 10,544 |

EK6 and GK6 do not represent actual keys, but circuits are provided up to GK6 for use with octave coupling.

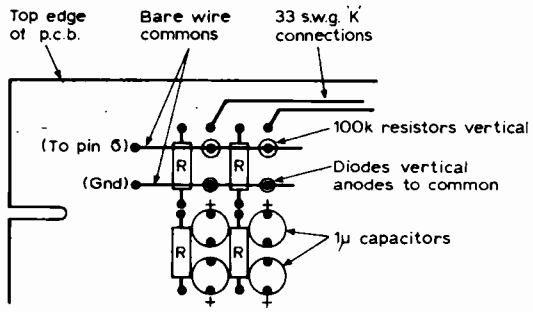
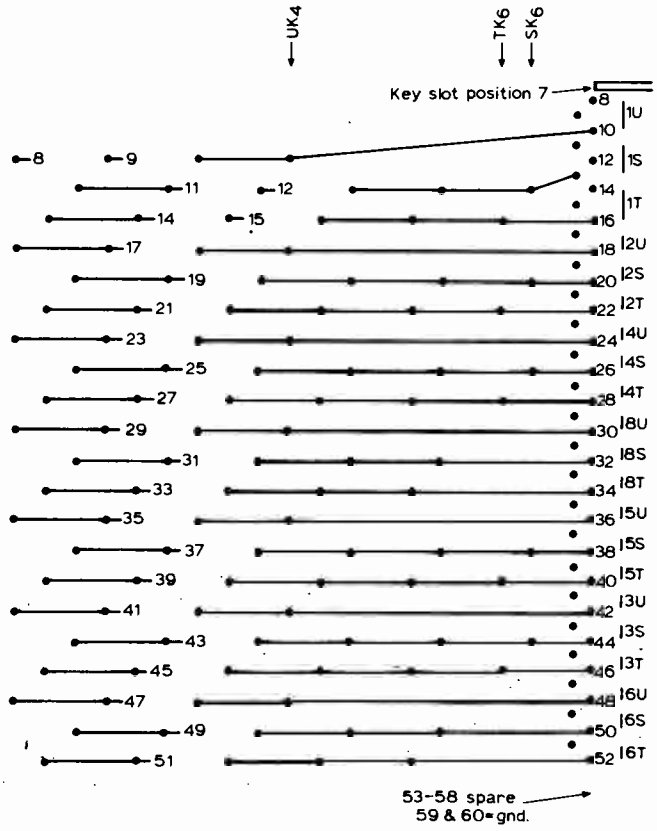



**Fig. 17.** *Keying circuit layout from component side, showing two circuits. Except for the value of R, all of the circuits are identical. The common wire connections bend down to enter the p.c.b. on the left.*

**Fig. 18.** *Card C square-wave bus output connections on copper side. This pattern also applies to cards C' to G, except for fewer gates in the TK6 and SK6 columns. Spare gate positions at the bottom are not shown.*



1B in Fig. 12, rather than pin 4, and so multiplying the reference by 30 instead of 60. This selection is by a wire link on the p.c.b. see Fig. 16.

## Keying

Because a large number of gates are needed, a minimum component count per gate is desirable, and the common-base transistor configuration which was chosen is shown in Fig. 13. Input signals $F_1$ and $F_2$ are 5V square-wave divider outputs. When the base voltage of one of the transistors, e.g. $Vk_1$, is zero, it is held off. As this voltage is increased, the transistor starts to conduct during the low excursions of $F_1$ and a current of roughly $(Vk_1-0.6)/R_1$ flows out of the emitter. When $Vk_1$ is about 5.6V, the transistor ceases to cut off during the $F_1$ cycle and the output current swing at the collector is at a maximum of $5/R_1$, with a mean level of $2.5/R_1$ for a unity mark to space ratio. A further increase of $Vk_1$ merely raise the mean current without increasing the a.c. component.

The high output resistance of the common-base connection means that, with practical values of filter input impedance, the contribution of each gate is more or less independent of the others, and almost entirely determined by its input resistor. The base provides a low-current input for the keying signal and, if decoupled to ground, isolates the input and output. The main cause of breakthrough with the gate off, is emitter-collector capacitance, but for the suggested BC548C transistor this is less than 0.2pF.

Although the common-base configuration has advantages over the usual diode gate, it does have a drawback in common with other unbalanced gates, of the d.c. output component. If switched directly by the key, there would be an intolerable thump at the start and finish of a note, especially as the following filters must be low-pass. This thump is controlled by shaping the keying envelope with a double-integrating circuit as shown in Fig. 14. The time constants are graded over the frequency range. A 100kΩ pull-down resistor produces a turn-off time similar to the attack time, and the voltage at K is limited by the diode.

## Amplitude control

Reducing the direct keying voltage below 5.6V provides one means of reducing the volume of a complete department, without using controls in the signal path, and can be used for expression pedals and/or switchable departmental balance. A square waveform, as used here, is the only type which can be controlled in this way without affecting the harmonic spectrum.

## Keying matrix

With provision for coupling, there are 68 keying circuits for each manual department, and 32 + 12 for the pedal. Thus, there are in all 180 of the circuits in Fig. 14 with 16 on each card C to G, and 13 each on G' to B.

Each KB signal controls seven gates, one for each harmonic pitch, except where the higher harmonics are discontinued at the top end. Every manual SQB set collects the outputs of up to 68 gates and similarly, each pedal SQB set collects the outputs of up to 44 gates. The generated frequencies on a gate card may feed one or more gates because, for example, the fundamental of C6 is the 2nd harmonic of C5, the 4th harmonic of C4, and the 8th of C3.

The required interconnection pattern using a three-way matrix, is shown in Fig. 15. Keying circuits, not shown, are at the top, and their KB outputs, as printed tracks, run vertically to the transistor bases. Input signals at frequencies $F_1$, $F_2$, etc., are connected by wires on the component side, and the input resistors project upwards from the board with their lower ends connected to the emitters by printed track. The collector leads pass through holes and are connected below the board by wire to form the buses 1, 2, 4, etc. This layout minimises stray capacitance across the gates. A suitable wire is 33 s.w.g. Kynar insulated, as used for wire-wrapping.

## Component layout

The EO1 board carries connector pads on both of its vertical edges, 24 at the input end and 59 at the output end. The frequency-generating components shown in Fig. 16 are towards the input side, separated from the matrix area by a broad vertical ground track.

The board also carries tracks for an additional p.l.l., and for three further i.cs, associated with options to be described later. The keying components mount along the top of the matrix area and, as shown in Fig. 17, the 100kΩ resistors and diodes are mounted on end with overhead wires which terminate in the left of the board. Connections K to the input pads are made in wire starting with UK1 to position 10, TK1 to 11, and so on leaving positions 1 to 9 unused. This differs from Figs. 22 and 23, but is suggested to simplify one of the options described later. On cards with only 13 keying inputs, G' to B, positions 19, 24, 25 (UK4, TK6 and SK6) will also be unused.

**Fig. 19.** *Card output connections for G' to B. Connection on pads 25 to 52 follow the pattern of Fig. 18, except that there are no gates in columns UK4, TK6 and SK6.*

## Matrix area

As already mentioned, only the base and emitter leads are soldered to p.c.b. tracks, and the collector connections are made with wire as shown in Figs. 18 and 19. The output edge connections finish at oval pads indicated by the numbered dots at the right.

The labelling at the far right identifies the SQB by harmonic number and department. For example, 1U is the pedal fundamental, 2T is the great 2nd harmonic, and so on. The low, middle, where used, and high sections of each SQB are connected in sequence so that pad 8 is 1UL, pad 9 is 1UM, and pad 10 is 1UH, pad 21 is 2TL, pad 22 is 2TH, etc. Labelling is primarily for descriptive purposes and the connections are straightforward. The staggered rows of dots represent the collector leads, and the short rows are associated with the pedal buses.

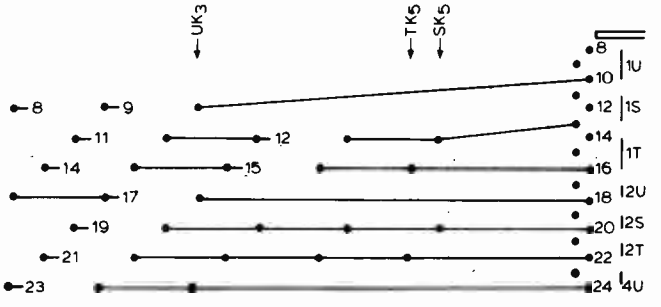
Each horizontal rectangle in Fig. 20 represents a gate transistor and its vertically mounted input resistor, $R_n$. The upper ends of the resistors are soldered to the wire signal buses which run diagnonally. The divider output connection points of Fig. 16 are indicated at the right, and connections from these to the signal buses are made on the component side with wire.

Values of $R_n$ vary with frequency to produce, in conjunction with the filter response, a predetermined amplitude/frequency characteristic, which will be described in a later article. Choosing appropriate filter parameters minimises the variety of values on any one gate card.

## Assembly and testing

For the output connections of Figs. 17 and 18, where two or more collectors are joined, wire is stripped to length and soldered to the leftmost position. A small blob of solder is deposited on each collector lead to the right, and the wire is then held tight and soldered to each lead and finally to the output pad. To suit the suggested rack spacing, the component leads must not project more than 4½mm from the underside of the p.c.b.

It is convenient to first connect the



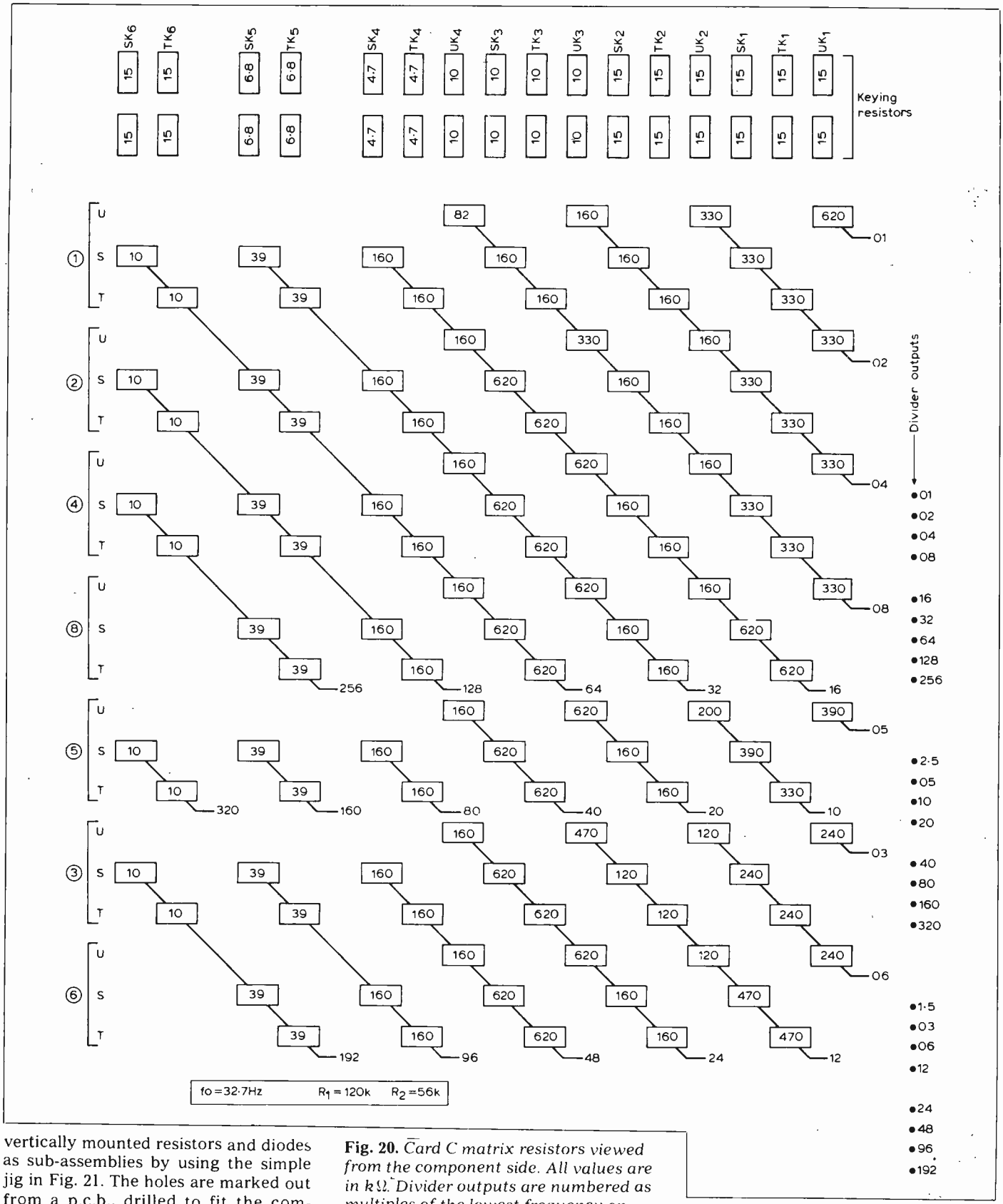



**Fig. 20.** *Card C matrix resistors viewed from the component side. All values are in kΩ. Divider outputs are numbered as multiples of the lowest frequency on the card. Harmonic numbers are in circles. Pedal harmonics are at half the manual frequencies. The lowest three rows of the matrix, which are not shown, are spares.*

vertically mounted resistors and diodes as sub-assemblies by using the simple jig in Fig. 21. The holes are marked out from a p.c.b., drilled to fit the components, and opened out at the top for easier soldering. Leads at the p.c.b. ends of the components are cut to a uniform short length and, after insertion in the jig, their upper leads are soldered to a straightened length of bare wire laid along the top. The jig and cutting dimensions should give a maximum projection above the board of 14mm.

It is recommended that the area in Fig. 16 is completed and tested first, which requires +5V on connector 3, ground on 59 and 60, and the appropriate reference on connector 4. The vibrato connection should be substituted by a 1μF capacitor to ground. A 1kΩ resistor temporarily in the 5V lead should not drop more than about 2V unless there is a fault, in which case it should prevent damage. Divider outputs should be checked with an oscillograph and frequency meter if possible. The trimmer should be set to give 2.5V at the lower end of the 10MΩ resistor.

*To be continued.*

**Fig. 21.** *Section of assembly jig constructed from two pieces of hardwood.*