SECTION 7-7

Simulation, Breadboarding and Prototyping

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In this final section of the chapter, the practical aspects of assembling hardware for op amp and other analog functions are brought to play. Various experimental techniques are useful towards verifying the integrity of a design. These include electronic *analog circuit simulation* programs, to be used with (but not to the exclusion of) the allied lab processes of *breadboarding* and *prototyping*.

Analog Circuit Simulation

In the past decade, circuit simulation has taken on an increasingly important role within analog circuit design. The most popular simulation tool for this is SPICE, which is available in multiple forms for various computer platforms (see References 1 and 2). However, to achieve meaningful simulation results, designers need accurate models of many system components. The most critical of these are realistic models for ICs, the active devices that drive modern designs. In the early 1990s, Analog Devices developed an advanced op amp SPICE model, which is, in fact, still in use today (see References 3 and 4). Within this innovative open amplifier architecture, gain and phase response can be fully modeled, enabling designers to accurately predict ac, dc, and transient performance behavior. This modeling methodology has also been extended to include other devices such as in amps, voltage references, and analog multipliers.

Figure 7-120 lists some major SPICE simulation objectives. The popularity of SPICE simulation has led to many op amp macromodel releases, which (ideally) software-mimic amplifier electrical performance. With numerous models available, several confusions are possible. There may be uncertainty as to what is/isn't modeled, plus a basic question of *model accuracy*. All of these points are important, in order to place confidence in simulation results. So, *verification* of a model is important, checking it by comparison to the actual device performance conditions, before trusting it for serious designs.

- Understand Realistic Simulation Goals
- Evaluate Available Models Accordingly
- Know the Capabilities for Each Competing Op Amp Model
- Following Simulation, *Breadboarding is Always Desirable and Necessary*

Figure 7-120: Used wisely, simulation is a powerful design tool

Of course, a successful first design step using an accurate op amp model by itself doesn't necessarily guarantee totally valid simulations. A simulation based on incomplete information has limited value. All parts of a target circuit should be modeled, including the surrounding passive components, various parasitic effects, and temperature changes. Then, the circuit needs to be verified in the lab by breadboarding and prototyping. A breadboard circuit is a quickly executed mockup of a circuit design using a semi-permanent lab platform, i.e., one that is in less than final physical form. It is intended to show real performance, but without the total physical environment. A good breadboard can often reveal behavior not predicted by SPICE, either because

of an incomplete model, external circuit parasitics, or numerous other reasons. However, by using SPICE along with intelligent breadboarding techniques, a circuit can be efficiently and quickly designed with reasonably good assurance of working properly on a prototype version, or even a final PCB. The following prototype phase is just one step removed from a final PCB, and may in fact be an actual test PCB, with nearly all design components incorporated, and with close to full performance.

The breadboard/prototype design steps are closely allied to simulation, usually following it in the overall design process. These are more fully discussed in subsequent sections.

Macromodel versus Micromodel

The distinction between *macromodel* and *micromodel* is often unclear. A micromodel uses the actual *transistor level* and other SPICE models of an IC device, with all active and passive parts fully characterized according to the manufacturing process. In differentiating this type of model from a macromodel, some authors use the term *device level model* to describe the resulting overall op amp model (see Reference 5). Typically, a micromodel is used in the actual design process of an IC.

A macromodel takes another route in emulating op amp performance. Taking into consideration final device performance, it uses ideal native SPICE elements to model observed behavior—as many as necessary. In developing a macromodel, a real device is measured in terms of lab and data sheet performance, and the macromodel is adjusted to match this behavior. Some aspects of performance may be sacrificed in doing this. Figure 7-121 compares the major pros and cons between macromodels and micromodels.

	METHODOLOGY	ADVANTAGES	DISADVANTAGES
MACROMODEL	Ideal Elements Model Device Behavior	Fast Simulation Time, Easily Modified	May Not Model All Characteristics
MICROMODEL	Fully Characterized Transistor Level Circuit	Most Complete Model	Slow Simulation, Convergence Difficulty, Nonavailability

Figure 7-121: Differentiating the Macromodel and Micromodel

There are advantages and disadvantages to both approaches. A micromodel can give a complete and accurate model of op amp circuit behavior under almost all conditions. But, because of a large number of transistors and diodes with nonlinear junctions, simulation time is very long. Of course, manufacturers are also reluctant to release such models, since they contain proprietary information. And, even though all transistors may be included, this isn't a guarantee of total accuracy, as the transistor models themselves don't cover all operational regions precisely. Furthermore, with a high node count, SPICE can have convergence difficulties, causing a failed simulation. This point would make a micromodel virtually useless for multiple amplifier active filters, for example.

On the other hand, a carefully developed macromodel can produce both accurate results and simulation time savings. In more advanced macromodels such as the ADSpice model described, transient and ac device performance can be closely replicated. Op amp nonlinear behavior can also be included, such as output voltage and current swing limits.

However, because these macromodels are still simplifications of real devices, all nonlinearities aren't modeled. For example, not all ADSpice models include common-mode input voltage range, or noise (while

more recent ones do). Typically, in model development parameters are optimized as may be critical to the intended application; for example, ac and transient response. Including every possible characteristic could lead to cumbersome macromodels that may even have convergence problems. Thus, ADSpice macromodels include those op amp behavior characteristics critical to intended performance for normal operating conditions, but not necessarily all nonlinear behavior.

The ADSpice Op Amp Macromodels

The basic ADSpice model was developed as an op amp macromodeling advance, and as an improved design tool for more accurate application circuit simulations. Since being introduced in 1990, it has become a standard op amp macromodel topology, as evidenced by industry adoption of the frequency shaping concepts (see References 6 and 7).

Prior to about 1990, a dominant op amp model architecture was the Boyle model (see Reference 8). This macromodel, developed in the early 70s, cannot accurately model higher speed amplifiers. The primary reason for this is that it has limited frequency shaping ability—only two poles and no zeroes. In contrast, the ADSpice model topology has a flexible and open architecture, allowing virtually unlimited pole and zero frequency shaping stages to be cascaded. This key difference provides much more accurate ac and transient response, vis-à-vis the more simplistic Boyle model topology.

An ADSpice model is comprised of three main portions, described as follows. The first of these is a combined input and gain stage, which will include transistor models as appropriate to the device being modeled (NPN or PNP bipolar, JFET, MOSFET, and so forth). Next are the synthetic pole and zero stages, which are comprised of ideal SPICE native elements. There may be only a few of these or there may be many, dependent on the complexity of the op amp's frequency response. Finally, there is an output stage, which couples the first two sections to the outside world.

Before describing these sections in detail, it is important to realize that many variations upon what is shown do in fact exist. This is due to not just differences from one op amp model to another, but also to evolutionary topology developments in op amp hardware, which in turn has led to corresponding modeling changes. For example, modern op amps often include either rail-rail output or input stages, or both. Consequently more recent developments in the ADSpice models have addressed these issues, along with corresponding model developments.

Furthermore, although the Boyle model and the original ADSpice models were designed to support *voltage feedback* op amp topologies, subsequent additions have added *current feedback* amplifier topologies. In fact, Reference 9 describes an ADSpice current feedback macromodel which appeared just shortly after the voltage feedback model of Reference 3. These current feedback macromodels are discussed in more detail next.

Input and Gain/Pole Stages

A basic ADSpice voltage feedback op amp macromodel input stage is shown in Figure 7-122. As noted, it uses what are (typically) the only transistors in the entire model, in this example the Q1-Q2 NPN pair, to the left on the diagram. These are needed to properly model an op amp's differential input stage characteristics. A basic tenet of this model topology is that this stage is designed for unity gain, by the proper choice of Q1-Q2 operating current and gain-setting resistors R3-R4 and R5-R6.

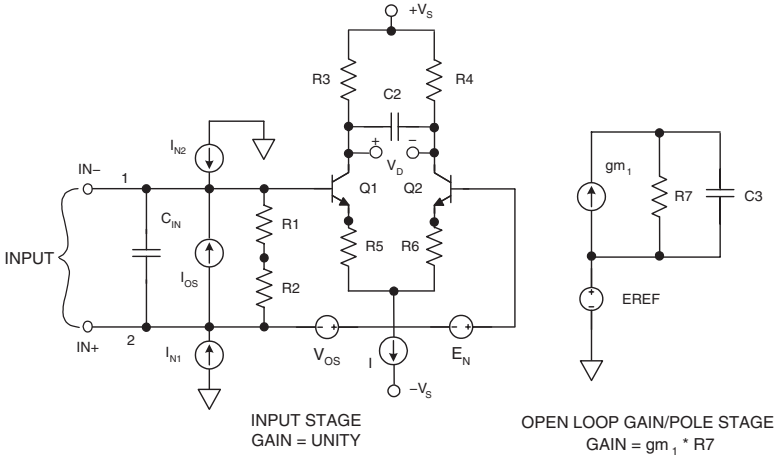


Figure 7-122: Input and gain/pole stages of ADSpice macromodel

Although this example uses NPN transistors, the input stage is easily modified to use PNP bipolars, JFET, or MOSFET devices. The rest of the input stage uses simple SPICE elements such as resistors, capacitors, and controlled sources.

The open-loop gain versus frequency characteristics of the modeled op amp is provided by the gain stage, to the right in the diagram. Here controlled source gm_1 senses the differential collector voltage V_D from the input stage, converting this voltage to a proportional current. The gm_1 output current flows in load resistor R_7, producing a single ended voltage referenced to an internal voltage, EREF. Typically, this voltage is derived as a supply voltage midpoint, and is used throughout the model.

By simply making the gm_1–R_7 product equal to the specified gain of the op amp, this stage produces the entire open-loop gain of the macromodel. This design factor means that all other model stages operate at unity gain, a feature leading to significant flexibility in adding and deleting subsequent stages. This approach allows the quick synthesis of the complex ac characteristics typical of high performance, high speed op amps. In addition, this stage also provides the dominant pole of the amplifier's ac response. The open-loop pole frequency is set by selection of capacitor C3, as noted in the diagram.

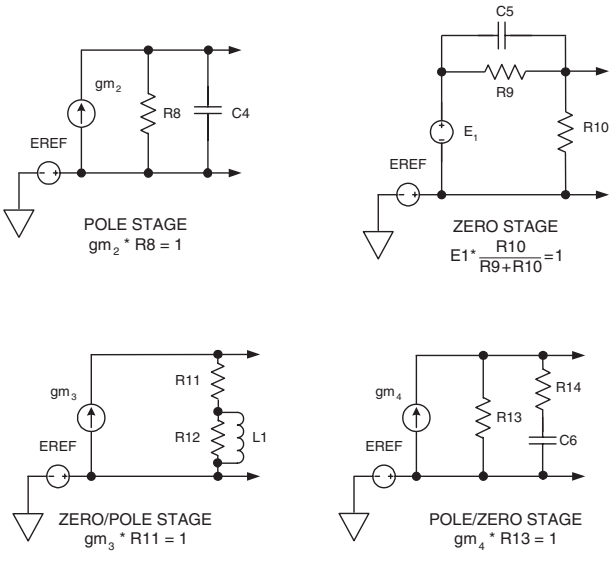


Figure 7-123: The frequency-shaping stages possible within the ADSpice model

Frequency-Shaping Stages

Following the gain stage of the macromodel is a variable but unlimited number of pole and/or zero stages which, in combination, provide frequency response shaping. Typical topologies for these stages are as shown in the Figure 7-123 diagram. The stages can be either a single pole or a single zero, or combined pole/zero or zero/pole stages. All such stages have a dc transfer gain of unity, and a given amplifier type can have all or just a few of these stages, as may be require to synthesize its response.

The pole or zero frequency is set by the combination of the resistor(s) and capacitor, or resistor(s) and inductor, as may be the case. Because an infinite number of values are possible in SPICE, choice of RC values is somewhat arbitrary, and a wide range work. Early ADSpice models used relatively high values, while later ones employ lower values to reduce noise (described in more detail later). In all instances, it is assumed that each stage provides zero loading to the driving stage. The stages shown reflect no particular op amp, but example principles can be found within the OP27 model (see Reference 10).

Because all of these frequency-shaping stages are dc-coupled and have unity gain, any number of them can be added or deleted, with no affect on the model's low frequency response. Most importantly, the high frequency gain and phase response can be precisely tailored to match a real amplifier's response. The benefits of this frequency-shaping flexibility are especially apparent in performance comparisons of the ADSpice model closed loop pulse response and stability analysis, versus that of a more simplistic model. This point is demonstrated by a later example.

Macromodel Output Stages

A general form of the output stage for the ADSpice model, shown in Figure 7-124, models a number of important op amp characteristics. The Thevenin equivalent resistance of R_{O1} and R_{O2} mimics the op amp's dc open-loop output impedance, while inductor L_O models the rise in impedance at high frequencies. A unity gain characteristic for the stage is set by the g_7–R_{O1} and g_8–R_{O2} products.

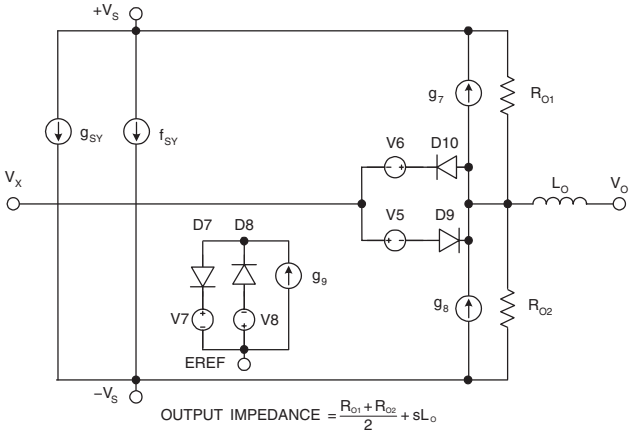


Figure 7-124: General-purpose macromodel output stage

Additionally, output load current is correctly reflected in the supply currents. This feature is a significant improvement over the Boyle model, because the power consumption of the loaded circuit can be analyzed accurately. Furthermore, circuits using the op amp supply currents as part of the signal path can also be correctly simulated. The output stage shown is not intended to reflect any particular op amp, but close similarity is found within the AD817 model (see Reference 11).

With the recent advent of numerous rail-rail output stage op amps, a number of customized model topologies have been developed. This expands the ADSpice library to include rail-rail model behavior, matching op amp architectures using P and N MOSFET devices, as well as bipolar devices. Characteristically, a rail-rail output stage includes several key differentiating performance points. First and foremost is the ability to swing the op amp output to within a few mV of both supplies. A second point is the fact that such an output stage has a voltage gain greater than one, and a third is the relatively high output impedance (high as contrasted to traditional emitter follower outputs).

Examples of several modeling approaches to rail-rail output stages are found in the ADI SPICE macromodel library. Reference 12 employs CMOS devices to realize a rail-rail output, while Reference 13 uses bipolar devices to the same end. The macromodels of References 14 and 15 use synthesis techniques to model rail-rail outputs. References 16–18 utilize combinations of selected discrete device models and synthesis techniques, to realize rail-rail output operation for both op amp and in amp devices.

In addition to rail-rail output operation, many modern op amps also feature rail-rail *input stages*. Such stages essentially duplicate, for example, an NPN-based differential stage with a complementary PNP stage, both stages operating in parallel. This allows the op amp to provide a CM range that includes both supply rails. This performance feature can also be accomplished within CMOS op amps, using both a P and N type MOS differential pairs. Model examples reflecting rail-rail input stages include References 13, 14, and 17.

Model Transient Response

The performance advantage of the multiple pole/zero stages is readily demonstrated in a transient pulse response test, as in Figure 7-125. This figure compares an actual OP249 op amp, the ADSpice model, and the Boyle model. It reveals the improved execution resulting from the unlimited number of poles and zeros in this model.

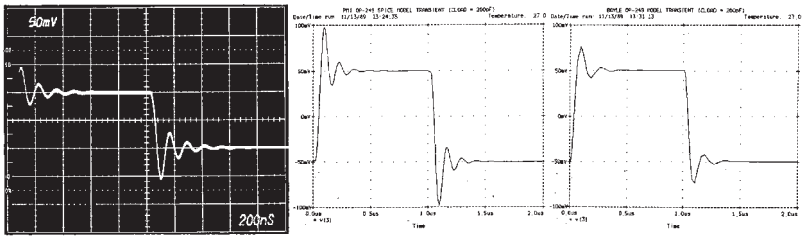


Figure 7-125: A pulse response comparison of an OP249 follower (left) model favors the ADSpice model in terms of fidelity (center), but not the Boyle (right)

The difference is easily apparent from this transient analysis plot for a unity gain follower circuit. An OP249 amplifier was used, with the output connected to the inverting input, and a 260 pF capacitive load.

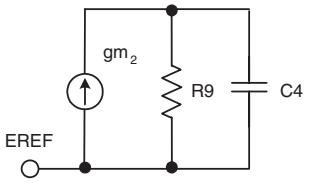
This results in ringing, as seen in the op amp response (left). Note that the ADSpice model accurately predicts the amount of overshoot and frequency of the damped ringing (center). In contrast, the Boyle model (right) predicts about half the overshoot and significantly less ringing.

The Noise Model

An important enhancement to the ADSpice model is the ability to realistically model noise performance of an op amp. The capability to model a circuit's noise in SPICE can be appreciated by anyone who has tried to analyze noise by hand. A complete analysis is an involved and tedious task that involves adding all the individual noise contributions from all active devices and all resistors, and referring them to the input.

To aid this task, the ADSpice model was enhanced to include noise generators that accurately mimic the broadband and 1/f noise of an actual op amp. Conceptually, this involves first making an existing model noiseless, and then adding discrete noise generators, so as to emulate the target device. As noted earlier, all ADI models aren't necessarily designed for this noise-accurate performance. Selected device models are designed for noise however, when their typical uses include low noise applications.

The first step is an exercise in scaling down the model internal impedances. For example, by reducing the resistances in the pole/zero stages from a base resistance of 1E6 Ω to 1 Ω, total noise is reduced dramatically, as figure 7-126 illustrates.



	CASE	
	"Noisy"	"Noiseless"
R9	$1x10^{6}\Omega$	1Ω
gm_2	$1x10^{-6}$	1.0
C4	$159x10^{-15}F$	$159x10^{-9}F$
Noise	129nV/√Hz	129pV/√Hz

Figure 7-126: Towards achieving low noise operation, a first design step is the reduction of pole/zero cell impedances to low values

For the "Noisy" column of the table, the noise from the pole stage shown with a large R9 resistor value is $129\ nV/\sqrt{Hz}$. But when this resistor is scaled down by a factor of 10^6, to 1 Ω , as in the "Noiseless" column, stage noise is $129\ pV/\sqrt{Hz}$. Note also that transconductance and capacitance values are also scaled by the same factor, maintaining the same gain and pole frequency. To make the model's input stage noiseless, it is operated at a high current and with reduced load resistances, making noise contributions negligible. Extending these techniques to the entire model renders it essentially noiseless.

Once global noise reduction is achieved, independent noise sources are added, one for voltage noise and two for current noise. The basic noise source topology used is like Figure 7-127, and it can be set up to produce both voltage and current noise outputs.

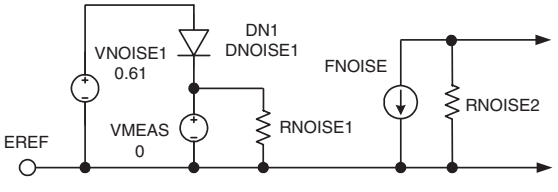


Figure 7-127: A basic SPICE noise generator is formed with diodes, resistors, and controlled sources

Note that, within SPICE, semiconductor models can generate 1/f (flicker) noise. The noise generators use diodes such as DN1 to produce this portion of the noise, modeling the 1/f noise of the op amp. By properly specifying diode model parameters and bias voltage VNOISE1, the 1/f noise is tailored to match the op amp. The noise current from DN1 passes through a zero voltage source. Here VMEAS is being used as a measurement device, combining the 1/f noise from DN1 and the broadband noise from RNOISE1.

RNOISE1 is selected for a value providing an appropriate broadband noise. The combined noise current in VMEAS is monitored by FNOISE, and appears as a voltage across RNOISE2. This voltage is then injected in series with one amplifier input via a controlled voltage source, such as E_N of Figure 7-122. Either FNOISE or a controlled voltage source coefficient can be used for overall noise voltage scaling.

Current noise generation is similar to the above, except that the RNOISE2 voltage producing resistor isn't used, and two current-controlled sources drive the amplifier inputs. With all noise generators symmetrical about ground, dc errors aren't introduced.

Current Feedback Amplifier Models

As noted previously, a new model topology was developed for current feedback amplifiers, to accommodate their unique input stage structure (see Reference 9). The model uses a topology as shown in Figure 7-128 for the input and gain stages. The remaining model portions (not shown) contain multiple pole/zero stages and the output stage, and are essentially the same as voltage feedback amplifiers, described above.

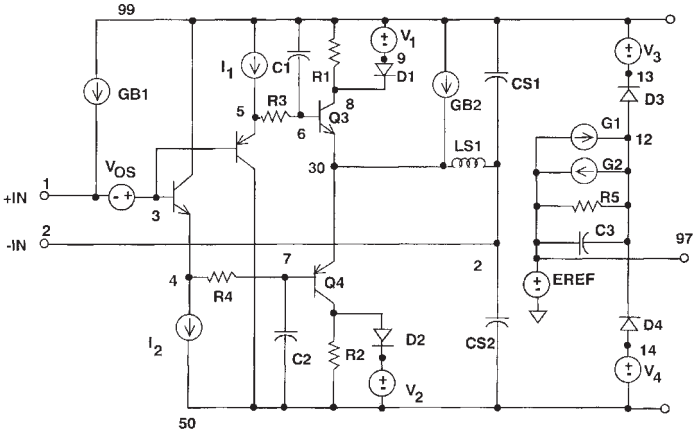


Figure 7-128: Input and gain stages of current feedback op amp macromodel

The four bipolar transistor input stage resembles actual current feedback amplifiers, with a high impedance noninverting input (+IN) and a low impedance inverting input (–IN). In current feedback amplifiers, the maximum slew rate is very high, because dynamic slew current isn't limited to a differential pair tail current (as in voltage feedback op amps). In current feedback op amp designs, much larger amounts of error current can flow in the inverting input, as developed by the feedback network. Internally, this current flows in either Q3 or Q4, and charges compensation capacitor C3 via current mirrors.

The current mirrors of the ADSpice model are actually voltage controlled current sources in the gain stage, G1 and G2. They sense voltage drops across input stage resistors R1 and R2, and translating this into a C3 charging current. By making the value of G1 and G2 equal to the R1-R2 reciprocal, the slew currents will be identical. By clamping the R1-R2 voltage drops via D1–V1 and D2–V2, the maximum current is limited, which thus sets the highest slew rate. Open loop gain or transresistance of the model is set by R5, and the open loop pole frequency by C3–R5 (as described previously, Figure 7-122). The output from across R5–C3 (node 12) drives the model's succeeding frequency-shaping stages, and EREF is again an internal reference voltage.

One of the unique properties of current feedback amplifiers is that bandwidth is a function of the feedback resistor and the internal compensation capacitor, C3. The lower the feedback resistor, the greater the bandwidth, until a practical lower limit is reached, i.e., the value at which the part oscillates. As the model includes a low impedance inverting input, it accurately mimics real part behavior as R_F is altered. Figure 7-129 compares the ADSpice model to the actual device for an AD811 video amplifier. As shown, the model accurately predicts the gain roll-off at the much lower frequency for the 1 kΩ feedback resistor as opposed to the 500 Ω resistor.

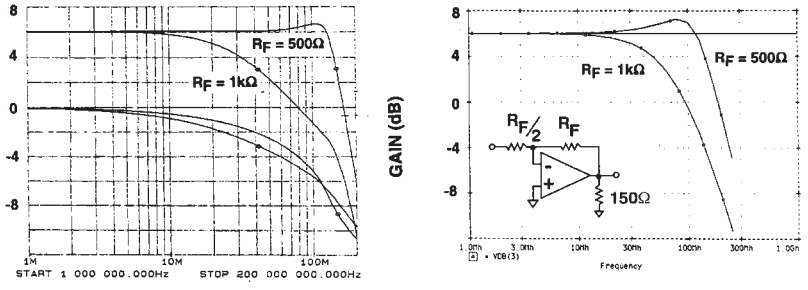


Figure 7-129: Comparison of a real AD811 current feedback op amp (left) with macromodel (right) shows similar characteristics as feedback resistance is varied

The current feedback amplifier input and gain stage is an enhancement to the ADSpice model that increases flexibility in modeling different op amp devices, and provides a net increase in design cycle speed.

Simulation Must Not Replace Breadboarding

No matter how accurate the models, or how much confidence you have with simulations, *SPICE analysis alone should never totally replace breadboarding*. As part of a layout and the actual devices existing within a real world PCB assembly, there are second and third order effects that can easily become relevant to performance. By and large, SPICE will never "know" of such things, unless explicitly entered into the SPICE netlist. However, this may be either difficult or outright impossible. The user may not be aware of some things before a PCB is built and tested within the final system—spurious signal coupling, the effects of crosstalk, the inevitable parasitic capacitance, inductance, and resistance—on and on goes the list. It is virtually impossible to include all of these effects in a simulation. Without actually building a PCB, and operating it under the intended conditions, the user will not have any data whatsoever on the magnitudes involved.

Furthermore, remember the fact that no macromodel includes all op amp characteristics. For example, exceeding the input voltage range can cause nonlinear behavior in an op amp, which is not necessarily included in its model. Because of such effects that a simulation might not predict, it is necessary to breadboard the circuit.

Even with models as comprehensive as those of the ADSpice library, external effects can easily cause a circuit to work improperly. As noted, PCB parasitics can significantly alter the frequency performance in high speed designs. Such parasitics are easily overlooked in a SPICE simulation, but a breadboard will reveal the problems.

Ultimately, simulation and breadboarding should be used together to maximize the design efficiency. Figure 7-130 summarizes these pro and con points of analog simulations.

- Understand What's Real (Hardware), and What Isn't (SPICE)
- Use Breadboarding/Prototyping as Final Design Verification
- Be Aware of Non-Modeled Op Amp Characteristics
- Pay Attention to PCB Parasitics Impacting Circuit Behavior

Figure 7-130: Some analog simulation caveats

Obviously, the designer needs to be wary of what SPICE can/cannot do, and the necessity of closely allying simulations with breadboarding and prototyping.

Simulation is a Tool to be Used "Wisely"

It must be remembered that while simulation is an extremely powerful tool, it must be used wisely to realize its full benefits. This includes knowing models well, understanding PCB and other parasitic effects, and anticipating the results. For example, consider a simple differential amplifier comprised of an op amp and four equal resistors, to be analyzed for common-mode rejection ratio (CMRR) performance. At low frequencies, CMRR will be dominated by resistor mismatch, while at higher frequencies it is dominated by op amp CMRR performance. However, a SPICE simulation will only show this if the external resistors are realistically mismatched, and the op amp model used also properly treats not only dc CMRR, but also CMRR reduction at higher frequencies. If these critically important points are overlooked in the analysis, then an optimistic result will shows excellent CMRR performance over the entire circuit bandwidth. Unfortunately, this is simply wrong. Alternatively, substituting into the netlist resistors mismatched by their specified tolerances as well as an ADSpice model (which *does* have CMRR frequency effects modeled) the end results will be quite different. CMRR performance at low frequencies will be limited by resistor mismatch errors, and will degrade at higher frequencies, as would a real op amp device with CMRR versus frequency effects.

Know the Models

Using various dc and ac tests, any op amp macromodel can be checked for accuracy and functional completeness. Specialized test simulations can also be devised for other op amp parameters important for a particular analysis. All this is critically important, as knowing a model's capabilities ahead of time can help prevent many headaches later.

Understand PCB Parasitics

Even if the model passes all preliminary tests, caution still should be exercised. As noted, PCB parasitics can have significant impact on a circuit's performance. This is especially true for high speed circuits. A few picofarads of capacitance on the input node can make the difference between a stable circuit and one that oscillates. Thus, these effects need to be carefully considered when simulating the circuit to achieve meaningful results.

To illustrate the impact of PCB parasitics, the simple voltage follower circuit of Figure 7-131 (left) was built twice. The first time this was on a carefully laid out PCB, and the second time on a component plug-in type of prototype board. An AD847 op amp is used because of its 50 MHz bandwidth, which makes the parasitic effects much more critical (smaller C values will have a greater effect on results).

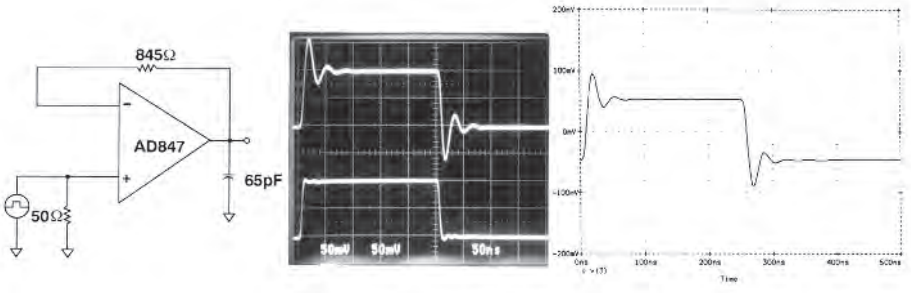


Figure 7-131: With care and low parasitic effects in the PCB layout, results of lab testing (center) and simulation (right) can converge

As the results above indicate, this circuit executed on a properly laid out PCB has a clean response with minor overshoot and ringing (center picture). The SPICE model results also closely agree with the real part, showing a corresponding simulation (right picture).

On the other hand, the same circuit built on the plug-in prototype board shows distinctly different results. In general, it shows much worse performance, due to the relatively high nodal capacitances around the op amp inputs, which degrade the square wave response to severe ringing, much less than full capability of the part.

This is shown in Figure 7-132 in the center and right pictures, respectively. The voltage follower circuit on the left shows the additional capacitances as inherent to the prototype board. With this test circuit and corre-

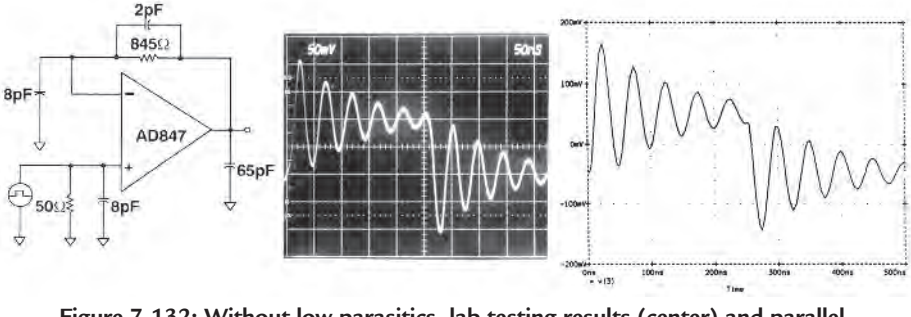


Figure 7-132: Without low parasitics, lab testing results (center) and parallel simulation (right) still show convergence—with a poorly damped response

sponding analysis, there was (initially) no agreement between the poor lab test, and the parallel SPICE test. However, when the relevant PCB parasitic capacitances are included in the SPICE file, then the simulation results do agree with the real circuit, as noted in the right picture.

This example illustrates several key points. One, PCB parasitics can easily make a high speed circuit behave much differently from a simplistic SPICE analysis. Secondly, when the SPICE netlist is adjusted to more reasonably reflect the parasitic elements of a PCB, the simulation results do compare with the actual lab test. Finally, a point that should be obvious, a clean PCB layout with minimal parasitics is critically important to high speed designs. To put this in a broader perspective, op amps of today are capable of operating to 1 GHz or more.

Another interesting point is that the simulation can be used as a rough measure of the PCB layout design. If the simulation, without any parasitics, agrees with the PCB, there is a reasonable assurance that PCB is laid out well.

Parasitic PCB elements are not the only area that may cause differences between the simulation and the breadboard. A circuit may exhibit nonlinear behavior during power-on that will cause a device to lock up. Or, a device may oscillate due to insufficient power supply decoupling or lead inductance. SPICE circuits need *no* bypassing, *but real world ones always do*. It is, practically speaking, impossible to anticipate all normal or abnormal operating conditions to which an amplifier might be subjected.

Thus, it is always important that circuits be breadboarded and thoroughly checked in the lab. Careful forethought in these stages of design helps minimize any unknown problems from showing up when the final PCBs are manufactured.

Simulation Speeds the Design Cycle

Simulation is very effective in the initial design phase, to try out different ideas and circuit configurations. When a circuit topology has been decided upon and tested in SPICE, a breadboard can be built. If the simulation was done carefully, the breadboard has good likelihood of working correctly without significant modifications.

When the simulation and the actual results correlate, the circuit can easily be altered in SPICE to perform many different types of analysis. For example, it is much easier to try to optimize the circuit while working within SPICE, as opposed to repeatedly modifying a breadboard. Quick substitutions of the op amps and components can be made in SPICE and the results immediately viewed.

Worst-case and sensitivity analyses are also done in SPICE much easier than on paper, and with multiple SPICE runs, the sensitivity to a certain parameter can be determined. Consider for example an analysis of a multistage active filter, for all possible combinations of component values. This is a nightmare, if not impossible, either by hand or in the lab, but valid results for response extremes can be obtained relatively easily via a SPICE Monte Carlo option, providing greater design confidence.

Some general SPICE-related points are useful towards an overall healthy perspective on this, as shown in Figure 7-133.

- Quickly Check Circuit Ideas
- Eases Circuit Optimization
- Allows Component Alteration for Worst Case and Sensitivity Analyses
- Allows Quick Comparison of Different Op Amps

Figure 7-133: Some useful points on using SPICE simulations

While simulation cannot reasonably be allowed to replace breadboarding, the two can and should be used together, to increase the efficiency of a design cycle.

SPICE Support

A variety of industry vendors offer SPICE analysis packages for various computer platforms, including the PC. The first of these and among the most popular is PSpice®, a commercial program that now includes allied packages for both schematic capture and PCB layout (see Reference 19). In addition, many vendors also offer low or no cost limited capability student versions of their SPICE programs.

Model Support

The ADSpice model library is available in several different forms. Included within it are models of several IC device types, in addition to the op amps discussed above. These are for in amps, analog multipliers, voltage references, analog switches, analog multiplexers, matched transistors, and buffers. Individual op amp models are available as listings on many data sheets. Electronic ASCII text files of the model library are found from either the ADI website (see References), the Analog Devices Literature Center via 1-800-ANALOGD (1-800-262-5643), or on the ADI support CD.

Acknowledgments:

There have been numerous model authors of SPICE macromodels for the ADI library. These include Derek Bowers, Eberhard Brunner, Joe Buxton, Vic Chang, Bob Day, Wes Freeman, Adolfo Garcia, Antonio Germano, John Hayes, John McDonald, Troy Murphy, Al Neves, Steve Reine, Bill Tolley, Tim Watkins, and James Wong.

Breadboard and Prototyping Techniques

A basic principle of a breadboard or a prototype structure is that it is a *temporary* one, designed to test the performance of an electronic circuit or system. By definition it must therefore be easy to modify, particularly so for a breadboard.

There are many commercial prototyping systems, but unfortunately for the analog designer, almost all of them are designed for prototyping *digital* systems. In such environments, noise immunities are hundreds of millivolts or more. Prototyping methods commonly used include noncopper-clad Matrix board, Vectorboard, wire-wrap, and plug-in breadboard systems. Quite simply, these all are unsuitable for high performance or high frequency analog prototyping, because of their excessively high parasitic resistance, inductance, and capacitance levels. Even the use of standard IC sockets is inadvisable in many prototyping applications (more on this below).

Figure 7-134 summarizes a number of key points on selecting a useful analog breadboard and/or prototyping system, which follows.

- Always Use a Ground Plane for Precision or High Frequency Circuits
- Minimize Parasitic Resistance, Capacitance, and Inductance
- If Sockets Are Required, Use "Pin Sockets" ("Cage Jacks")
- Pay Equal Attention to Signal Routing, Component Placement, Grounding, and Decoupling in Both the Prototype and the Final Design
- Popular Prototyping Techniques:
  - Freehand "Deadbug" Using Point-to-Point Wiring
  - "Solder-mount"
  - Milled PC Board from CAD Layout
  - Multilayer Boards: Double-Sided with Additional Point-to-Point Wiring

Figure 7-134: A summary of analog prototyping system key points

One of the more important considerations in selecting a prototyping method is the requirement for a large-area ground plane. This is required for high frequency circuits as well as low speed precision circuits, especially when prototyping circuits involving ADCs or DACs. The differentiation between *high speed* and *high precision* mixed-signal circuits is difficult to make. For example, 16+-bit ADCs (and DACs) may operate on high speed clocks (>10 MHz) with rise and fall times of less than a few nanoseconds, while the effective throughput rate of the converters may be less than 100 kSPS. Successful prototyping of these circuits requires that equal (and thorough) attention be given to good high speed and high precision circuit techniques.

Deadbug Prototyping

A simple technique for analog prototyping uses a solid copper-clad board as a ground plane (see References 20 and 21). In this method, the ground pins of the ICs are soldered directly to the plane, and the other components are wired together above it. This allows HF decoupling paths to be very short indeed. All lead lengths should be as short as possible, and signal routing should separate high level and low level signals. Connection wires should be located close to the surface of the board to minimize the possibility of stray inductive coupling. In most cases, 18-gauge or larger insulated wire should be used. Parallel runs should not be "bundled" because of possible coupling. Ideally the layout (at least the relative placement of

the components on the board) should be similar to the layout to be used on the final PCB. This approach is often referred to as *deadbug prototyping*, because the ICs are often mounted upside down with their leads up in the air (with the exception of the ground pins, which are bent over and soldered directly to the ground plane). The upside-down ICs look like deceased insects, hence the name.

Figure 7-135 shows a hand-wired "deadbug" analog breadboard. This circuit uses two high speed op amps and, in fact, gives excellent performance in spite of its lack of esthetic appeal. The IC op amps are mounted upside down on the copper board with the leads bent over. The signals are connected with short point-to-point wiring. The characteristic impedance of a wire over a ground plane is about 120 Ω, although this may vary as much as ±40%, depending on the distance from the plane. The decoupling capacitors are connected directly from the op amp power pins to the copper-clad ground plane. When working at frequencies of several hundred MHz, it is a good idea to use only one side of the board for ground. Many people drill holes in the board and connect the sides together by soldering short pieces of wire. If care isn't taken, this may result in unexpected ground loops between the two sides of the board, especially at RF frequencies.

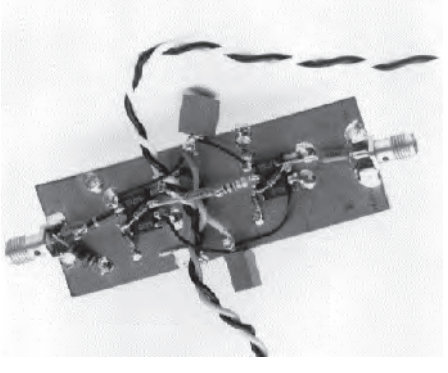


Figure 7-135: A "deadbug" analog breadboard

Pieces of copper-clad board may be soldered at right angles to the main ground plane to provide screening, or circuitry may be constructed on both sides of the board (with through-hole connections) with the board itself providing screening. For this, the board will need corner standoffs to protect underside components from being crushed.

When the components of a breadboard of this type are wired point-to-point in the air (a type of construction strongly advocated by Bob Pease (see Reference 21) and sometimes known as "bird's nest" construction) there is always the risk of the circuitry being crushed and resulting short-circuits. Also, if the circuitry rises high above the ground plane, the screening effect of the ground plane is diminished, and interaction between different parts of the circuit is more likely. Nevertheless, the technique is very practical and widely used because the circuit may easily be modified (this of course assumes the person doing the modifications is adept with soldering techniques).

Another prototype breadboard variation is shown in Figure 7-136. Here the single-sided copper-clad board has pre-drilled holes on 0.1" centers (see Reference 22). Power buses are used at the top and bottom of the board. The decoupling capacitors are used on the power pins of each IC. Because of the loss of copper area due to the predrilled holes, this technique does not provide as low a ground impedance as a completely covered copper-clad board of Figure 7-135, so be forewarned.

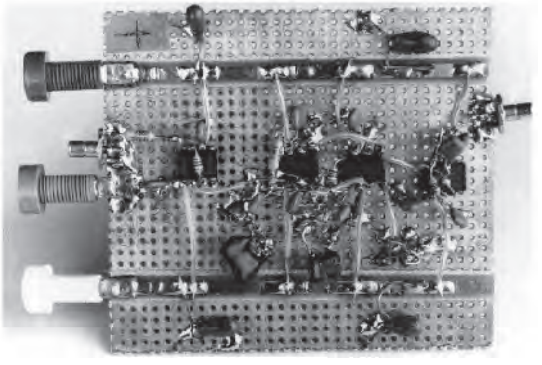


Figure 7-136: A "deadbug" prototype using 0.1" predrilled single-sided, copper-clad printed board material

In a variation of this technique, the ICs and other components are mounted on the noncopper-clad side of the board. The holes are used as vias, and the point-to-point wiring is done on the copper-clad side of the board. Note that the copper surrounding each hole used for a via must be drilled out, to prevent shorting. This approach requires that all IC pins be on 0.1" centers. For low frequency circuits, low profile sockets can be used, and the socket pins then will allow easy point-to-point wiring.

Solder-Mount Prototyping

There is a commercial breadboarding system that has most of the advantages of the above techniques (robust ground, screening, ease of circuit alteration, low capacitance, and low inductance) and several additional advantages: it is rigid, components are close to the ground plane and, where necessary, node capacitances and line impedances can be easily calculated. This system is made by Wainwright Instruments and is available in Europe as "Mini-Mount" and in the USA (where the trademark "Mini-Mount" is the property of another company) as "Solder-Mount" (see References 23 and 24).

Solder-Mount consists of small pieces of PCB with etched patterns on one side and contact adhesive on the other. These pieces are stuck to the ground plane, and components are soldered to them. They are available in a wide variety of patterns, including ready-made pads for IC packages of all sizes from 8-pin SOICs to 64-pin DILs, strips with solder pads at intervals (which intervals range from 0.040" to 0.25", the range includes strips with 0.1" pad spacing which may be used to mount DIL devices), strips with conductors of the correct width to form microstrip transmission lines (50 Ω, 60 Ω, 75 Ω or 100 Ω) when mounted on the ground plane, and a variety of pads for mounting various other components. Self-adhesive tinned copper strips and rectangles (LO-PADS) are also available as tie-points for connections. They have a relatively high capacitance to ground and therefore serve as low inductance decoupling capacitors. They come in sheet form and may be cut with a knife or scissors.

The main advantage of Solder-Mount construction over "bird's nest" or "deadbug" is that the resulting circuit is far more rigid and, if desired, may be made far smaller (the latest Solder-Mounts are for surface-mount devices and allow the construction of breadboards scarcely larger than the final PCB, although it is generally more convenient if the prototype is somewhat larger). Solder-Mount is sufficiently durable that it may be used for small quantity production as well as prototyping.

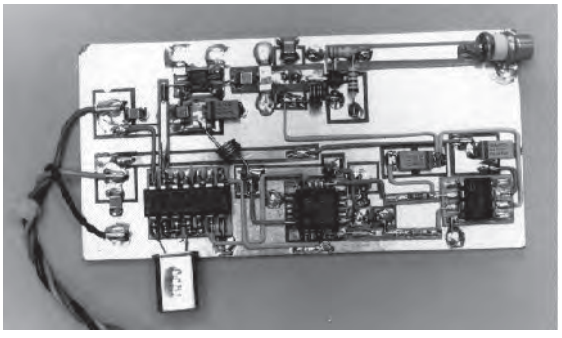


Figure 7-137: A "Solder-Mount" constructed prototype board

Figure 7-137 shows an example of a 2.5 GHz phase-locked-loop prototype, built with Solder-Mount techniques. While this is a high speed circuit, the method is equally suitable for the construction of high resolution low frequency analog circuitry.

A particularly convenient feature of Solder-Mount at VHF is the relative ease with which transmission lines can be formed. As noted earlier, if a conductor runs over a ground plane, it forms a microstrip transmission line. The Solder-Mount components include strips that form microstrip lines when mounted on a ground plane (they are available with impedances of 50 Ω, 60 Ω, 75 Ω, and 100 Ω). These strips may be used as transmission lines for impedance matching or, alternately, more simply as power buses. Note that glass fiber/epoxy PCB is somewhat lossy at VHF/ UHF, but losses will probably be tolerable if microstrip runs are short.

Milled PCB Prototyping

Both "deadbug" and "Solder-Mount" prototypes become tedious for complex analog circuits, and larger circuits are better prototyped using more formal layout techniques.

There is a prototyping approach that is but one step removed from conventional PCB construction, described as follows. This is to actually lay out a double-sided board, using conventional CAD techniques. PC-based software layout packages offer ease of layout as well as schematic capture to verify connections (see References 25 and 26). Although most layout software has some degree of autorouting capability, this feature is best left to digital designs. The analog traces and component placements should be done by hand, following the rules discussed elsewhere in this chapter. After the board layout is complete, the software verifies the connections per the schematic diagram net list.

Many designers find that they can make use of CAD techniques to lay out simple boards. The result is a pattern-generation tape (or Gerber file) which would normally be sent to a PCB manufacturing facility where the final board is made.

Rather than use a PCB manufacturer, however, automatic drilling and milling machines that accept the PG tape directly are available (see References 27 and 28). An example of such a prototype circuit board is shown in Figure 7-138 (top view).

These systems produce either single or double-sided circuit boards directly, by drilling all holes and using a milling technique to remove conductive copper, thus creating the required insulation paths and, finally, the finished prototype circuit board. The result can be a board functionally quite similar to a final manufactured double-sided PCB.

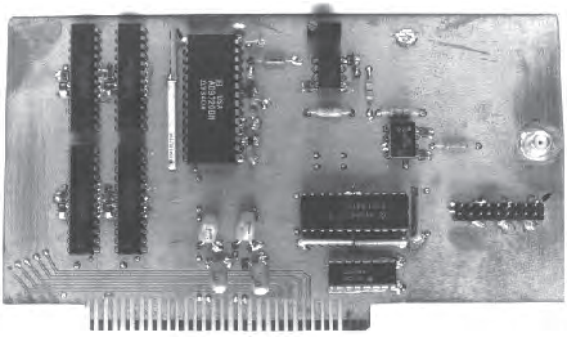


Figure 7-138: A milled circuit construction prototype board (top view)

However, it should be noted that a chief caveat of this method is that there is no "plated-through" hole capability. Because of this, any conductive "vias" required between the two layers of the board must be manually wired and soldered on both sides.

Minimum trace widths of 25 mils (1 mil = 0.001") and 12 mil spacing between traces are standard, although smaller trace widths can be achieved with care. The minimum spacing between lines is dictated by the size of the milling bit used, typically 10 to 12 mils.

A bottom-side view of this same milled prototype circuit board is shown in Figure 7-139. The accessible nature of the copper pattern allows access to the traces for modifications.

Perhaps the greatest single advantage of the milled circuit type of prototype circuit board is that it approaches the format of the final PCB design most closely. By its very nature, however, it is basically limited to only single or double-sided boards.

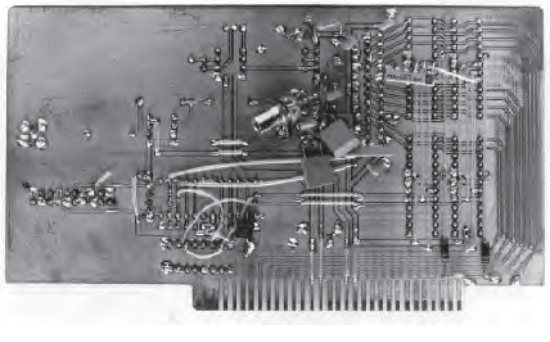


Figure 7-139: A milled circuit construction prototype board (bottom view)

Beware of Sockets

IC sockets can degrade the performance of high speed or high precision analog ICs. Although they make prototyping easier, even *low profile* sockets often introduce enough parasitic capacitance and inductance to degrade the performance of a high speed circuit. If sockets must be used, a socket made of individual *pin sockets* (sometimes called *cage jacks*) mounted in the ground plane board may be acceptable, as in Figure 7-140.

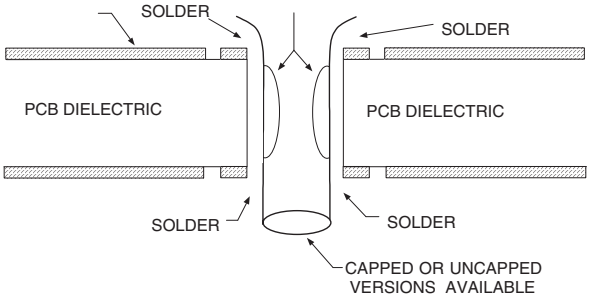


Figure 7-140: When necessary, use pin sockets for minimal parasitic effects

To use this technique, clear the copper (on both sides of the board) for about 0.5 mm around each ungrounded pin socket, Then solder the grounded socket pins to ground, on both sides of the board.

Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6, respectively). The pin sockets protrude through the board far enough to allow point-to-point wiring interconnections.

Because of the spring-loaded gold-plated contacts within the pin socket, there is good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade the performance of the pin socket, so this factor should be kept in mind.

Note also that the uncapped versions allow the IC pins to extend out the bottom of the socket. This feature leads to an additional useful function. Once a prototype using the pin sockets is working and no further changes are to be made the IC pins can be soldered directly to the bottom of the socket. This establishes a rugged, permanent connection.

Some Additional Prototyping Points

The prototyping techniques discussed so far have been limited to single or double-sided PCBs. Multilayer PCBs do not easily lend themselves to standard prototyping techniques. If multilayer board prototyping is required, one side of a double-sided board can be used for ground and the other side for power and signals. Point-to-point wiring can be used for additional runs which would normally be placed on the additional layers provided by a multilayer board. However, it is difficult to control the impedance of the point-to-point wiring runs, and the high frequency performance of a circuit prototyped in this manner may differ significantly from the final multilayer board.

Other difficulties in prototyping may occur with op amps or other linear devices having bandwidths greater than a few hundred megahertz. Small variations in parasitic capacitance (<1 pF) between the prototype and the final board can cause subtle differences in bandwidth and settling time.

Sometimes, prototyping is done with DIP packages, when the final production package is an SOIC. *This is not recommended.* At high frequencies, small package-related parasitic differences can account for different performance, between prototype and final PCB. To minimize this effect, always prototype with the final packages.

Evaluation Boards

Most manufacturers of analog ICs provide *evaluation boards,* usually at a nominal cost. These boards allow customers to evaluate ICs without constructing their own prototypes. Regardless of the product, the manufacturer has taken proper precautions regarding grounding, layout, and decoupling to ensure optimum device performance. Where applicable, the evaluation PCB artwork is usually made available free of charge, should a customer wish to copy the layout directly or make modifications to suit an application.

General-Purpose Op Amp Evaluation Boards

Evaluation boards can either be dedicated to a particular IC, or they can be general-purpose. With op amps the most universal linear IC, it is logical that evaluation boards be developed for them, to aid easy applications. However, it is also important that a good quality evaluation board avoid the parasitic effects discussed above. An example is the general-purpose dual amplifier evaluation board of in Figure 7-141 (see Reference 29).

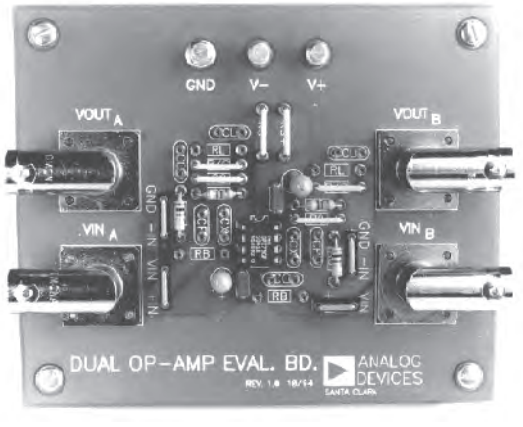


Figure 7-141: A general-purpose op amp evaluation board allows fast, easy configuration of low frequency op amp circuits

This board uses pin sockets for any standard dual op amp pinout device, and a flexible set of component jumper locations allows it to be setup for inverting or noninverting amplifiers. Various gains can be configured by choice of the component values, in either ac- or dc-coupled configurations.

The card design provides signal coupling via BNC connectors at input and output. It also uses external lab power supplies, which are wired to the lug terminals at the top. The card does, however, contain local supply voltage decoupling and bypassing components.

These general-purpose boards are intended for medium to high precision uses at frequencies below 10 MHz, with moderate op amp input currents. For higher operating speeds, a dedicated, device-specific evaluation board is likely to be a better choice.

Dedicated Op Amp Evaluation Boards

In high speed/high precision ICs, special attention must be given to power supply decoupling. For example, fast slewing signals into relatively low impedance loads produce high speed transient currents at the power supply pins of an op amp. The transient currents produce corresponding voltages across any parasitic impedance that may exist in the power supply traces. These voltages, in turn, may couple to the amplifier output, because of the op amp's finite power supply rejection at high frequencies.

The AD8001 high speed current-feedback amplifier is a case in point, and a dedicated evaluation board is available for it. A bottom side view of this SOIC board is shown in Figure 7-142. A triple decoupling scheme was chosen, to ensure a low impedance ground path at all transient frequencies. Highest frequency transients are shunted to ground by dual 1000 pF/0.01 μF ceramic chip capacitors, located as close to the power supply pins as possible to minimize series inductance and resistance. With these surface-mount components, there is minimum stray inductance and resistance in the ground plane path. Lower frequency transient currents are shunted by the larger 10 μF tantalum capacitors.

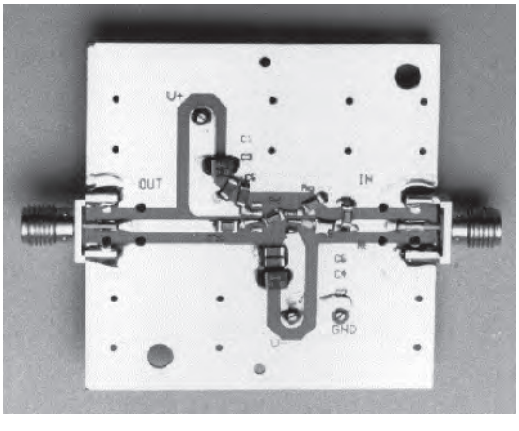


Figure 7-142: A high speed op amp such as the AD8001 requires a dedicated evaluation board with suitable ground planes and decoupling (bottom view)

The input and output signal traces of this board are 50 Ω microstrip transmission lines, as can be noted towards the right and left. Gain-set resistors are chip-style film resistors, which have low parasitic inductance. These can be seen in the center of the photo, mounted at a slight diagonal.

Note also that there is considerable continuous ground plane area on both sides of the PCB. Plated-through holes connect the top and bottom side ground planes at several points, in order to maintain lowest possible impedance and best high frequency ground continuity.

Input and output connections to the card are provided via the SMA connectors as shown, which terminate the input/output signal transmission lines. The board's power connection from external lab supplies is made via solder terminals, which are seen at the ends of the broad supply line traces.

Some of these points are more easily seen in a topside view of the same card, which is shown in Figure 7-143. This AD8001 evaluation board is a noninverting signal gain stage, optimized for lowest parasitic capacitance. The cutaway area around the SOIC outline of the AD8001 provides lowest stray capacitance, as can be noted in this view.

In this view is also seen the virtually continuous ground plane and the multiple vias, connecting the top/bottom planes.

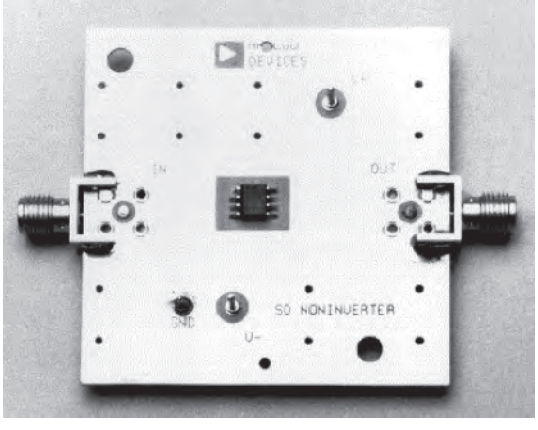


Figure 7-143: The AD8001 evaluation board uses a large area ground plane as well as minimal parasitic capacitance (top view)

Summary

In summary, good analog designers utilize as many tools as possible to ensure that the final system design performs correctly. The first step is the intelligent use of IC op amp and other macromodels, where available, to simulate the circuit. The second step is the construction of a prototype board to further verify the design, and to validate the simulation. The final PCB layout should then be based on the prototype layout as much as possible, with careful attention to parasitic effects.

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CHAPTER 8

Op Amp History

- Section 8-1: Introduction
- Section 8-2: Vacuum Tube Op Amps
- Section 8-3: Solid-State Modular and Hybrid Op Amps
- Section 8-4: IC Op Amps