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## Circuit uses two reference voltages to improve hysteresis accuracy

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In advanced IC comparators, programmable hysteresis eliminates 0V-centered differential-input-voltage noise (Reference 1) and improves the comparator's response if its differential-input voltage is low or varies slowly over time. For example, the ADCMP609 comparator from Analog Devices (www.analog.com) lets you program its hysteresis from 0 to 160 mV with a single resistor that connects between the HYS (hysteresis) pin and ground. That voltage range may be too narrow for some applications, however. The circuit in Figure 1

lets you widen the hysteresis by using two reference voltages applied to the noninverting input. The circuit uses IC<sub>3</sub>, an Analog Devices ADR390B, to generate a high reference voltage, V<sub>REFH</sub>, of 2.048V. Resistor divider R<sub>1</sub>/R<sub>2</sub> produces a low reference voltage, V<sub>REFL</sub>, of 0.2048V, or a difference of 1.8432V. Thus, the hysteresis equals the high reference voltage minus the low reference voltage. IC<sub>2</sub>, an Analog Devices ADG772 dual-SPDT (single-pole/double-throw) switch, routes the voltages to the comparator's noninverting input (Reference 2).

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Whenever the input voltage at the comparator's inverting input exceeds the high reference voltage, the output

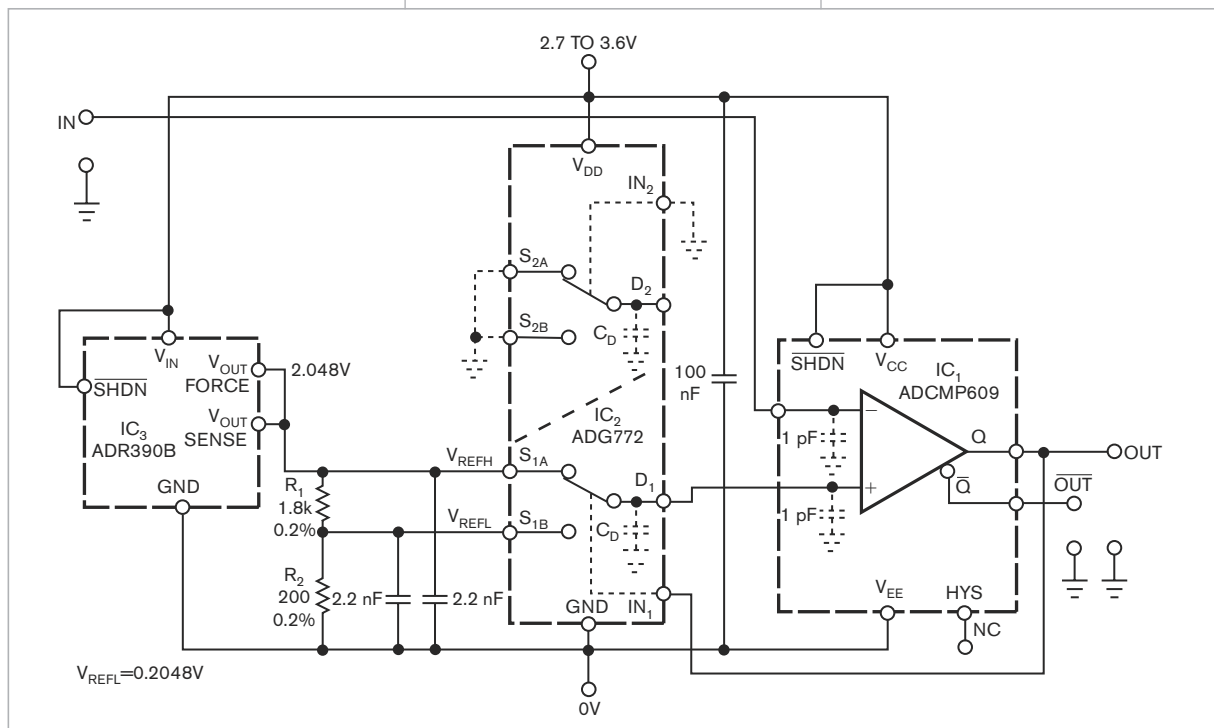


Figure 1 An analog switch changes the comparator's reference voltage, thus increasing hysteresis.

goes to a logic low. That action forces  $S_{1B}$  to connect the low reference voltage to the comparator's noninverting input. The circuit remains in that state until the input voltage drops below the low reference voltage. At that point, the switch connects the high reference voltage back to the comparator. For fast-ramping waveforms at the input, the hysteresis increases because of signal-propagation delays in both  $IC_1$  and  $IC_2$ . The 35-nsec propagation delay in the ADCMP609 occurs at approximately 10 mV of input overdrive, and this overdrive roughly doubles in effect as an addition to the hysteresis voltage, increasing it by approximately 1%.

Because ADCMP60x comparators are rail-to-rail I/O devices, the low reference voltage could be 0V. In this

case, however, the value of 0.2048V lets the comparator cooperate with other rail-to-rail I/O ICs from the same supply voltage. The outputs of these ICs can swing between 0V and the power-supply voltage with a margin of millivolts to tens of millivolts, depending on the load. An ADR390B provides the reference voltages (**Reference 3**). The 2.2-nF decoupling capacitors suppress variations of these voltages during voltage transitions at the Q output. These values are sufficient because the parasitic-charge transfer from the switch's control input,  $IN_1$ , to the respective channel's source electrode is typically 0.5 pC. The short-term variation of the decoupled reference voltages is less than 250  $\mu$ V. **EDN**

## REFERENCES

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- 2 "ADG772 CMOS Low Power Dual 2:1 Mux/Demux USB 2.0 (480 Mbps)/USB 1.1 (12 Mbps)," Analog Devices, 2007 to 2008, [www.analog.com/en/switchesmultiplexers/analog-switches/ADG772/products/product.html](http://www.analog.com/en/switchesmultiplexers/analog-switches/ADG772/products/product.html).
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