wireless world circard

Set 12: Wideband amplifiers

After considering the suitability of various transistor equivalent circuits, the accompanying article describes the many ways to get extended h.f. performance from transistor circuits. As with valve circuits, there is the well-known limitation to the number of stages that can be cascaded for optimum gain-bandwidth product. To improve on it shunt and series peaking with inductors is the first line of attack, which soon runs into problems of instability and interaction when stages are cascaded. Incidentally, card 2 recalls the dodge, widely used in pulse circuits, of making a parallel RC input network equal in time constant to $R_{in}C_{in}$. A popular method of reducing the effect of Miller (or should we say Blumlein) multiplication of input capacitance is the cascode arrangement (cards 5 & 7), considered as a common-emitter, common-base cascade.

There are other arrangements of two transistors (see also set 20) that can provide good bandwidth; card 12 shows a common-base, common-collector arrangement, related to the d.c. feedback pair of card 9. (For readers who are unclear of the various feedback arrangements around transistor pairs, see Fig. 8, the table and the text on pages 28 and 29.)

Integrated circuits offer good solutions in many situations, useful types being variants of the standard 741, 301 devices, and compensation points to modify h.f. characteristics are provided on i.cs such as the LM318 (card 11). A dodge not to be forgotten is to use digital i.cs in a linearly-biased mode; cards 6 & 8 show how, the e.c.l. circuits offering bandwidths up to a few hundred megahertz.

Wideband amplifiers

Wideband amplifiers are extensively used in instrumentation and communication systems where the signals to be handled may be of an analogue or a digital nature. Such amplifiers are required to provide fairly equal amplification of a large range of frequencies with a lower frequency limit of zero or nearly zero. The high-frequency behaviour of the active devices must be considered in conjunction with the passive network elements to design an amplifier with required characteristics.

Many different circuit models are available for such devices, but not all are necessarily useful. Consider, for example, the bipolar junction transistor models shown in Fig. 1. The three versions of the intrinsic low-frequency equivalent circuit shown in (a), (b) and (c) are highly-idealized models that focus attention on the basic active properties of the device. The low-frequency T and h-parameter models shown in (d) and (e) are more useful, but are unsatisfactory for predicting amplifier performance in the region of its upper cut-off frequency.

Models that are useful for high-frequency design must provide a more realistic representation of the transistor as a network element. The high-frequency model one chooses is often determined by availability of data, personal preferences and experience or whether the parameters of interest are readily determined by measurement. Fig. 2(a) shows the hybrid equivalent circuit which is a reasonable compromise between accuracy and complexity and which may be reduced to simpler forms for low-frequency and high-frequency calculations.

In high-frequency transistors, r_{ce} and $r_{b'c}$ are often sufficiently large to be neglected, the former being much larger than the load impedance and the latter much greater than the reactance of $C_{b'c}$ at high frequencies. The simplified form of Fig. 2(b) is often sufficiently accurate for assessing high-frequency performance and this may be reduced to that shown in Fig. 2(c), where C_{in} consists of $C_{b'e}$ in parallel with the Miller effect equivalent of $C_{b'c}$. The base spreading resistance $r_{bb'}$ and the product $g_m r_{b'e}$ may normally be assumed to be independent of the operating point, g_m increasing and $r_{b'e}$ decreasing as I_E increases. The value of $C_{b'e}$ increases with I_E and the depletion-layer capacitance $C_{b'e}$ varies as $1/(V_{CB})^{\frac{1}{2}}$ to $1/(V_{CB})^{\frac{1}{3}}$.

To obtain a wide bandwidth with the simple cascade of common-emitter stages shown in Fig. 3, the collector coupling re-

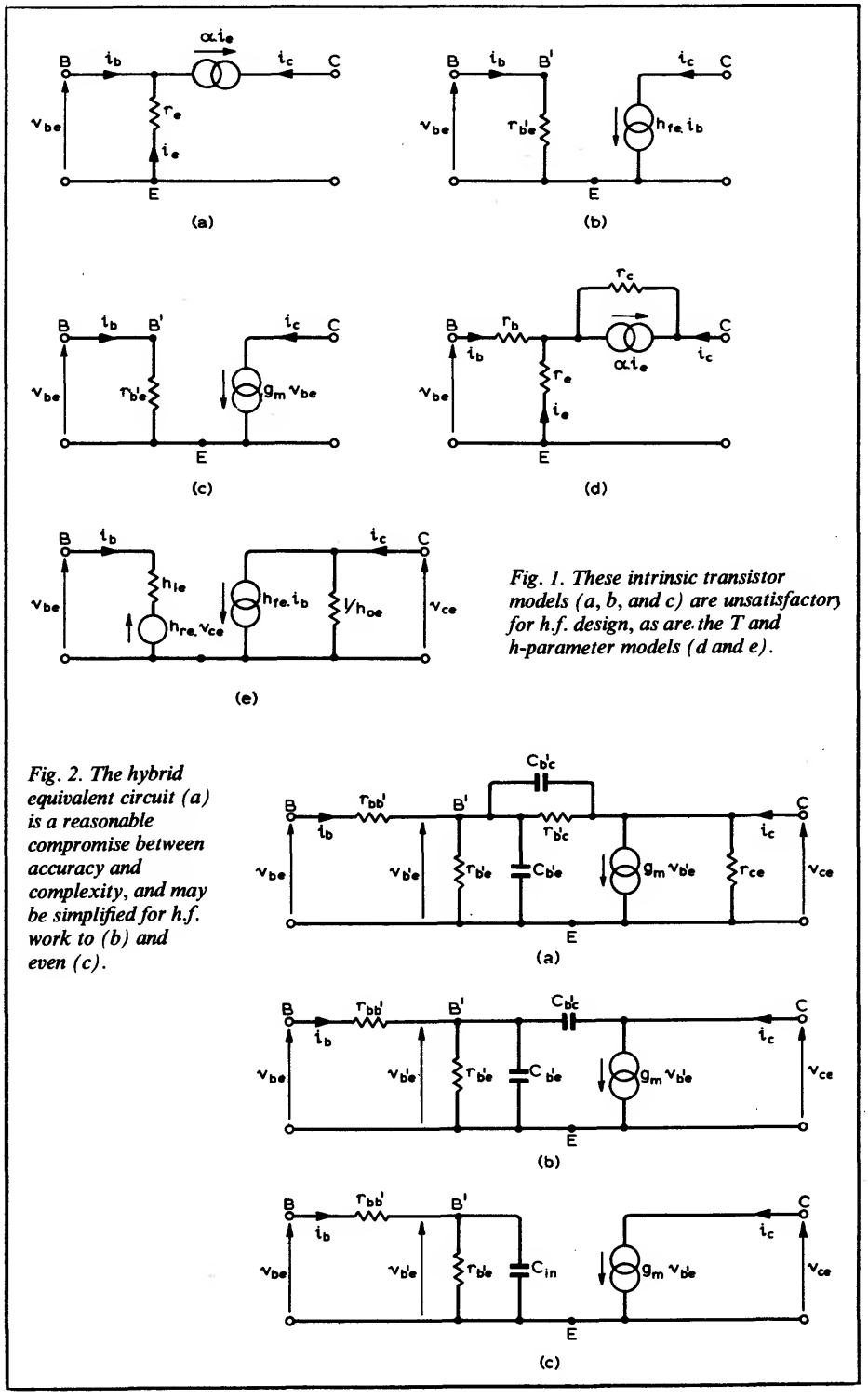


Fig. 1. These intrinsic transistor models (a, b, and c) are unsatisfactory for h.f. design, as are the T and h-parameter models (d and e).

Fig. 2. The hybrid equivalent circuit (a) is a reasonable compromise between accuracy and complexity, and may be simplified for h.f. work to (b) and even (c).

sistors must be made small compared with the input impedance of the following stage, the capacitive component of which causes the gain to fall at high frequencies. Further reduction of R_C to exchange gain for bandwidth is limited by the presence of $R_{bb'}$. Also, if the gain per stage is reduced, more stages must be cascaded to achieve a desired amplifier gain and it becomes increasingly difficult to maintain the overall bandwidth which shrinks as the number of cascaded stages increases. The gain-bandwidth product of the transistors (f_T) attains a maximum value at a particular value of emitter current, which is often small. Adjusting the emitter current of each stage to its optimum value may result in a small signal-handling capability if significant distortion is to be avoided.

Several techniques are available for improving the achievable stage gain-bandwidth product, the simplest of which is the inclusion of an inductor to compensate for the falling response due to transistor input capacitance. The stages in Figs. 4(a) and 4(b) are said to be shunt-peaked and series-peaked respectively, the latter being far less effective in improving gain-bandwidth product. The effect of the shunt-peaking inductor is illustrated in Fig. 5 and by correct design the stage bandwidth, for a given gain, can be improved by a factor of about two without lifting the high-frequency gain above its low-frequency value. Too large a value of L results in overcompensation which produces overshoot and ringing in the transient response. Amplifiers using a number of these stages in cascade may suffer from instability and prove difficult to align.

This problem may be alleviated by making the effective load on each transistor resistive. Referring to Fig. 6, this can be achieved by considering L and R_C to be in parallel with the series equivalent of the CR input network, making R_C equal to the equivalent series input resistance and designing L to produce the same short-circuit time constant for each of the parallel branches. A disadvantage of this constant-resistance cascade is that it is no longer possible to vary a network element to adjust amplifier gain or bandwidth, which must be attempted by variation of the transistor parameters, e.g. by adjusting the individual collector currents. The foregoing techniques have the disadvantage that all the cascaded stages interact, any change in the design of one stage normally requiring changes in the others.

As the input capacitance, including that due to Miller effect, plays an important part in limiting the achievable bandwidth, a design approach that attempts to eliminate the effects of internal feedback is useful. The cascode amplifier shown in Fig. 7 employs this technique and it may be considered as a common-emitter common-base cascade. The common-base stage has a very low input impedance, so the common-emitter stage has a current gain approaching h_{fe} and a very small voltage swing at its collector, resulting in a large reduction of the internal feedback between collector and base. The bandwidth of the common-emitter stage approaches f_β and as that of the common-base stage is much larger, the cascode pro-

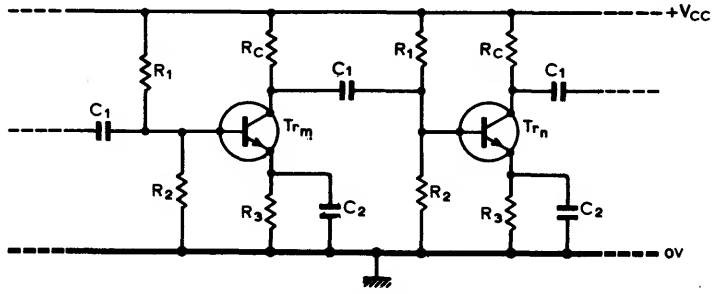


Fig. 3. Reducing R_c and increasing the number of stages can reduce overall bandwidth and give poor signal handling.

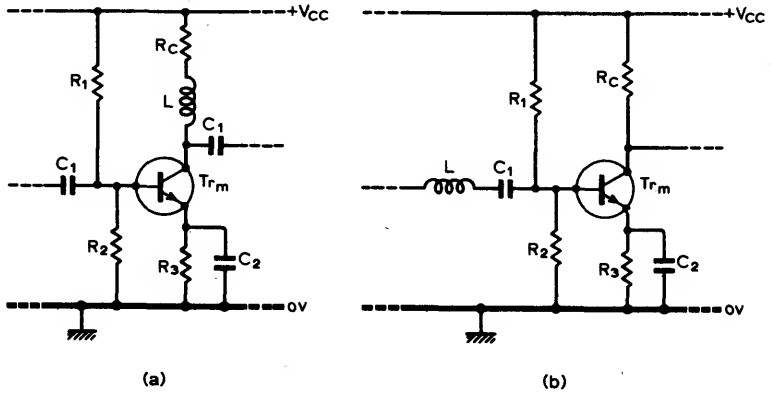


Fig. 4. Simplest way of improving bandwidth is to add shunt (a) or series (b) compensation. Effect of shunt peaking—the most effective—is shown in Fig. 5.

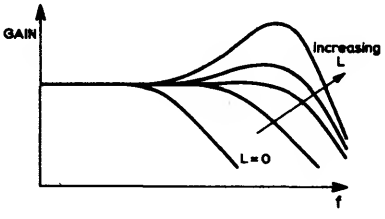


Fig. 5. Too large a value of L in Fig. 4(a) results in overshoot and ringing.

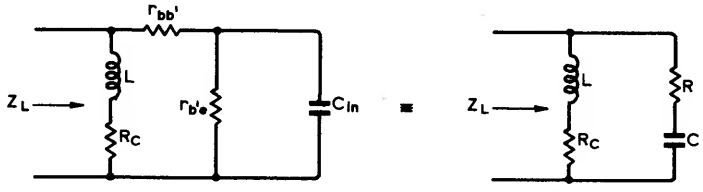


Fig. 6. To avoid instability in cascaded circuits of Fig. 4(a), the transistor load can be made resistive.

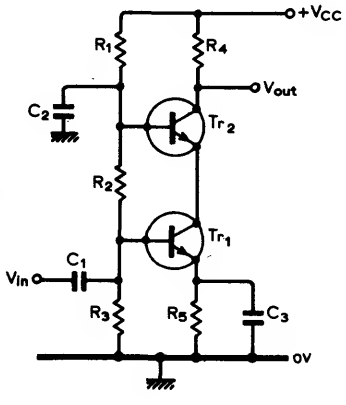


Fig. 7. Cascode circuit minimizes effect of internal feedback.

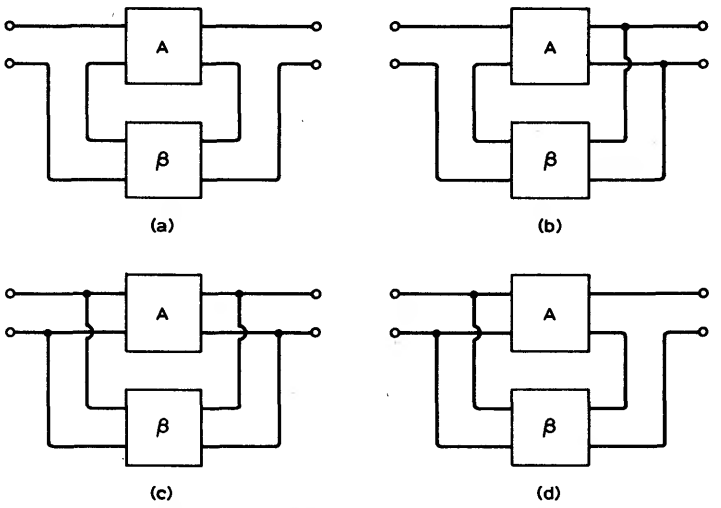


Fig. 8. Four basic ways of increasing bandwidth using negative feedback.

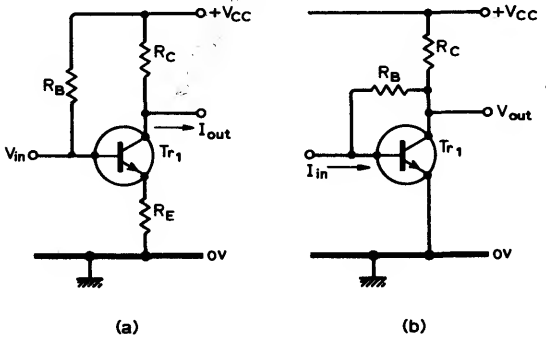


Fig. 9. Series and shunt feedback applied to a single stage.

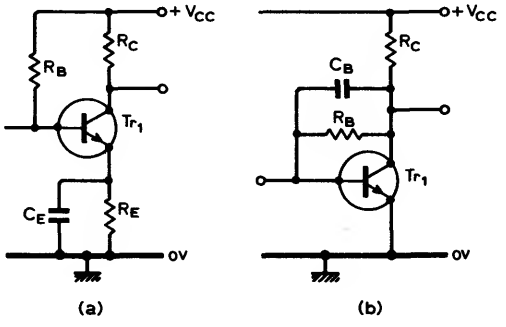


Fig. 10. Peaking capacitors improve h.f. response of Fig. 9.

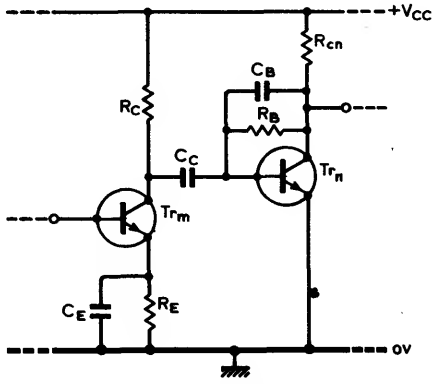


Fig. 11. Deliberate mismatching of impedances can improve stability.

vides the voltage gain and current gain of a common-emitter stage with a wider bandwidth than that obtainable with a simple common-emitter amplifier.

Satisfactory design of wideband amplifiers usually requires the interaction between individual stages or elementary building blocks to be negligible, or definable, the mid-band gain to be stable and input and output impedances to be adjustable to desired values. Use of feedback in the design allows these criteria to be approached without undue concern for the variations in transistor parameters and permits bandwidth to be extended at the expense of gain in a controllable manner. While the reduction in gain is a disadvantage it is not an expensive price to pay, bearing in mind the benefits obtained and the relatively low cost of adding extra feedback stages to meet the overall gain requirement.

Another disadvantage of feedback is the increased possibility of oscillation, which may be avoidable at the design stage by using a sufficiently accurate circuit model. In a multi-stage amplifier designed for the highest possible bandwidth before the application of feedback, the cut-off frequencies of all stages will normally be similar. Hence there is a near certainty that the combined phase shift can reach 180° while the magnitude of the gain is well in excess of unity. To remove this possibility, by deliberately setting one of the cut-off frequencies much lower than the others, negates the original requirement for maximum pre-feedback bandwidth. General-purpose operational amplifiers, such as the 741-type, have internal stages with high cut-off frequencies, but a dominant lag at about 10Hz has to be introduced to cope with the possibility of 100% feedback.

Four basic feedback configurations may be used to create elementary building blocks. Fig. 8 shows these configurations which may be described in terms of the method in which the feedback is derived and applied. Thus, (a) is series-derived series-applied, (b) is shunt-derived series-applied, (c) is shunt-derived shunt-applied and (d) is series-derived shunt-applied. Alternative descriptions of these configurations are in common usage e.g. (a) transimpedance feedback, series-series or simply series, (b) voltage-ratio feedback or series-shunt, (c) transadmittance feedback, shunt-shunt or simply shunt, and (d) current-ratio feedback or shunt-series. Other descriptions include the use of the terms current feedback or voltage feedback. In the former case the signal fed back is proportional to the output current but may itself be a current or a voltage. With voltage feedback the fed-back signal is proportional to the output voltage. All four arrangements have the property of increased bandwidth and reduced gain compared with the open-loop values. The input and output impedances become modified as shown in the table, shunt derivation (application) reducing the output (input) impedance and series derivation (application) increasing the output (input) impedance.

The two types of single-stage feedback, series and shunt, are shown in Fig. 9. In Fig. 9(a) the load impedance should be low and the input supplied from a voltage source

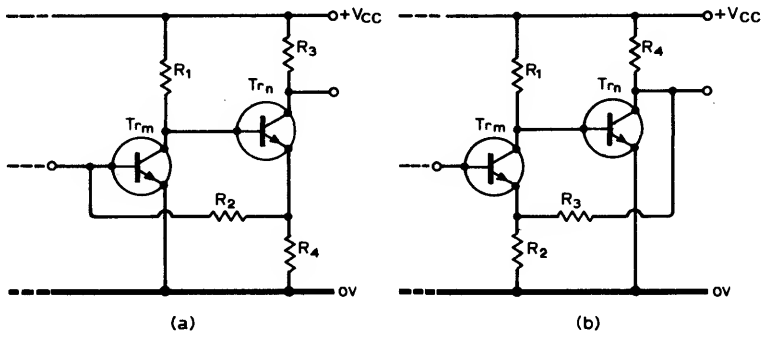


Fig. 12. Widely differing input and output impedances make two-stage feedback circuits useful for cascading.

whereas in Fig. 9(b) the load impedance should be high and the amplifier input should be from a current source. The high-frequency response of these elementary blocks may be improved by the addition of peaking capacitors as shown in Fig. 10.

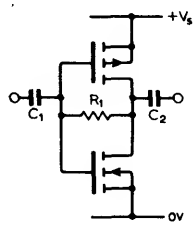
Source and load impedance requirements for stable gain with single-stage feedback can be met by purposely creating a large mismatch between cascaded stages, i.e. by alternating series and shunt feedback stages as shown in Fig. 11. With this arrangement gain-bandwidth product is high, low-frequency gain may be determined with reasonable accuracy by multiplication of individual stage gains, and there is little interaction between stages. Feedback applied to two stages can offer similar merits, Figs. 12(a) and 12(b) showing series-derived shunt-applied and shunt-derived series-applied configurations respectively. Both networks have widely differing input and output impedances and are therefore attractive as basic building blocks for cascaded stages.

Although discrete devices may be used in a multistage realization, the availability of integrated-circuit transistor arrays, containing about five transistors with parameters inherently reasonably matched, are very attractive for many designs. Integrated circuits are available in the form of a long-tailed pair which can be operated as single-ended or differential-input wideband amplifiers by the addition of external passive components that allow a high degree of flexibility in the selection of gain, bandwidth and signal-handling capability.

Other integrated circuit versions provide emitter-follower input and output transistors to make the input and output impedances high and low respectively. Integrated wideband power amplifiers can be obtained providing bandwidths up to about 8MHz and outputs of about 14V pk-pk. Integrated circuits containing pairs of cascode amplifiers and some with gating facilities are also very useful as wideband amplifiers. Modern integrated-circuit logic gates designed for high-speed switching applications may also be usefully employed as low-cost wideband amplifiers by setting the quiescent conditions in a linear part of the transfer characteristic and employing feedback to define the gain.

Feedback type	Z_{out}	Z_{in}
Fig. 8(a)	increases	increases
Fig. 8(b)	decreases	increases
Fig. 8(c)	decreases	decreases
Fig. 8(d)	increases	decreases

High input impedance c.m.o.s. amplifier



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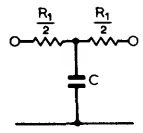

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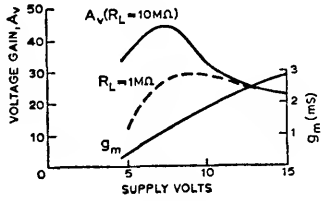

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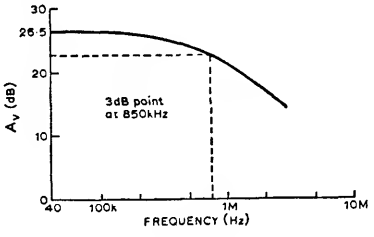


4

Circuit description

C.m.o.s. circuits have been designed for digital systems. Basic building block is the inverter consisting of a complementary pair of enhancement-mode m.o.s. devices with threshold voltages in the region of 1.7V and peak current capabilities of a few tens of milliamperes at maximum forward bias. Input resistance is extremely large with the leakage currents of the protection diodes as the limiting action. The individual device g_m is around 1 to 2mS for forward gate-source voltages in excess of 5V. Biased in the linear mode, the devices each have $|V_{gs}| \approx V_s/2$, so maximum forward bias is $\approx$7.5V for the rated supply voltage of 15V. This restricts the upper value of g_m that can be attained. In the absence of an external load resistance the voltage gain is limited by the finite slope resistance. An unusual property of this circuit is that the voltage gain falls with increasing supply voltage, as the relatively small rise in g_m is more than offset by the fall in output slope resistance at the higher resulting currents.

The disadvantage of operating at low supply voltages (and hence currents) is that the voltage gain is more load-dependent and the upper cut-off frequency falls sharply. To maximize the input resistance while using d.c. negative feedback to stabilize the operating point, the feedback resistor is decoupled (see Fig. 2). Gate current is negligible and the input and output quiescent voltages are equal.

Other c.m.o.s. devices using different fabrications, e.g. silicon gate, ion implantation, offer greater bandwidths and/or lower threshold voltages. Complementary m.o.s. circuits designed for the linear market have been recently announced.

Component changes

IC_1: Any c.m.o.s. inverter including CD4001 NOR gate, CD4009/CD4049 inverting buffers, MC1407, MC14009 and other equivalents.

R_1: 220k to 22MΩ.

C: Sets the lower frequency at which the negative feedback becomes operative, reducing the input impedances. 0.1 to 10μF (time constant $R_1C/2$).

C_2: Depends on load which, with this circuit, cannot be very low unless transconductance properties alone required with little voltage gain. 0.1 to 100μF.

V_s: 3 to 15V. At voltages below 5V the quiescent current becomes very small and output impedance is very high.

Circuit modifications

● Negative feedback may be applied over any odd number of inverting stages, e.g. over three as in the circuit shown left. Multiple phase shifts within the amplifier, together with the high voltage gain available, make the method difficult to apply without precautions. Open-loop gains of 80dB and greater may occur. Even decoupling the feedback still allows oscillation at low frequencies via the coupling/decoupling/supply time-constants.

● A better method of controlling gain than simply attenuating it is to cascade stages with shunt and series negative feedback as shown centre where inserting a resistor in the source of each device in stage 1 reduces and defines the transconductance. Shunt feedback across stage 2 defines its transresistance and the combination has a lower but well-defined voltage gain.

● Because the above amplifier is non-inverting, d.c. feedback may be applied via the third stage used purely as a d.c. coupling element linking A-A′, B-B′, with the overall a.c. feedback decoupled.

Further reading

RCA, COS/MOS Digital Integrated Circuits, 1973, pp. 24–30, pp. 37–42, p. 346, p. 355.

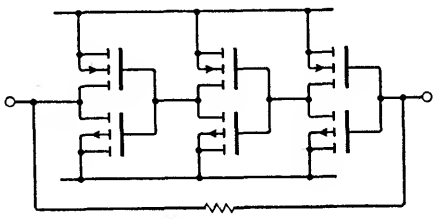
Wujek, J. H. Field-effect transistor circuits, in Electronic Circuits Manual by J. Markus, McGraw-Hill 1971, p. 22.

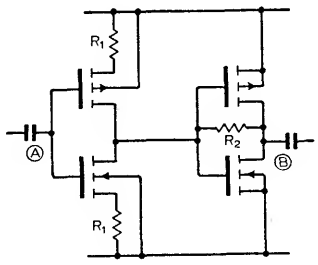
Ferranti Ltd., FET Source Follower and Bootstrapped FET Source Follower, FETs and Applications, no. 22, 1965.

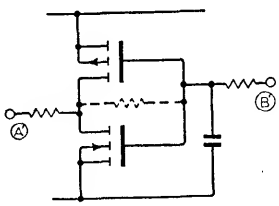
Cross references

Set 12, cards 4 & 7.
Set 11, cards 5 & 6.

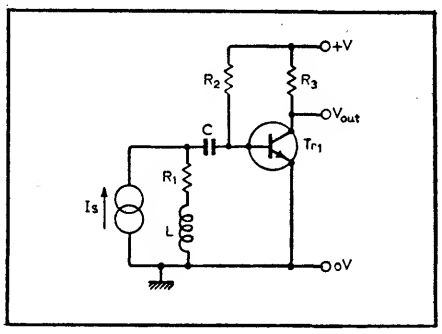
Circuit modifications



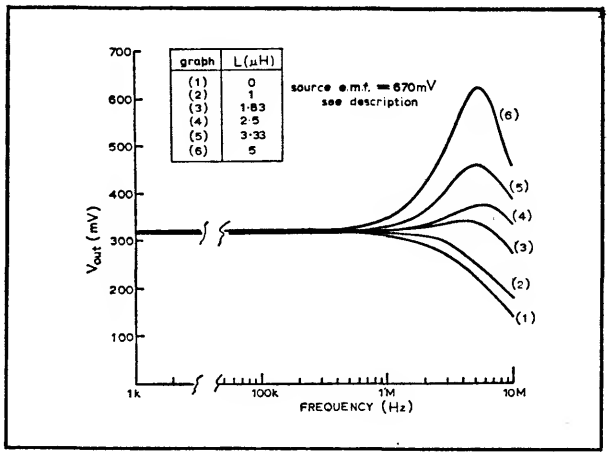




Shunt-peaked wideband amplifier



Circuit data/
Supply: +6V, 4.5mA
Tr_1: 1/5×CA3046
C: 10μF tantalum
R_1: 68Ω; R_2: 100kΩ
R_3: 680Ω
L: 1.83μH (38 turns 28 swg, close wound on 0.2in dia.)



Circuit description
Bandwidth of a common-emitter amplifier may be extended by including an inductor in shunt with its input producing a shunt-peaked amplifier. The circuit is fed from a current source, or alternatively in a cascaded amplifier R_1 and L may be used as the collector coupling network of each stage which is loaded by the input impedance of the following transistor.
Because the gain-bandwidth product of a transistor varies with its collector current, R_2 was chosen to maximize the gain-bandwidth product for the device used. Resistor R_3 was chosen to make $V_{CE} \approx +V/2$ and R_1 to provide the desired low-frequency current gain. Source resistance was 100Ω, so a current source was simulated by a chain of ten 1-kΩ resistors in series to reduce the effect of the shunt capacitance of a single 10-kΩ resistor on the measured high-frequency response.
With $L=0$, amplifier input voltage falls with increasing frequency due to transistor input (and Miller effect) capacitance. With L in circuit, low-frequency response is the same but a low-Q resonance occurs between L and C_{in} of the transistor, causing the response to peak as the frequency is raised towards its original cut-off value.
By designing L on the basis of available transistor parameter data and the required current gain, it is possible to produce a maximally-flat gain response while maximizing stage gain-bandwidth product.
Alternatively, a good starting point is to use the measured low frequency input resistance and upper cut-off frequency with $L=0$ to estimate C_{in} and then design L to resonate with this value in the region of the desired cut-off frequency with the peaked response. (See curve 3 above.)

Component changes
Useful range of supply +3 to +30V. Values of R_2 and R_3 should be adjusted to produce f_T max. for transistor if maximum stage gain-bandwidth product is to be achieved. Select R_1 to give desired low-frequency gain, and C to give desired lower cut-off frequency. High-frequency response may be tailored to suit requirements by choice of L value. (See curves 2, 4, 5 & 6.)

Circuit modifications
● Up to five cascaded stages may be obtained with the same integrated circuit package but it may prove easier to obtain the desired response experimentally than by calculated design. Problems of alignment and possible instability due to inter-action between cascaded shunt-peaked stages can be alleviated if each transistor feeds a resistive load. The load on each device consists of L and R_1 in parallel with the input impedance of the following stage, as shown left. Load impedance may be made purely resistive by adjusting the values of R_1 and L to be $r_{bb}'(r_{bb}'+R_{in})/R_{in}$ and $C_{in}r_{bb}'$ respectively, where r_{bb}' the transistor base spreading resistance. In such a constant-resistance cascade, L and R_1 cannot be used to adjust the gain and bandwidth of the amplifier which must be trimmed by adjusting the collector currents of the transistors.
● A series-peaking inductor may be connected between a low-impedance source and the base, as shown centre, to extend the bandwidth. Stage gain-bandwidth product is less than for the shunt-peaked arrangement and its maximum value cannot be achieved with a maximally flat response.
● Another high-frequency compensation network, widely used in pulse applications, is shown right. Bandwidth may be extended by making $R_1C_1 = R_{in}C_{in}$ but the stage gain-bandwidth product, while constant, does not approach that of the shunt-peaked stage. However the constancy of the gain-bandwidth product does allow exchange of gain for bandwidth by adjusting R_1.

Further reading
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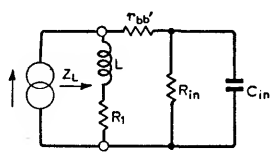
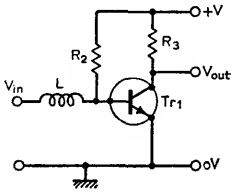
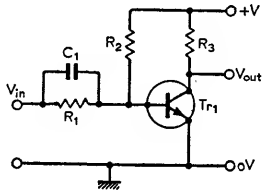
Markus, J. Electronic Circuits Manual, McGraw-Hill, 1971, p. 913.

Cross references
Set 12, cards 5, 9 & 12.
Set 7, card 9

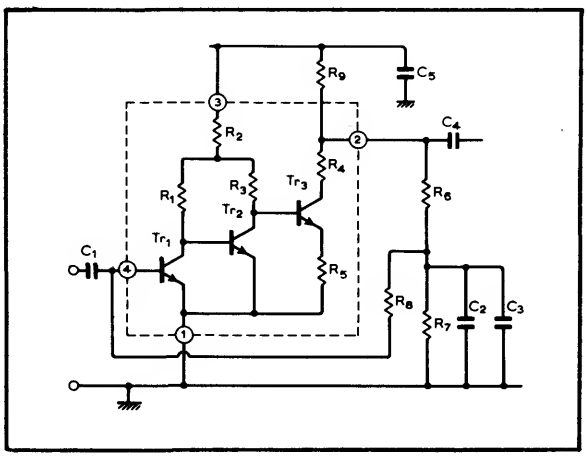
Circuit modifications







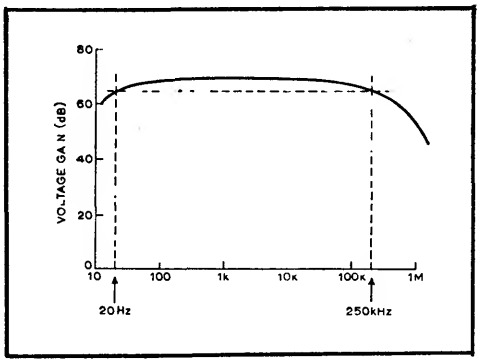
High-gain wideband amplifier



Typical performance

R_6	33kΩ	R_7	15kΩ
R_8	2.2kΩ	R_9	10kΩ
C_1	20μF	C_2	10nF
C_3	64μF	C_4	10μF
C_5	100nF		

IC MFC4010A
V_S +6V
f 100Hz to 50kHz
Voltage gain > 3000 (70dB)
Cut-off 250kHz
Input resistance 700Ω
Output resistance 8.5kΩ



Circuit description

This amplifier uses an integrated circuit developed for consumer applications. It is simple in design, consisting of three common-emitter transistors directly coupled so that the collector potentials of Tr_1, Tr_2 are defined by the base potentials of Tr_2, Tr_3 respectively, i.e. they are at ≈0.6V. Resistor R_5 has a low value with only a marginal effect on these potentials.

Output potential is forced by the feedback effect via R_6, R_7, R_8 to be some defined multiple of the base potential of Tr_1.

If $R_8 < R_6$, R_7 then the output p.d. to ground is $\approx(R_6/R_7+1)$ V_{be1} and would typically be set near the supply mid-value.

Current in each stage increases with increasing supply voltage, and as a result both open-loop gain and bandwidth increase. Increased current also reduces the input impedance. Resistor R_9 determines quiescent output current provided output voltage has been fixed by feedback as outlined above. As there are three stages all contributing phase shift, the total phase shift is in excess of 180° before the magnitude of the gain falls towards unity. Hence it is difficult to apply heavy negative feedback to extend the bandwidth at the expense of gain as can be done with amplifiers using common-emitter stages. (For audio frequency applications it is possible to control the feedback to produce defined characteristics as for tape recording/playback amplifiers.) As the high gain extends to high frequencies, $A_v \approx 100$ at f=4MHz, proper grounding, decoupling and use of short leads, screened where appropriate are all important.

Component changes

IC: No direct replacements but groups of three transistors from CA3046 and similar multi-transistor packages may be used.

R_6, R_7: Ratio fixes output quiescent voltage $\approx(R_6/R_7+1)$ 0.6V. Resistors may be increased to minimize loading on output, but base current of Tr_1 becomes significant factor in determining quiescent conditions. Typical range 5k to 50kΩ.

R_8: Also limited by base current effects, but may be increased up to 10kΩ to maximize input resistance of circuit if required.

R_9: Determines output stage quiescent current and hence maximum load current. No advantage to making too high since current in preceding stages fixed by internal resistors. 2.2k to 22kΩ.

$+V_S$: 2 to 18V. At low voltages, gain falls sharply Choose R_6, R_7 in conjunction with V_S to bias output near mid-point of supply for maximum output swing.

C_1, C_3, C_4: Determine low frequency cut off. Maintain ratio increasing values for pro rata fall in cut-off. C_4 may be reduced greatly if feeding high impedance load.

Circuit modifications

● Any group of three transistors may be used in similar configurations. Simple arrangement (left) for low-voltage applications where output quiescent voltage of 0.6V would be adequate. Again decoupling of feedback essential since gain/phase properties too complex for application of heavy negative feedback. Resistors R_1 to R_5 may be comparable value resistors (1k to 10kΩ) though R_4, R_5 may be higher if somewhat higher output direct voltage desired.

● By using complementary transistors, each transistor has current defined by V_{be} of succeeding stage. This makes current and gain/bandwidth less dependent on supply voltage (middle). Complementary versions of each form are equally possible, reversing the supply voltage.

● The good high frequency gain allows its use in 10.7MHz i.f. applications (right) with the d.c. feedback applied via the input tuned circuit and the output taken to a ceramic filter. Similar principles apply at 470kHz but the high voltage gain makes careful design obligatory. In all r.f. applications drive from a 50Ω source is normal, but the output impedance of the circuit is relatively high.

Further reading

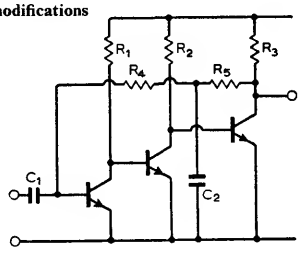
Motorola Linear Integrated Circuits Data Book, 2nd edition 1972, pp. 7–561 to 7–564.

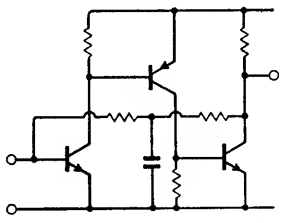
CA3095E Wideband Amplifier, RCA Databook SSD-201A, 1973, p. 249.

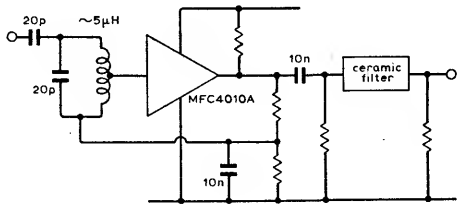
Cross references

Set 12, cards 5, 10 & 11.

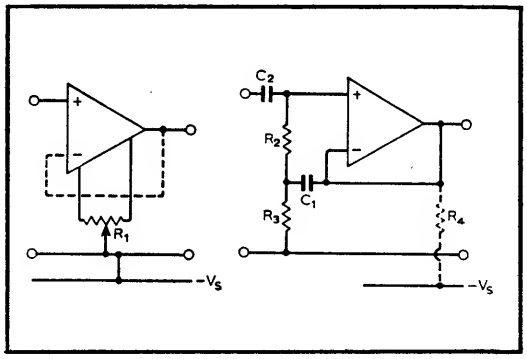
Circuit modifications







Wideband voltage followers



Circuit data
IC: LM310
R_1: 1kΩ
R_2, R_3: 100kΩ
R_4: 3.3kΩ
C_1: 2.2μF
C_2: 0.01μF
Supply: ±15V

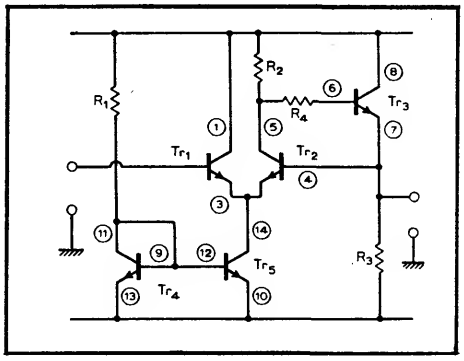
Circuit description
A specially-designed monolithic voltage-follower, the 310 has a combination of highly desirable parameters: high input impedance, low output impedance, and wide frequency range. The negative feedback is connected internally but some modifications to performance that can be made externally include offset zero by means of R_1, increased output current capability by preloading with R_4 at the expense of increased dissipation, and a.c. coupling to source, bootstrapping the bias resistors R_2, R_3 to minimize loading effects.
Slew-rate limitations imposed by the maximum charging rate of an internal compensation capacitor, mean that the large signal bandwidth is much less than small signal bandwidth—true of amplifiers having heavy negative feedback in general.

Performance
Upper cut-off frequency for small signals.
15MHz for zero source resistance, 2MHz for 10kΩ. At 1MHz, output impedance is 25Ω, output voltage swing is ±3V, and input impedance is 3pF plus strays.

Component changes
IC: Direct replacements from many manufacturers. Any op-amp compensated for 100% negative feedback may be used. In general it will not be possible to achieve the same spread of parameters, i.e., high input impedance may preclude wide bandwidth.
R_2, R_3: Increase for higher Z_{in} at expense of increased offset.
C_2, C_1: Determine lower cut-off frequency (with R_1, R_3). Combination gives inductive term to input impedance at low frequencies. 0.1 to 10μF.
R_4: Increases negative current capability at expense of dissipation.
V: ±5 to ±15V (down to ±3V in extreme cases).

Further reading
LM110—An Improved IC Voltage Follower, National Semi-conductor Linear Applications Handbook, 1972, p. LB11-1 and 2.
Campbell, T. C. Application note ICAN-5213, in RCA Databook SSD-202, 1972, pp. 203–4.
Markus, J. Electronic Circuits Manual, McGraw-Hill, p. 13.

Cross references
Set 12, cards 1 & 11.
Set 7, card 3.



Circuit data
Tr_{1-5}: CA3046
R_2: 3.9kΩ
R_1: 4.7kΩ
R_3: 1kΩ
R_4: 1kΩ
Supply: ±2.5V

Circuit description
Using the five transistors in an i.c. package (CA3046), this is a simple wide-band voltage follower. A similar circuit could be used with discrete transistors replacing current mirror Tr_4, Tr_5 by a similar current source or by a single resistor particularly if the supply voltages were higher. Transistors Tr_1, Tr_2 are the differential pair comparing input with output, the use of a monolithtic pair giving good temperature drift. Transistor Tr_3 is an emitter follower within the feedback loop. Resistor R_4 may be required to suppress very high frequency oscillations (dependent on circuit layout). Not shown, but generally important, is the decoupling of the supply voltages as close to the i.c. as possible—typically 0.01 to 1μF.

Performance
Upper cut-off frequency ≈4.5MHz.
Output impedance ≈10Ω.
Input impedance: ≈100kΩ.
Output voltage swing ≈2.5V pk-pk at 100kHz.

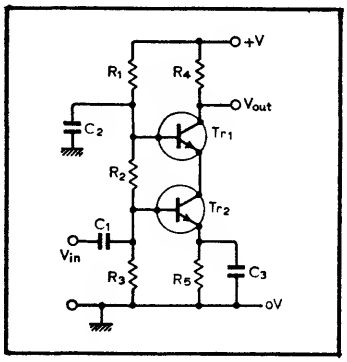
Circuit modifications
● Replace Tr_4, Tr_5 by any other constant current source (or even resistor, with reduced stability against supply changes).
● Increase open-loop gain output capability, by replacing R_2, R_3 with constant current sources.
● Replace Tr_3 by common emitter p-n-p transistor taking signal from Tr_1 collector instead. Higher open-loop gain, greater output swing capability, greater likelihood of oscillations requiring compensating capacitor, e.g., collector-base of Tr_3.

Component changes
IC: CA3046, CA3045, CA3086.
R_1: 1kΩ to 100kΩ. Lower values increase bandwidth and dissipation.
R_2: Set to carry half current in R_1 (assuming unity ratio for current mirror). Typically $R_1 \approx R_2$.
R_3: Low values maximize output swing and dissipation 330Ω to 33kΩ.
V: ±2 to ±7½V. Higher voltages possible if discrete transistors used.

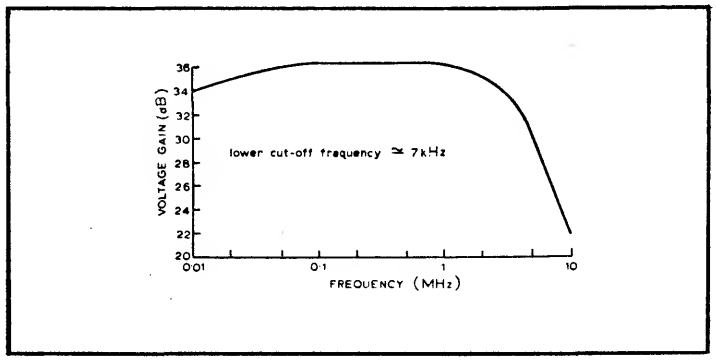
wireless world circard

Series 12: Wideband amplifiers—5

Bipolar cascode wideband amplifier



Circuit data
Supply: +6V, 1.2mA
Tr_1, Tr_2: 1/5×CA3046
R_1: 39kΩ; R_2: 3.3kΩ
R_3: 33kΩ; R_4: 2.2kΩ
R_5: 1kΩ
C_1, C_2, C_3: 1μF
V_{in}: 10mV r.m.s.



Circuit description
The bipolar transistor cascode amplifier offers very good isolation between its input and output ports, so that the possibility of instability is virtually non-existent for all types of load. Input transistor Tr_2 acts as a common-emitter stage which is loaded by the upper transistor connected in the common-base configuration and having a very low input impedance. Thus the common-emitter stage has a current gain approaching h_{fe} and the voltage swing at its collector is very small, producing a significant reduction of the internal feedback between collector and base. Bandwidth of the common-emitter stage approaches f_β and as that of the common-base stage is much larger, the complete circuit behaves like a common-emitter amplifier as far as voltage gain and current gain are concerned, but has a wider bandwidth than is achievable with a simple common-emitter stage providing the same high voltage gain.
A reasonable estimate of the 3-dB bandwidth obtainable with the cascode amplifier may be made using available data and the relationship: gain-bandwidth product $(f_T) \approx h_{fe} \cdot f_\beta$ if it is assumed that h_{fe} and f_β are the approximate current gain and bandwidth values for the whole circuit. Each of the transistors in the integrated circuit array has typical h_{fe} and f_T values of 110 and 450MHz respectively, with $I_C \approx 1.2$mA giving $f_\beta \approx$ 4.1MHz. (Measured upper 3dB cut-off frequency was approximately 3.7MHz for the circuit.)

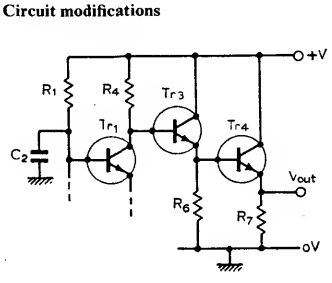
Component changes
Useful range of supply +2 to +30V.
V_{in}(max) ≈ 40mV(pk-pk).
Midband gain falls by 3dB when output is loaded with approximately 6.8kΩ (capacitively coupled).
Upper cut-off frequency largely determined by R_4 for given transistors.
Lower cut-off frequency adjustable by changing C_1, C_2 and C_3. Tr_1 and Tr_2 may each be replaced by ¼×CA3018 or equivalent discrete devices e.g. 2N706-type.

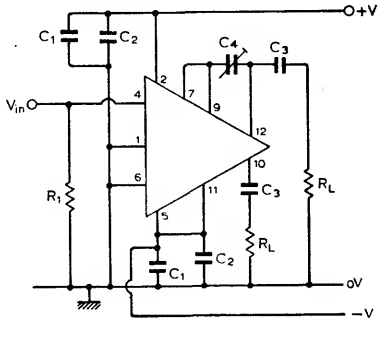
Circuit modifications
●One of the differentially-connected pair of transistors in the CA3046 package may be connected as an output emitter-follower stage to provide a low output impedance cascode amplifier. If a CA3018 package is used, all four transistors may be used by following the cascode with a pair of cascaded emitter followers as shown left. In this form, with R_6=3.3kΩ and R_7=2.7kΩ a voltage gain of about 36dB is obtainable with an upper cut-off frequency of approximately 11MHz.
●A pair of cascode stages with a common tail resistor may be used as a differential cascode amplifier. This arrangement is the basis of the CA3040 integrated circuit wideband amplifier, which employs high-input-impedance emitter-follower buffer stages between the input terminals and the common-emitter sections of the cascodes. Outputs from the cascode common-base stages are fed to the output terminals via emitter followers to produce a reasonably low output impedance.
●Centre circuit shows the CA3040 connected to a pair of equal load resistors (R_L) which receive antiphase outputs. With the amplifier connected to a 50-Ω source and R_L=50Ω the voltage gain to each output is about 22dB with a bandwidth of approximately 30MHz. The values increase to about 32dB and 50MHz respectively when R_L is raised to 1kΩ and the bandwidth may be increased to about 90MHz by including the input series peaking circuit shown right. Supplies must be decoupled with capacitors C_1 and C_2 at the integrated-circuit package pins and ferrite beads on the supply leads and careful printed circuit layout are necessary. Supply ±6V, R_1 50Ω, C_1, C_3 100nF, C_2 1nF, C_4 is a small trimmer to adjust high-frequency gain and phase balance.

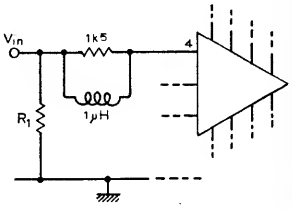
Further reading
Theriault, G. E. et al. Application of the RCA-CA3018 Integrated-Circuit Transistor Array, RCA Databook SSD-202 1972, pp. 68–70.
Austin, W. M. Principal Features and Applications of the RCA-CA3040 Intregrated-Circuit Wideband Amplifier, RCA Databook SSD-202, 1972, pp. 171–81.

Cross references
Set 12, cards 2, 3, 7 & 12.
Set 7, card 5.

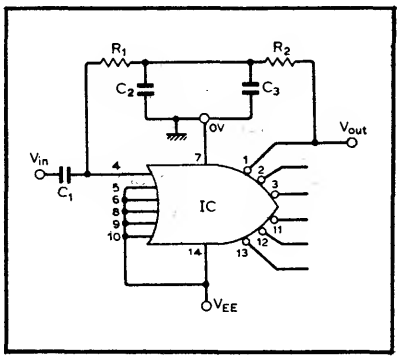
Circuit modifications







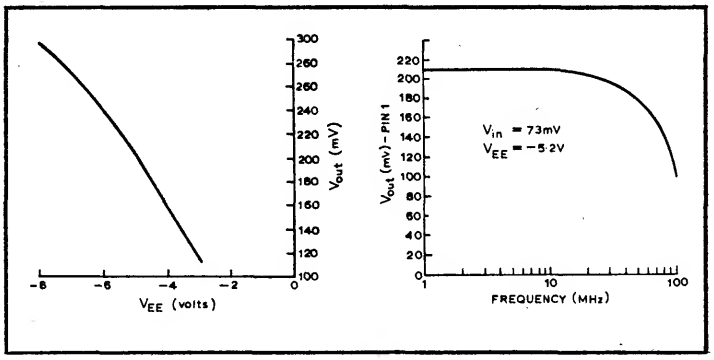
Wideband amplifier using e.c.l.



Typical performance

V_{EE}	−5.2V, 20mA
R_1, R_2	390Ω
C_1	100nF, C_2 100pF
C_3	1μF tantalum
IC	MC1001

Voltage gain (l.f.) 2.89
V_{in} 73mV r.m.s.



Circuit description

The integrated circuit is an emitter-coupled logic gate designed for high-speed digital applications. This type of gate has an input stage consisting of a long-tailed pair with multiple inputs to one half of the pair via separate transistors having their collector-emitter paths in parallel. Each half of this differential stage feeds an emitter follower output stage, a number of which may be paralleled within the package. Thus, at least one inverted and at least one non-inverted output is available and the logic gate may be used as a linear, wide-band amplifier provided it is correctly biased, for example by means of R_1 and R_2 as shown above. This simple arrangement of connecting one of the logical NOR outputs back to the input provides self-biasing of the gate that ensures that the d.c. input and output voltages are the same except for the small drop across R_1 and R_2. This is only possible if the gate is operating in the middle of its transfer characteristic, the arrangement automatically compensating for changes in bias and offset voltages.

Only the d.c. component of the output signal is fed back to the input, C_2 and C_3 decoupling the a.c. component. Capacitor C_1 prevents any d.c. component of the input signal from disturbing the self-biasing conditions. The a.c. signal voltage available at the NOR output used to derive the feedback, is typically 3 to 4% lower than that obtainable from other NOR outputs, and is approximately 9 to 10% higher than at the unloaded NOR outputs.

Careful printed circuit layout is required if a smooth, high-frequency roll-off is to be obtained in the frequency response.

Component changes

Useful range of $V_{EE} \approx -3$ to -8V (see graph).

Minimum load resistance for 10% fall in mid-band gain ≈ 270Ω (a.c. coupled via 100nF capacitor).

Distortion is less than 1% for V_{in} in the range approximately 1 to 20mV and useful V_{in} (max) without significant distortion is approximately 200mV pk-pk.

For bandwidths in excess of 300MHz use MC1660.

Circuit modifications

- More than one input of the gate may be used to increase gain by connecting others in parallel, but the offset voltage between output and input rises as the number of paralleled inputs increases. This may not be a severe disadvantage in certain applications.
- The simple self-biasing arrangement may be applied over several e.c.l.-gate amplifying stages, as shown left.
- A given total bias network resistance (R_1+R_2) may be decoupled asymmetrically. For example, if it is required that the bias-network loading of the output be reduced without changing (R_1+R_2), values such as those shown centre may be used. This will cause the input impedance of the amplifier to fall from about 390Ω to about 220Ω.
- The biasing arrangement may be changed to allow an increase in both the input and output impedances without changing the d.c. input and output voltages. One such arrangement is shown right, where the junction of R_1 and R_2 may be returned to the 0-volt rail through a suitable-value, additional bias resistor R_3. For example, with R_1, R_2 2.2kΩ, a suitable value for R_3 would be around 47kΩ. This arrangement slightly increases voltage gain.

Further reading

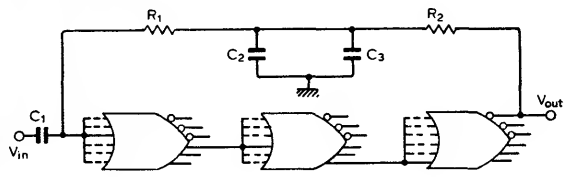
Using e.c.l. gates as wideband amplifiers, *Electronic Engineering*, June 1973.

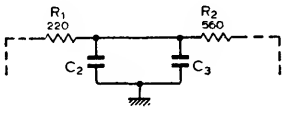
MECL Integrated Circuits Data Book, Motorola, 2nd edition, 1972, pp. 5–3 to 5–6 and pp. 4–17 to 4–20.

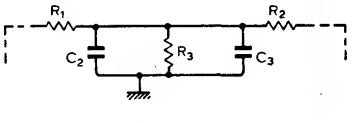
Cross references

Set 11, card 7.
Set 12, cards 8 & 10.

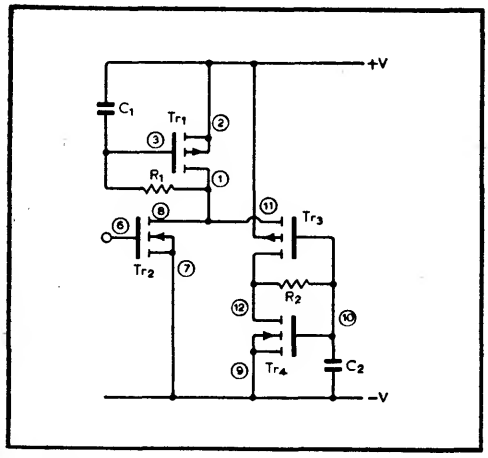
Circuit modifications



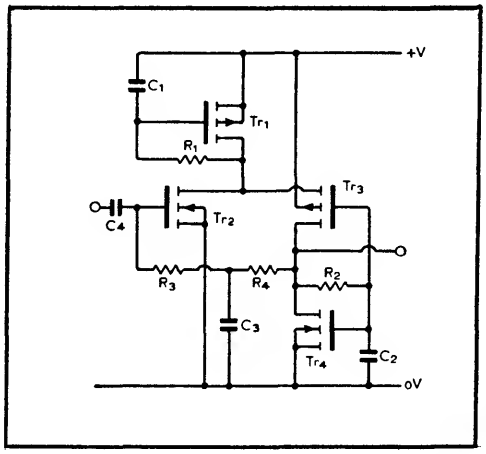




FET cascode amplifiers



Circuit data
Supply: ±7.5V
IC: CD4007AE
R_1, R_2: 1MΩ
C_1: 0.1μF; C_2: 0.33μF
Voltage gain: ≈26(R_L 33kΩ)
Cut-off frequency: 320kHz
Alternative bias for single supply: R_3, R_4: 1MΩ
C_3: 1μF; C_4: 0.01μF



Circuit description
The basic principle of a cascode stage is that of a common-emitter or common-source amplifier feeding directly into a common-base or common-gate stage, so that the first stage feeds into a near short-circuit. This allows it to develop its maximum current gain or transconductance, but more important the voltage swing at the collector or drain is small. Large voltage swings produce relatively large currents in the inevitable feedback capacitance, with a corresponding heavy shunting effect at high frequencies. This reduction in feedback (commonly called the Miller effect though first discussed by Blumlein) is of particular importance in wideband and r.f. amplifiers. In particular, the better the isolation between input and output the higher the gain that can be achieved consistent with stability. The devices need not be in series for d.c. purposes though this is more common.
In the circuit shown, based on a low-cost c.m.o.s. i.c., Tr_2 is a common-source stage whose output signal current is diverted into Tr_3 provided that Tr_1 has a high dynamic impedance at a.c. (see circuit modifications). The voltage gain of the cascode pair is equal to or greater than the highest voltage gain obtainable from a single stage, while coupling between output and input is minimized.
An alternative version is shown in which a decoupled d.c. feedback path via R_3, R_4 gives self-biasing (with a.c.-coupled source). The high input resistance of the m.o.s. devices together with the possibility of operation at $V_{dg}=0$ allows for simple biasing networks and offsets the disadvantage of the wider tolerance on m.o.s. devices as against bipolar transistors.

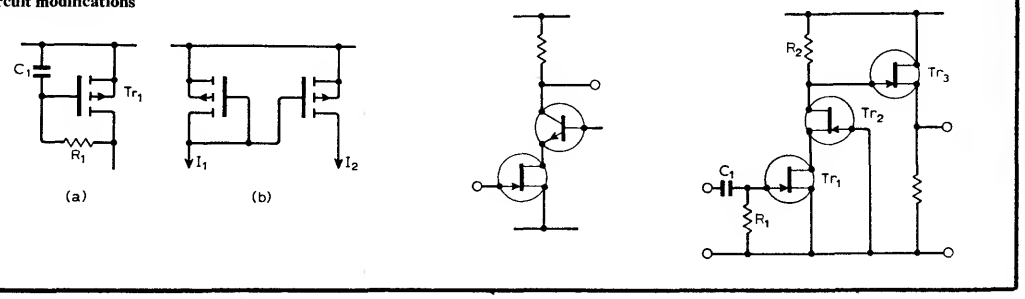
Component changes
IC: Equivalents of CD4007AE including MC14007, etc.
Other combinations of enhancement-mode m.o.s.f.e.ts may function but simpler circuits can be devised for these. This circuit was intended to make best use of this low-cost i.c.
Supply voltage: Positive voltage may need to be increased with some devices; negative rail is then reduced accordingly to stay within rating.
R_1, R_2, R_3, R_4: Not critical. 100kΩ to 22MΩ. With low resistances, low-frequency time constants are raised unless large capacitances used, while input impedance falls for second version. Very high resistances bring noise/hum/leakage problems.
C_1, C_2, C_3, C_4: High values to improve low-frequency response if required.

Circuit modifications
● The high impedance of the circuit is possible because the p-channel enhancement-mode m.o.s.f.e.t. can still have the drain well beyond the knee of its characteristics if biased with drain and gate at equal quiescent potentials. Provided the a.c. applied to the drain is adequately decoupled by R_1C_1, the dynamic impedance approaches that of the drain-source (R_1 may be very large and still achieve correct bias). The current mirror approach retains the high dynamic resistance down to d.c. at the expense of a second m.o.s.f.e.t., Fig. (b).
● Cascode circuits may have the devices in series, sharing the same d.c. current (rather than in parallel as with the complementary stage above). If the input device is a junction f.e.t., the simplest circuits demand only a bipolar transistor with base potential set to a value in excess of the pinch-voltage of the f.e.t. to achieve good cascode performances. The f.e.t. determines the input performance including very high input impedance at low frequencies, while the cascode configuration extends the high impedance to higher frequencies while allowing higher overall gain.
● All f.e.t. circuits are equally possible provided Tr_2 has a higher V_p than Tr_1. Transistor Tr_3 is a source follower to isolate the load R_2 from stray and load capacitances, i.e., increasing bandwidth of output circuit.

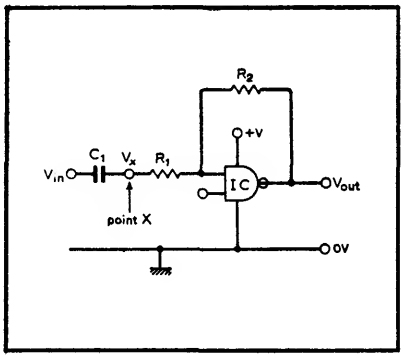
Further reading
FET Circuit Applications, National Semiconductor Linear Applications Handbook, 1972, p. AN32–2.
Schade, O. H. Jr. Application note ICAN-6080, in RCA Data Book SSD-203A, 1973, pp. 299–300.

Cross references
Set 12, cards 1 & 5.
Set 11, cards 5 & 6.
Set 7, card 5.

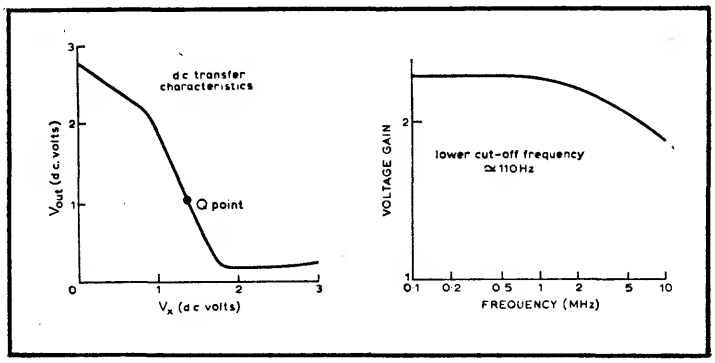
Circuit modifications



Wideband amplifiers with t.t.l., r.t.l., d.t.l.



Circuit data
Supply: 5V, 19mA
IC: 1/4×SN7400
C_1: 10μF tantalum
R_1: 220Ω; R_2: 560Ω
V_{in}: 50mV r.m.s.

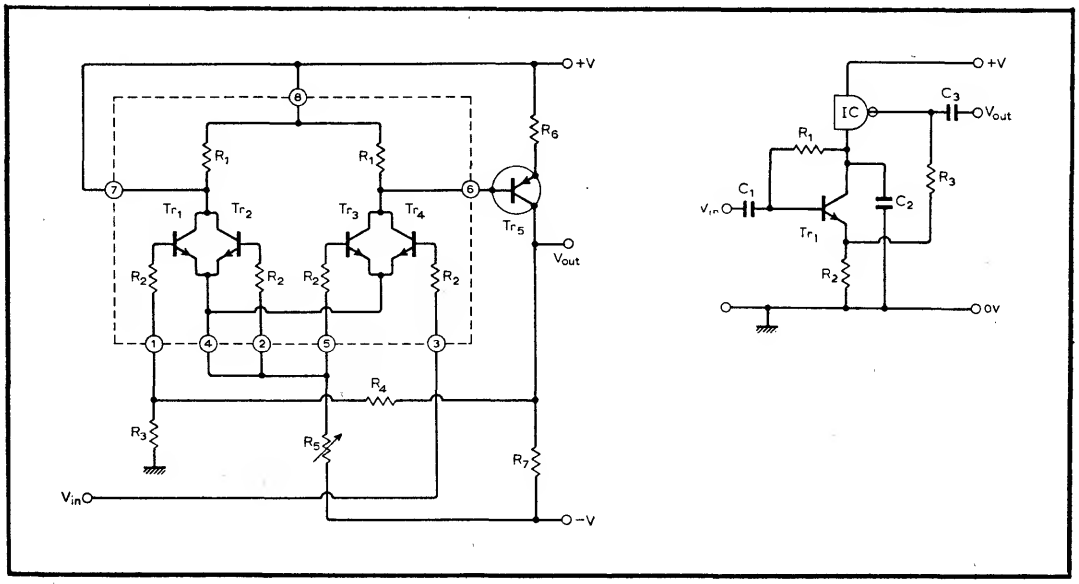


T.t.l. gate description
Without the use of negative feedback, the normal transfer characteristic of the t.t.l. gate is designed to provide well-defined logic levels with a high-gain transition region between them causing the gate to rest in either the on or off condition. Compared with the static on or off state, the supply current drain increases sharply as the gate is switched through the narrow transition region. Although designed for medium-speed digital switching applications a t.t.l. NAND gate can be converted into a linear wideband amplifier. By addition of R_1 and R_2, as shown, the shunt-derived shunt-applied negative feedback has the effect of linearizing the overall d.c. transfer characteristic, eliminating the well-defined logic states, widening the transition region, reducing the gain, and increasing the standing supply current.
Thus, a suitable operating point may be established, with a quiescent supply current of about 19mA, which will allow linear amplification of input signals having levels up to about 800mV pk-pk in the frequency range of approximately 100Hz to 12MHz. Unused gate inputs may be paralleled with the used input rather than being left open-circuit. Alternatively, a logic signal may be applied to the unused input to provide a gating facility on the used input's signal.

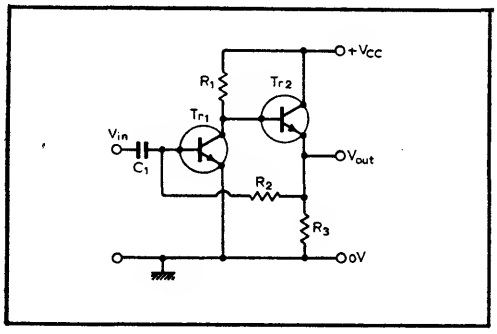
Component changes
Useful range of supply +3 to +5.5V.
Changing R_2 varies gain, shape of the transfer characteristic, and signal-handling capability.
In principle, all four gates in the package may be used simultaneously for linear amplification but the package dissipation is then far in excess of that when used for logic operation.

R.t.l. and d.t.l. gate descriptions.
A dual NAND/NOR r.t.l. gate, contained in a single 914 package (shown dotted), has Tr_1, Tr_2 and Tr_3, Tr_4 connected as a long-tailed pair with R_5 returned to the −V rail and serving as an approximation to a constant-current Source below. Transistor Tr_5 is used as an inverting output stage having a gain of two, with the output at its collector fed back to Tr_1 via R_4 and R_3. Thus, a non-inverted output is available for signals applied to Tr_4 base. The d.c. output voltage can be set to zero with the input grounded, by adjusting R_5. A gain of 10 with bandwidth greater than 10MHz is obtainable with a supply of ±6V, Tr_5 2N3702, R_1 640Ω, R_2 450Ω (internal to 914), R_3, R_5, R_6, 1kΩ, R_4 10kΩ, R_7 2.2kΩ.
● Circuit below right Shows a d.t.l. buffer gate connected in the collector circuit of Tr_1 using the former's +V and extender pins. The gate is operated at its logic switching threshold where it provides high gain. Negative feedback is provided by R_2 and R_3 which determine the overall gain. By decoupling a section of R_2, the gain may be increased without affecting the d.c. operating conditions. A gain of 10, a bandwidth in excess of 500kHz and a load-driving capability of 1 volt into 300Ω is achievable with a supply of +5V, IC ½×932, Tr_1 2N2222, R_1 120kΩ, R_2 120Ω, R_3 1.1kΩ, C_1 10nF, C_2 100pF, and C_3 10μF.

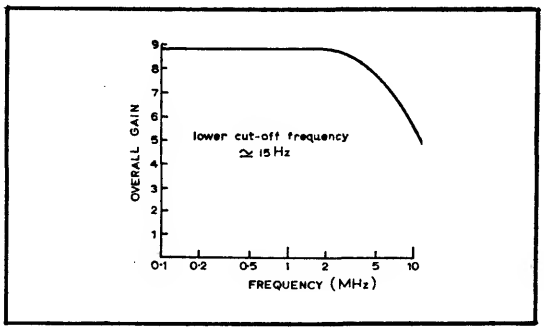
Further reading
Kolataj, J. H. Linearize your t.t.l. gates—then build useful circuits with them, in 400 Ideas for Design, Hayden 1971, pp. 2–3.
Klipstein, D. L. Build an operational amplifier from a dual NAND/NOR gate, in 400 Ideas for Design, Hayden 1971, p. 21.
Jones, D. Wideband amplifier uses a single d.t.l. gate, in 400 Ideas for Design, Hayden 1971, p. 23.



Amplifiers using d.c. feedback pair

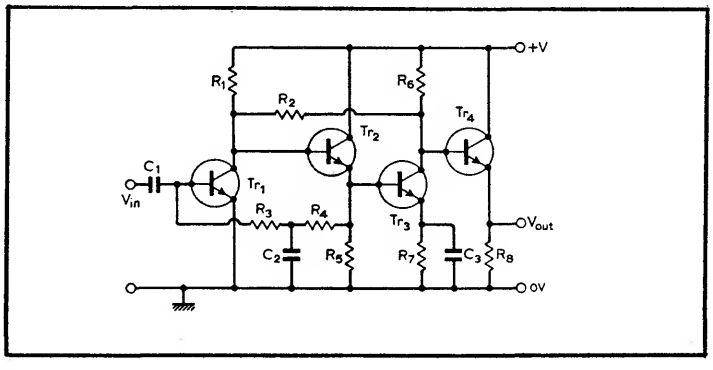


Circuit data
Supply: +5V, 6mA
Tr_1, Tr_2: 1/5 × CA3046
C_1: 10μF tantalum
R_1: 3.9kΩ; R_2: 10kΩ
R_3: 150Ω
V_{C_1}: 1.5V; V_{B_1}: 0.67V
V_{E_2}: 0.77V
Source e.m.f.: 50mV r.m.s.



Circuit description
Transistor Tr_1 is connected in the common-emitter configuration and feeds the emitter follower Tr_2 with overall shunt-derived shunt-applied feedback via R_2, which allows the overall gain and input impedance to be adjusted. If the circuit is supplied from an ideal voltage source the gain will be high and the bandwidth relatively small. Such a source could be heavily loaded when connected directly to the circuit shown above. This is due to the equivalent load on the source of h_{ie} of Tr_1 in parallel with $R_2/(1+|A_v|)$, where $|A_v| \approx g_m R_{L1}$; R_{L1} being the equivalent load resistance seen by Tr_1. The signal generator available had an output resistance of 100Ω which approximately matched the input resistance of the amplifier. This can be seen to be reasonable assuming h_{ie} of Tr_1 to be approximately 2.5kΩ and $|A_v| \approx 80$ with $R_{L1} \approx 3k\Omega$.
To define the overall gain and input impedance and to provide a wider bandwidth a resistor may be included in series with C_1. Response shown applies with a 900-Ω resistance included and the overall gain = V_{out}/source e.m.f. If it is desired to match the amplifier input resistance to a defined source resistance, this can be achieved using the circuit as shown above and adjusting the value of R_2.
The integrated-circuit package used contains a five-transistor array, two connected as a long-tailed pair. One of the single transistors has its emitter connected to the integrated circuit substrate which must be connected to the most negative supply rail, hence this transistor can be conveniently used as Tr_1 and any other as Tr_2. A discrete component version of the circuit is also viable.

Component changes
Useful range of $V_{cc} \approx +3$ to +15V.
Maximum source e.m.f. 72mV r.m.s. with $V_{cc} = +5$V.
R_2 adjustable to provide desired overall gain, bandwidth of input impedance, e.g. with $R_2 = 47k\Omega$ and circuit as shown above: overall gain ≈22 and bandwidth ≈3.4MHz.
Resistance values may be scaled by a given factor, e.g. increasing values by factor of 10: overall gain ≈28 and bandwidth ≈1MHz.

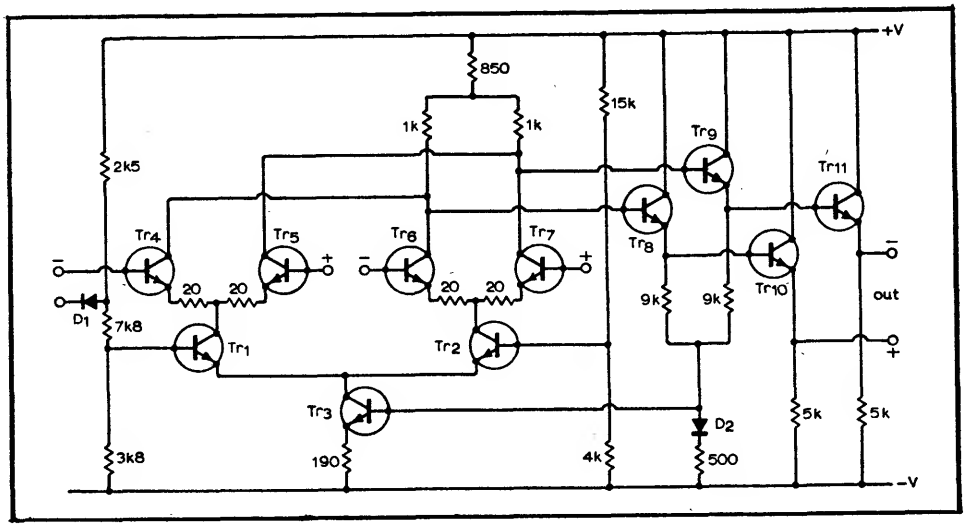


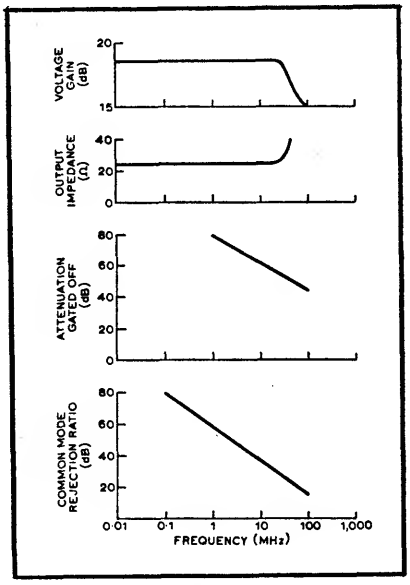
Circuit description
Another amplifier based on the configuration shown top, and also using an integrated-circuit transistor array is shown above. Transistors are contained in a single CA3018 package with Tr_3 emitter and Tr_3 base internally connected. The circuit arrangement of Tr_1, Tr_2 serving as a common-emitter common-collector pair followed by Tr_3, Tr_4 in the same configuration is designed to reduce internal capacitive feedback. The Tr_2-emitter follower acts as a low output impedance source to drive the Tr_3 common-emitter stage and also provides a low-capacitance high-impedance loading on the Tr_1 common-emitter stage.
All stages are d.c. coupled with two negative feedback paths. Feedback from Tr_2 emitter to Tr_1 base is effective at d.c. and low frequencies while that from Tr_3 collector to Tr_1 collector functions at all frequencies. Feedback provides stability of d.c. operating conditions and allows a gain-bandwidth tradeoff to be made. When supplied from a 50-Ω source, a voltage gain of 49dB with a bandwidth of approximately 32MHz is obtainable with a supply of +6V, C_1, C_2 1μF, C_3 470nF, R_1 3.5kΩ, R_2 8.2kΩ, R_3 22kΩ, R_4 18kΩ, R_5 1.8kΩ, R_6 2.5kΩ, R_7 1kΩ, R_8 2.7kΩ, using input signals in the range 7μV to 4mV (r.m.s.). Lower cut-off frequency largely depends on the capacitors used and is about 800Hz with the above values.

Further reading
RCA Application note ICAN 5296, in Databook SSD-202, 1972, pp. 68/9.
Cherry, E. M. and Hooper, D. E. Design of wide-band transistor feedback amplifiers, *Proc.I.E.E.*, vol. 110, 1963, pp. 375–87.
Tuil, J. Transistor-equipped aerial amplifiers—wideband amplifiers, *Electronic Applications*, vol. 28, 1968, pp. 75–8.

Cross references
Set 12, cards 2, 8 & 12.
Set 7, card 9.
Set 4, card 4.

Gated video amplifier





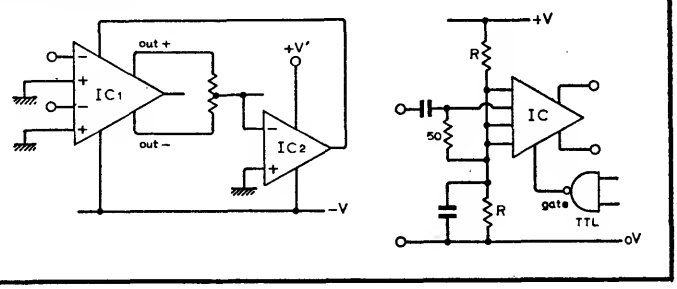
Circuit data
Supply: ±5V, 8mA
IC: MC1445L
Voltage gain: 19dB
Bandwidth: 60MHz
Output attenuation: 60dB with input gated off
Input impedance: ≈8kΩ
Output impedance: ≈22Ω
Input common-mode range: ±2.5V
Quiescent output voltage: ≈0.18V
Gate voltage range: 0.35 to 2.0V

Circuit description
The long-tailed pair is the key to the operation of this circuit, as of so many linear i.cs. The V_{be}/I_C characteristic of a bipolar transistor is given by $I_C = I_S \exp(qV_{be}/kT)$. Transconductance is obtained by differentiating I_C with respect to V_{be}, and is found to be proportional to I_C. Thus controlling I_C gives proportional control of the voltage gain of an amplifier provided that the collector load is low enough to allow the full transconductance to be developed. Used with a single transistor an output signal may be gated on and off by such a means, but the shift in d.c. level carries the gate signal through into the output circuit. With long-tailed pairs as shown, Tr_3 sustains a constant total current using common-mode feedback via the emitters of Tr_8, Tr_9. If Tr_3 conduction increases the collector potentials of Tr_4, Tr_6 must fall regardless of which the current is channelled through. This fall in potential at each collector is coupled via the emitter followers Tr_8, Tr_9 to close the d.c. feedback loop and stabilize operating conditions. The base of Tr_2 is fixed while that of Tr_1 is normally more positive, ensuring that Tr_4, Tr_5 are the conducting transistors, i.e. having sufficient g_m to give an overall voltage gain of 18 to 20dB. Transistor Tr_2 has negligible current and Tr_6, Tr_7 contribute nothing to the output. If the potential at the base of Tr_1 is lowered, either by placing a low direct voltage at the gate input (D_1), or by taking the input to the negative supply rail through a resistor, then the currents in Tr_6, Tr_7 increase at the expense of Tr_4, Tr_5. Hence the signals applied to these differential inputs are gated by a d.c. input. This input may be changed rapidly to allow gating for very short durations or may have intermediate values that allow the inputs to be summed in varying proportions.

Component changes
IC: MC1445, 1545; similar i.cs with different bias arrangements include Silicon General SG1402/2402/3402. "Discrete" versions based on transistor arrays are also possible but no particular advantages would be expected except possibility of operating at unusual supply voltage/current levels. Balanced modulators/demodulators (MC1496) have similar input stages with free collectors suitable for coupling into tuned circuits.
If the frequency range is more limited, it is possible to adapt analogue multipliers with one input switched between zero and some finite value. This also allows reversal of phase of the output if the control input polarity is reversed.
V_S: ±3.5 to ±12V.
R_L: At low supply voltages the output quiescent current may be increased by placing external resistors in parallel with the 5.0kΩ internal resistors. This increases the signal current that may be capacitively coupled into a load, while lowering the output impedance. 10k to 1kΩ at ±5V supply. Observe maximum dissipation limits of device (dependent on package, ambient temperature, but up to 400mW at <50°C).

Circuit modifications
● By applying the mean value of the output to a standard op-amp, the output can be made to provide a sensitive error signal for departures of the mean i.c. output potential from ground. If the op-amp is operated from a higher positive voltage than that required by the wide-band i.c., then d.c. feedback ensures that the positive voltage applied to the i.c. forces the mean output close to zero (depending on the op-amp offset of a few millivolts). This allows d.c. coupling of signal from input to output of wide-band amplifier with negligible offset.
● For single-ended supplies the unused inputs are taken to a decoupled potential divider, with the option of a 50Ω resistance added to define the input impedance of any signal input, e.g. capacitively coupled as shown. The gate terminal then becomes compatible with a t.t.l., c.m.o.s. logic gate sharing a common ground line.

Circuit modifications



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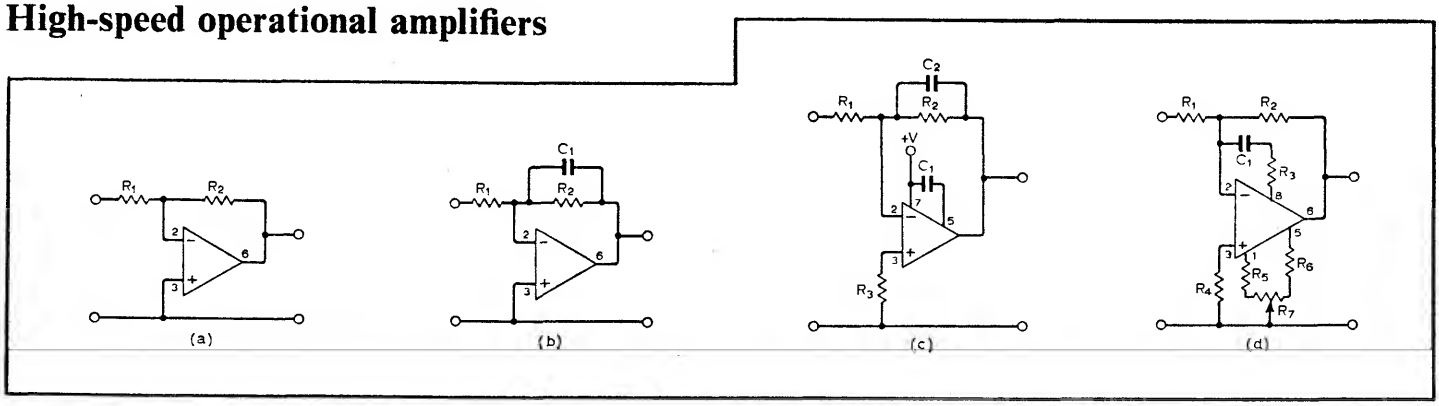
High-speed operational amplifiers



R_1, R_2: 10kΩ
Slew rate: 80V/μs
Small-signal bandwidth 14MHz

R_1: 5kΩ, R_2: 10kΩ
C_1: 5pF
Voltage gain: −2
Comparable figures to (a)

R_1, R_2: 10kΩ, R_3: 5kΩ
C_1: 0.1μF, C_2: 5pF
Shortens settling time to 1μs for 0.1% accuracy after 10V step

R_1, R_2: 4.7kΩ
R_3: 3.3kΩ, R_4: 1kΩ
R_5, R_6: 27kΩ, R_7: 2.5kΩ
Slew rate: 150V/μs

Circuit description

The bandwidth available from operational amplifiers has been extended by many manufacturers to the level where they can be applied to problems previously requiring specially-designed wideband amplifiers. The circuits (a)–(d) use a monolithic i.c. the LM318, showing how manufacturers are able to provide compensation points to modify the high-frequency characteristics—trading in stability margins for increased slew rates, minimum settling times, etc. The internal structure of any particular i.c. at this level of performance is immensely complex and most users will have to treat them as black boxes.

Using hybrid techniques as well as discrete circuitry, amplifiers are available with slew rates in excess of 1000V/μs and bandwidths greater than 100MHz. Methods of construction are more costly than monolithic circuits and they are relevant to specialized applications. In general to achieve such very high bandwidths, the open-loop voltage gain has to be restricted to the range 1 to 5000, while the monolithic amplifier above is optimized for best bandwidth consistent with voltage gains >100,000.

Further circuits

● As a standard operational amplifier, circuits commonly used with 741, 301 and similar devices may be adapted to high frequency units such as the LM318. Layout and decoupling are important, but high frequency amplifiers, oscillators, filters and the like follow similar configurations, generally with comparable resistance values and reduced capacitances. To combine the wide frequency range with high input resistance the technique shown may be adopted. At very low frequencies the high input impedance amplifier—LM312 or similar—develops its full gain applying its inverted output to the non-inverting input of the high-frequency amplifier. The overall characteristic is inverting and the feedback is negative, while the minimal input current of the high-impedance unit permits R_1 and R_2 to have megohm values. At high-frequencies the integrator configuration of the LM312 leaves the non-inverting input of the LM318 virtually grounded. The signal appears on the inverting input via the CR network and the feedback remains negative. The two time constants define the cross-over regions the overall gain being sustained to 1MHz.

● Non-linear circuits may be extended to higher frequencies, and for example precision half- and full-wave rectifiers operate to an order of magnitude higher in frequency than with 741, etc. At these higher frequencies, Schottky diodes with their smaller forward voltage drop and absence of charge storage are worthwhile alternatives to even high-speed conventional diodes.

● Component values for the voltage follower mode are similar to those for the unity-gain inverter. Not all amplifiers are compensated for 100% feedback, but may be optimized for higher gains instead.

Further reading

LM318 data sheet, National Semiconductor Linear Integrated Circuits Databook, 1972, pp. 185–9.

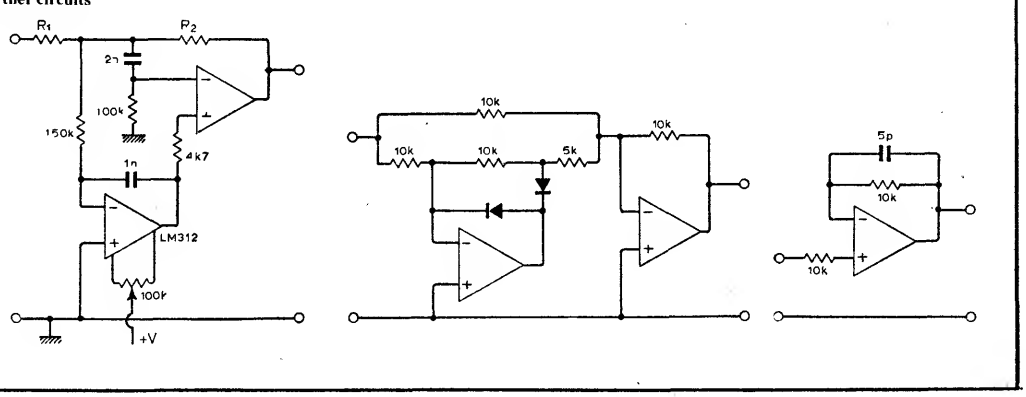
Young, R. L. Lift i.c. op-amp performance, *Electronic Design*, vol. 4, no. 21, 15 Feb, 1973, pp. 66–9.

Motorola application note—AN276, 14MHz wideband amplifier using the MC1530 op-amp.

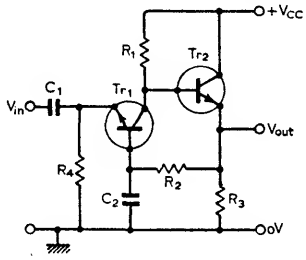
Cross references

Set 12, cards 3 & 4.

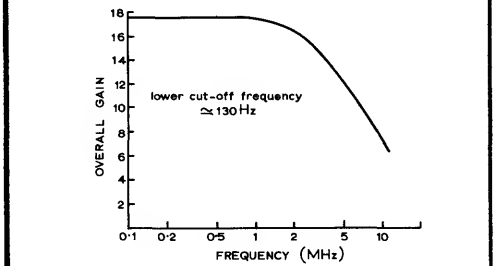
Further circuits



Common-base wideband amplifier



Circuit data
Supply: +5V, 8mA
Tr_1, Tr_2: 1/5×CA3046
C_1, C_2: 10μF tantalum
R_1: 3.9kΩ; R_2: 10kΩ
R_3: 150Ω; R_4: 470Ω
Source e.m.f.:
30mV r.m.s.
Source res.: 100Ω



Circuit description
The input stage consists of Tr_1 in the common-base configuration with this transistor feeding Tr_2 acting as an emitter follower with overall shunt-derived shunt-applied feedback through R_2. This arrangement is similar to the circuit shown on card 9, except that the source feeds the emitter instead of the base of Tr_1, indicating that the d.c. feedback pair is a convenient method of biasing a common-base stage.
Capacitor C_1 prevents any d.c. component present in the input signal from affecting the biasing, or it may be thought of as necessary if the source cannot sink current from Tr_1. cannot sink current from Tr_1 emitter. Capacitor C_2 grounds the base of Tr_1 to a.c. signals.
The input impedence of the circuit is low and may be adjusted or matched to a source, by means of R_1 which controls the collector current and hence the emitter current of Tr_1. This type of circuit is useful for applications where the common-base configuration offers advantages such as small non-linearity of its transfer characteristic and relatively constant gain with frequency, while providing moderate gain due to the impedance transformation between input and output.
The integrated circuit used is the same as that for card 9 where one transistor has its emitter connected to the substrate which must be connected to the most negative supply rail (0V in this case). Because neither Tr_1 nor Tr_2 has its emitter grounded in the above circuit the substrate-connected transistor cannot be used but its emitter must still be grounded.

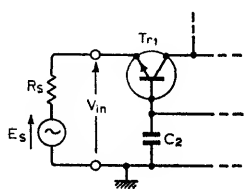
Component changes
Useful range of V_{cc}: +3 to +15V.
Maximum source e.m.f. ≈37mV r.m.s. (with V_{cc}=+5V).
With other resistors in the same ratios R_1 may be:
(a) raised as high as 100kΩ if low quiescent power is a major factor and maximum bandwidth less important.
(b) chosen to provide maximum gain-bandwidth product in Tr_1.
(c) reduced to about 100Ω if maximum output current is required.
R_3 may be reduced towards R_1/h_{FE} and R_2 increased towards $h_{FE}.R_1$.

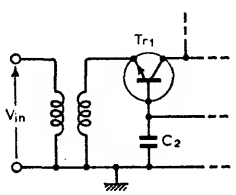
Circuit modifications
● If the signal source can sink direct emitter current of Tr_1, C_1 and R_4 may be omitted and the source connected directly to Tr_1 emitter as shown left, the rest of the circuit remaining the same.
● Where d.c. isolation of the source and Tr_1 emitter is required, an alternative input arrangement to the original circuit using a transformer may be adopted as shown centre, again the remaining circuitry being unchanged. This input transformer may be used to match the source to the input impedance of Tr_1 if desired.
● If it is required to use a common-base stage that provides an output current which is as nearly identical to the input current as possible, a compound transistor may be used as shown right. The base current of Tr_1 is a very good measure of the extent by which its collector current falls short of its emitter current. By feeding back the base current of Tr_1 to the common-base transistor Tr_3 and adding its collector current to the input current, the output current more nearly approaches I_{in}. This technique also raises the output impedance from Z_{out_1} to approximately $Z_{out_1}.h_{fb_1}/(1-h_{fb_3})$ and reduces the distortion from D_1% to approximately $D_1(1-h_{fb_3})$ % compared with Tr_1 alone.

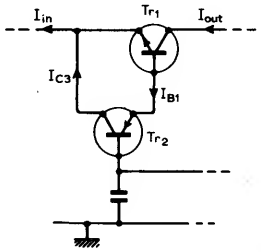
Further reading
Miller, J. R., Solid-State Communications, McGraw-Hill, 1966, chapter 15.
Boxall, F. S. Base current feedback and feedback compound transistor, *Semiconductor Products*, vol. 1, no. 5, 1958, pp. 17–24.

Cross references
Set 12, cards 2, 5 & 9.
Set 7, card 9.

Circuit modifications







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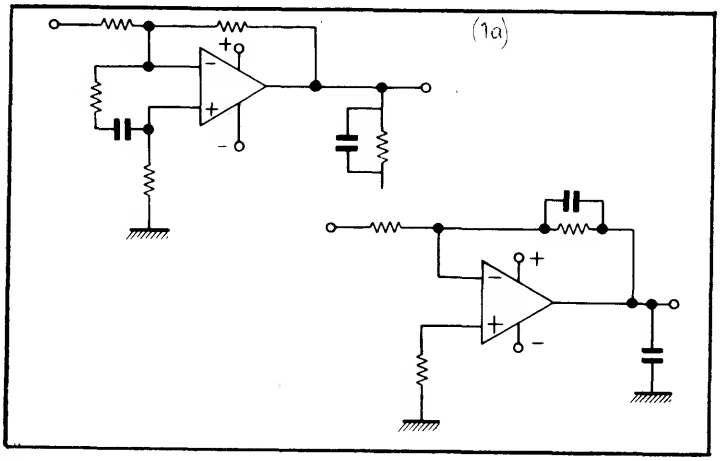
Set 12: Wideband amplifiers Up-date

1. Both input and output compensation of an operational-amplifier (with 100mA capability) to provide high slew-rates are considered. Fig. 1 (a) shows input compensation, where $R_C = 47\Omega$ and $C_C = 0.01\mu F$, for unity gain. Table 1 indicates variations required to these components at higher gains. For gains greater than 5, a single capacitor across the output is adequate for stability with a sacrifice in bandwidth Fig. 1(b). The slew-rates possible are quoted in the lower part of the table and little change occurs for capacitive loads up to 50nF.

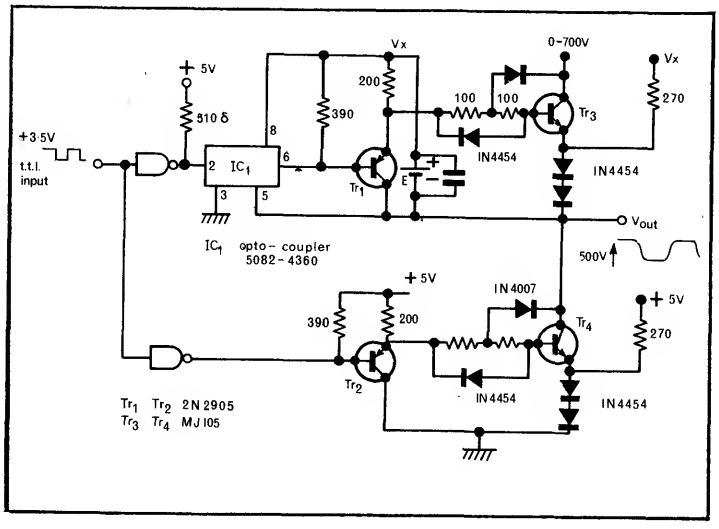


Gain	C_C nF	R_C Ω	Slew rate V/μs	Bandwidth kHz
1	10	47	50	600
10	4.7	100	30	600
100	—		100	600
5	200	—	0.75	12
10	100	—	1.5	24
50	20	—	7.5	120
100	10	—	15	240

Reference

Wyland, J. Ideas for Design, *Electronic Design* 10, May 10, 1975.

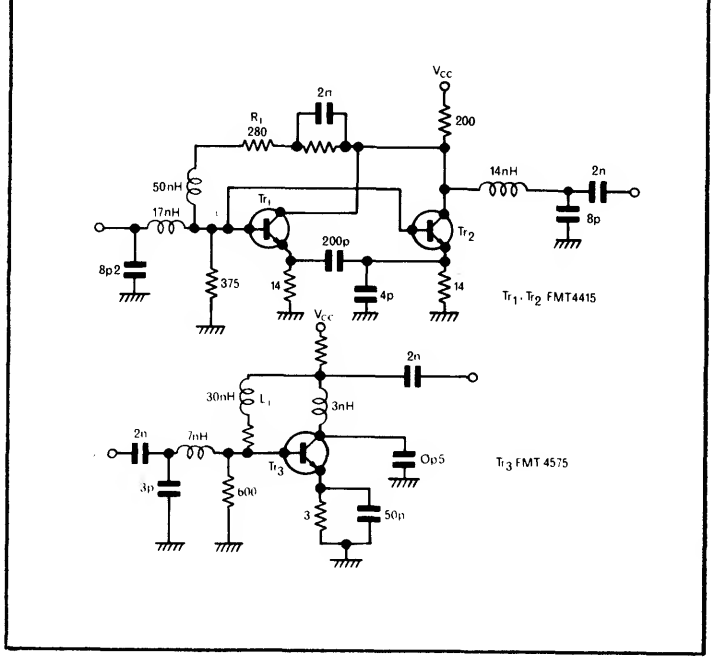
2. This circuit provides a pulse amplifier with a high voltage capability. The circuit is driven from t.t.l. levels, and can operate at frequencies up to 100kHz. High-voltage transistors Tr_3 and Tr_4 are alternately switched on and off via transistors Tr_1 and Tr_2. The bias supply for transistors Tr_1 and Tr_3 is obtained from a 4.5V battery and an optical coupler allows Tr_1 to be switched by the t.t.l. gate. No isolation is required for the lower transistor network which can be driven by t.t.l. directly. When the input is high, Tr_2 is hard on, removing the bias from Tr_4 which is convincingly off because its base-emitter junction will be reverse-biased by about −1.5V. Tr_3 will be biased on giving a high output voltage depending on power supply level.



Reference

Limuti, D. Ideas for Design, *Electronic Design* 20, Sept. 27, 1975.

3. Figs. 3 (a) and 3 (b) are circuits for wideband amplifiers using computer aided design techniques. The first provides an 11dB gain over the range 100–500MHz, and the last provides 14dB gain over the range 100MHz to 1GHz. When two transistors are placed in parallel for medium power (10 to 100mW), equal emitter resistors are included for d.c. balance, and also provide series feedback for the stage. The emitter capacitor C_E provides a gain compensation. Resistor R_1 is the shunt feedback resistor, with an inductor in series to reduce the feedback at the high frequency end of the response, and thus maintain flat gain. The reactive elements being selected at input and output for matching purposes. The single transistor amplifier is designed for discrete components, but for microstrip and thin-film hybrid amplifiers, it is suggested that a transmission line approach is better, for the necessary inductance values. It is suggested that the design in Fig. 3 (b) can be packaged in a standard TO-8 can.



Reference

Steivin, P. Use c.a.d. to optimize broadband amp design, *Electronic Design* 10, May 10, 1974.