CHAPTER 2

Specialty Amplifiers

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CHAPTER 2

Specialty Amplifiers

Walt Kester, Walt Jung, James Bryant

This chapter of the book discusses several popular types of *specialty* amplifiers, or amplifiers that are based in some way on op amp techniques. However, in an overall applications sense, they are not generally used as universally as op amps. Examples of specialty amplifiers include instrumentation amplifiers of various configurations, programmable gain amplifiers (PGAs), isolation amplifiers, and difference amplifiers.

Other types of amplifiers, for example such types as audio and video amplifiers, cable drivers, high-speed variable gain amplifiers (VGAs), and various communications-related amplifiers might also be viewed as specialty amplifiers. However, these applications are more suitably covered in Chapter 6, within the various signal amplification sections.

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SECTION 2-1

Instrumentation Amplifiers

Walt Kester, Walt Jung

Probably the most popular among all of the specialty amplifiers is the *instrumentation amplifier* (hereafter called simply an *in amp*). The in amp is widely used in many industrial and measurement applications where dc precision and gain accuracy must be maintained within a noisy environment, and where large common-mode signals (usually at the ac power line frequency) are present.

Op Amp/In Amp Functionality Differences

An in amp is unlike an op amp in a number of very important ways. As already discussed, an op amp is a general-purpose gain block—user-configurable in myriad ways using external feedback components of R, C, and, (sometimes) L. The final configuration and circuit function using an op amp is truly whatever the user makes of it.

In contrast to this, an in amp is a more constrained device in terms of functioning, and also the allowable range(s) of operating gain. In many ways, it is better suited to its task than would be an op amp—even though, ironically, an in amp may actually comprise of a number of op amps within it. People also often confuse in amps as to their function, calling them "op amps." But the reverse is seldom (if ever) true. It should be understood that an in amp is *not* just a special type op amp; the function of the two devices is fundamentally different.

Perhaps a good way to differentiate the two devices is to remember that an op amp can be programmed to do almost anything, by virtue of its feedback flexibility. In contrast to this, an in amp *cannot* be programmed to do just anything. It can *only* be programmed for gain, and then over a specific range. An op amp is configured via a number of external components, while an in amp is configured either by one resistor, or by pin-selectable taps for its working gain.

In Amp Definitions

An in amp is a *precision* closed-loop gain block. It has a pair of differential input terminals, and a single-ended output that works with respect to a reference or common terminal, as shown in Figure 2-1. The input impedances are balanced and high in value, typically $\geq 10^9\,\Omega$. Again, unlike an op amp, an in amp uses an

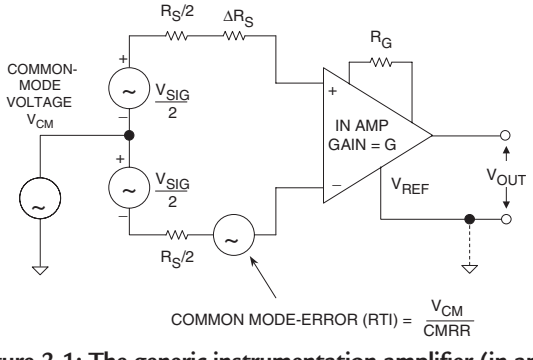


Figure 2-1: The generic instrumentation amplifier (in amp)

internal feedback resistor network, plus one (usually) gain set resistance, R_G. Also unlike an op amp is the fact that the internal resistance network and R_G are *isolated* from the signal input terminals. In amp gain can also be preset via an internal R_G by pin selection, (again isolated from the signal inputs). Typical in amp gains range from 1 to 1,000.

The in amp develops an output voltage that is referenced to a pin usually designated REFERENCE, or V_{REF}. In many applications, this pin is connected to circuit ground, but it can be connected to other voltages, as long as they lie within a rated compliance range. This feature is especially useful in single-supply applications, where the output voltage is usually referenced to mid-supply (i.e., 2.5 V in the case of a +5 V supply).

In order to be effective, an in amp needs to be able to amplify microvolt-level signals, while simultaneously rejecting volts of *common-mode* (CM) signal at its inputs. This requires that in amps have very high *common-mode rejection* (CMR). Typical values of in amp CMR are from 70 dB to over 100 dB, with CMR usually improving at higher gains.

It is important to note that a CMR specification for dc inputs alone isn't sufficient in most practical applications. In industrial applications, the most common cause of external interference is 50 Hz/60 Hz ac power-related noise (including harmonics). In differential measurements, this type of interference tends to be induced equally onto both in amp inputs, so the interference appears as a CM input signal. Therefore, specifying CMR over frequency is just as important as specifying its dc value. Note that imbalance in the two source impedances can degrade the CMR of some in amps. Analog Devices fully specifies in amp CMR at 50 Hz/60 Hz, with a source impedance imbalance of 1 kΩ.

Subtractor or Difference Amplifiers

A simple subtractor or difference amplifier can be constructed with four resistors and an op amp, as shown in Figure 2-2. It should be noted that this is *not* a true in amp (based on the previously discussed criteria), but it is often used in applications where a simple differential-to-single-ended conversion is required. Because of its popularity, this circuit will be examined in more detail, in order to understand its fundamental limitations before discussing true in amp architectures.

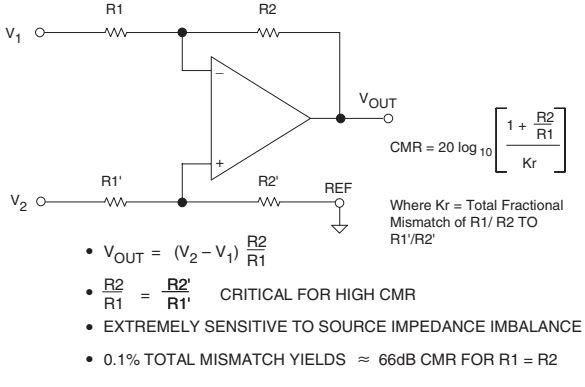


Figure 2-2: Op amp subtractor or difference amplifier

There are several fundamental problems with this simple circuit. First, the input impedance seen by V_1 and V_2 isn't balanced. The input impedance seen by V_1 is R1, but the input impedance seen by V_2 is R1' + R2'. The configuration can also be quite problematic in terms of CMR, since even a small source impedance imbalance will degrade the workable CMR. This problem can be solved with well-matched open-loop

buffers in series with each input (for example, using a precision dual op amp). But, this adds complexity to a simple circuit, and may introduce offset drift and nonlinearity.

The second problem with this circuit is that the *CMR is primarily determined by the resistor ratio matching,* not *the op amp*. The resistor ratios R1/R2 and R1'/R2' must match extremely well to reject common mode noise—at least as well as a typical op amp CMR of ≥100 dB. Note also that the *absolute* resistor values are relatively unimportant.

Picking four 1% resistors from a single batch may yield a net ratio matching of 0.1%, which will achieve a CMR of 66 dB (assuming R1 = R2). But if one resistor differs from the rest by 1%, the CMR will drop to only 46 dB. Clearly, very limited performance is possible using ordinary discrete resistors in this circuit (without resorting to hand matching). This is because the best standard off-the-shelf RNC/RNR style resistor tolerances are on the order of 0.1% (see Reference 1).

In general, the worst-case CMR for a circuit of this type is given by the following equation (see References 2 and 3):

$$\mathrm{CMR}\left(\mathrm{dB}\right) = 20\log\left[\frac{1+\mathrm{R2}/\mathrm{R1}}{4\mathrm{Kr}}\right], \qquad \text{Eq. 2-1}$$

where *Kr* is the *individual* resistor tolerance in fractional form, for the case where four discrete resistors are used. This equation shows that the worst-case CMR for a tolerance build-up for four unselected same-nominal-value 1% resistors to be no better than 34 dB.

A single resistor network with a net matching tolerance of Kr would probably be used for this circuit, in which case the expression would be as noted in the figure, or:

$$\mathrm{CMR}\left(\mathrm{dB}\right) = 20\log\left[\frac{1+\mathrm{R2}/\mathrm{R1}}{\mathrm{Kr}}\right] \qquad \text{Eq. 2-2}$$

A net matching tolerance of 0.1% in the resistor ratios therefore yields a worst-case dc CMR of 66 dB using Eq. 2-2, and assuming R1 = R2. Note that either case assumes a significantly higher amplifier CMR (i.e., >100 dB). Clearly for high CMR, such circuits need four single-substrate resistors, with very high absolute and TC matching. Such networks using thick/thin-film technology are available from companies such as Caddock and Vishay, in ratio matches of 0.01% or better.

In implementing the simple difference amplifier, rather than incurring the higher costs and PCB real estate limitations of a precision op amp plus a separate resistor network, it is usually better to seek out a completely monolithic solution. The AMP03 is just such a precision difference amplifier, which includes an on-chip laser trimmed precision thin film resistor network. It is shown in Figure 2-3. The typical CMR of the AMP03F is 100 dB, and the small-signal bandwidth is 3 MHz.

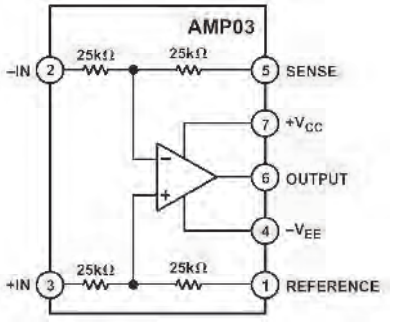


Figure 2-3: AMP03 precision difference amplifier

There are several devices related to the AMP03 in function. These are namely the SSM2141 and SSM2143 difference amplifiers. These sister parts are designed for audio line receivers (see Figure 2-4). They have low distortion, and high (pretrimmed) CMR. The net gains of the SSM2141 and SSM2143 are unity and 0.5, respectively. They are designed to be used with balanced 600 Ω audio sources (see the related discussions on these devices in the Audio Amplifiers section of Chapter 6).

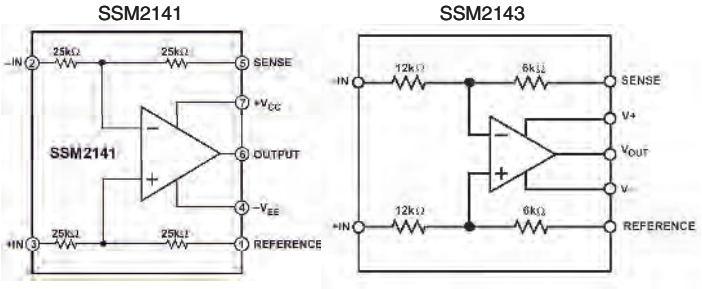
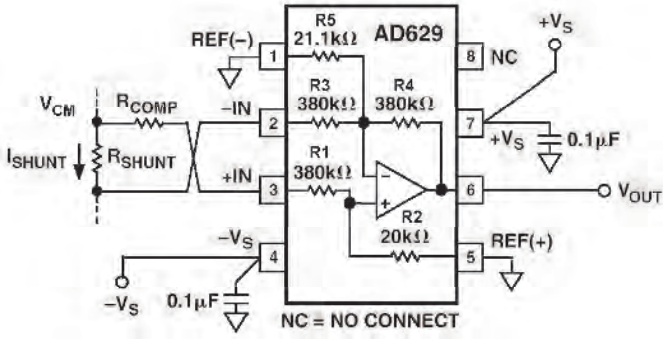


Figure 2-4: SSM2141 and SSM2143 difference amplifiers (audio line receivers)

Another interesting variation on the simple difference amplifier is found in the AD629 difference amplifier, optimized for high common-mode input voltages. A typical current-sensing application is shown in Figure 2-5. The AD629 is a differential-to-single-ended amplifier with a gain of unity. It can handle a common-mode voltage of ±270 V with supply voltages of ±15 V, with a small signal bandwidth of 500 kHz.



V_{CM} = ±270V for V_S = ±15V

Figure 2-5: High common-mode current sensing using the AD629 difference amplifier

The high common-mode voltage range is obtained by attenuating the noninverting input (Pin 3) by a factor of 20 times, using the R1–R2 divider network. On the inverting input, resistor R5 is chosen such that R5‖R3 equals resistor R2. The noise gain of the circuit is equal to 20 [1 + R4/(R3‖R5)], thereby providing unity gain for differential input voltages. Laser wafer trimming of the R1–R5 thin film resistors yields a minimum CMR of 86 dB @ 500 Hz for the AD629B. Within an application, it is good practice to maintain

balanced source impedances on both inputs, so dummy resistor R_{COMP} is chosen to equal to the value of the shunt sensing resistor R_{SHUNT}.

David Birt (see Reference 4) of the BBC has analyzed the simple line receiver topology in terms of loading presented to the source, and presented a modified and balanced form, shown as Figure 2-6. Here stage U1 uses a 4 resistor network identical to that of Figure 2-2, while feedback from the added unity gain inverter U2 drives the previously grounded R2' reference terminal. This has two overall effects; the input currents in the ± input legs become equal in magnitude, and the gain of the stage is halved.

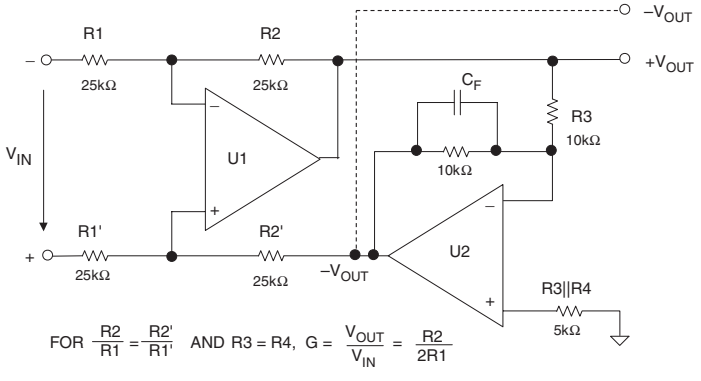


Figure 2-6: Balanced difference amplifier using push-pull feedback path

Compared to Figure 2-2, and for like resistor ratios, the Figure 2-6 gain from V_{IN} to V_{OUT} is one-half, or a gain of –6 dB (0.5) as shown. However the new circuit form also offers a complementary output from U2, $–V_{OUT}$.

The common-mode range of this circuit is the same as for Figure 2-2, but the CMR is about doubled with all resistors nominally equal (as measured to a single output). The inverter resistor ratio R3/R4 affects output balance, but not CMR. Like Figure 2-2, the gain of this circuit is not easily changed, as it involves precise resistor ratios.

Because of the two feedback paths, this circuit holds the inputs of U1 at a null for differential input signals. However CM signals are seen by U1, and the CM range of the circuit is $[1 + (R2'/R1')] \times V_{CM(U1)}$. Differential input resistance is R1 + R1'.

As can be noted from Figure 2-6, this circuit can be broken into a simple line receiver (left), plus an inverter (right). Thus existing line receivers like Figure 2-2 can be converted to the fully balanced topology, by simply adding an appropriate inverter, U2. This of course not only balances the *input* currents, but it also provides a balanced *output* signal.

For example, the SSM2141 line receiver and the OP275 are a good combination for implementing this approach. (See Reference 5, and the further discussions on these circuits in the Audio Amplifiers section of Chapter 6.)

In Amp Configurations

The simple difference amplifier circuits described above are quite useful (especially at higher frequencies) but lack the performance required for most precision applications. In many cases, true in amps are more suitable, because of their balanced and high input impedance, as well as their high common-mode rejection.

Two-Op-Amp In Amps

As noted initially, in amps are based on op amps, and there are two basic configurations that are extremely popular. The first is based on two op amps, and the second on three op amps. The circuit shown in Figure 2-7 is referred to as the *two-op-amp in amp*. Dual IC op amps are used in most cases for good matching, such as the OP297 or the OP284. The resistors are usually a thin film laser trimmed array on the same chip. The in amp gain can be easily set with an external resistor, R_G. Without R_G, the gain is simply 1 + R2/R1. In a practical application, the R2/R1 ratio is chosen for the desired minimum in amp gain.

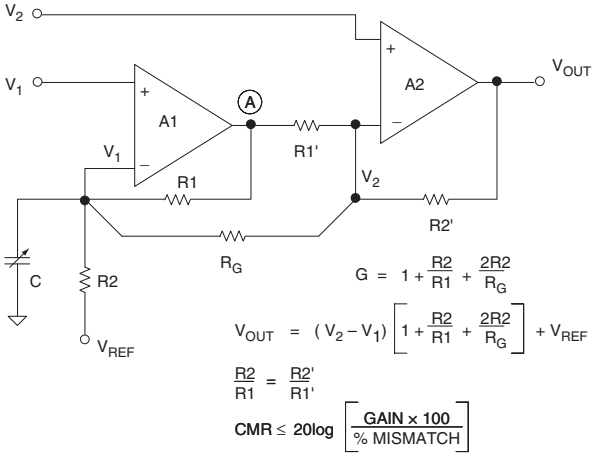


Figure 2-7: The two-op-amp instrumentation amplifier

The input impedance of the two-op-amp in amp is inherently high, permitting the impedance of the signal sources to be high and unbalanced. The dc common mode rejection is limited by the matching of R1/R2 to R1'/R2'. If there is a mismatch in any of the four resistors, the dc common mode rejection is limited to:

$$\mathrm{CMR} \le 20\log\left[\frac{\mathrm{GAIN}\times 100}{\%\mathrm{MISMATCH}}\right]. \qquad \text{Eq. 2-3}$$

Notice that the net CMR of the circuit increases proportionally with the working gain of the in amp, an effective aid to high performance at higher gains.

IC in amps are particularly well suited to meeting the combined needs of ratio matching and temperature tracking of the gain-setting resistors. While thin film resistors fabricated on silicon have an initial tolerance of up to ±20%, laser trimming during production allows the ratio error between the resistors to be reduced to 0.01% (100 ppm). Furthermore, the tracking between the temperature coefficients of the thin film resistors is inherently low and is typically less than 3 ppm/ºC (0.0003%/ºC).

When dual supplies are used, V_{REF} is normally connected directly to ground. In single supply applications, V_{REF} is usually connected to a low impedance voltage source equal to one-half the supply voltage. The gain from V_{REF} to node "A" is R1/R2, and the gain from node "A" to the output is R2'/R1'. This makes the gain from V_{REF} to the output equal to unity, assuming perfect ratio matching. Note that it is critical that the source impedance seen by V_{REF} be low, otherwise CMR will be degraded.

One major disadvantage of the two-op-amp in amp design is that common mode voltage input range must be traded off against gain. The amplifier A1 must amplify the signal at V_1 by 1 + R1/R2. If R1 >> R2 (a low gain example in Figure 2-7), A1 will saturate if the V_1 common-mode signal is too high, leaving no A1 headroom to amplify the wanted differential signal. For high gains (R1<< R2), there is correspondingly more headroom at node "A," allowing larger common-mode input voltages.

The ac common-mode rejection of this configuration is generally poor because the signal path from V_1 to V_{OUT} has the additional phase shift of A1. In addition, the two amplifiers are operating at different closed-loop gains (and thus at different bandwidths). The use of a small trim capacitor "C" as shown in Figure 2-7 can improve the ac CMR somewhat.

A low gain (G = 2) single-supply two-op-amp in amp configuration results when R_G is not used, and is shown in Figure 2-8. The input common mode and differential signals must be limited to values that prevent saturation of either A1 or A2. In the example, the op amps remain linear to within 0.1 V of the supply rails, and their upper and lower output limits are designated V_{OH} and V_{OL}, respectively. These saturation voltage limits would be typical for a single-supply, rail-rail output op amp (such as the AD822, for example).

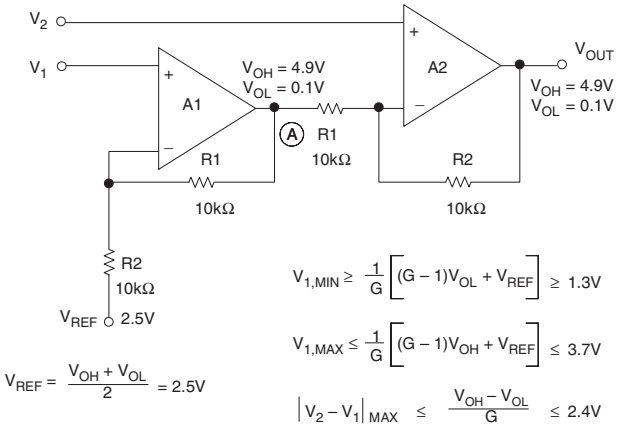


Figure 2-8: Two-op-amp in amp single-supply restrictions for V_s = +5 V, G = 2

Using the Figure 2-8 equations, the voltage at V_1 must fall between 1.3 V and 2.4 V to prevent A1 from saturating. Notice that V_{REF} is connected to the average of V_{OH} and V_{OL} (2.5 V). This allows for bipolar differential input signals with VOUT referenced to 2.5 V. A high gain (G = 100) single-supply two-op-amp in amp configuration is shown in Figure 2-9. Using the same equations, note that voltage at V_1 can now swing between 0.124 V and 4.876 V. V_{REF} is again 2.5 V, to allow for bipolar input and output signals.

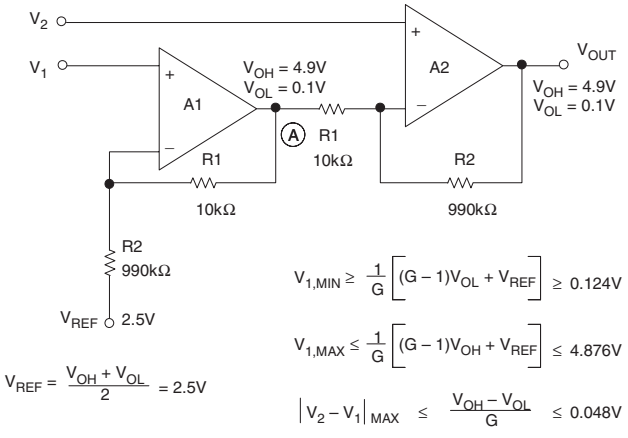


Figure 2-9: Two-op-amp in amp single-supply restrictions for V_s = +5 V, G = 100

All of these discussions show that the conventional two-op-amp in amp architecture is fundamentally limited, when operating from a single power supply. These limitations can be viewed in one sense as a restraint on the allowable input CM range for a given gain. Or, alternately, it can be viewed as limitation on the allowable gain range, for a given CM input voltage.

Nevertheless, there are ample cases where a combination of gain and CM voltage cannot be supported by the basic two-op-amp structures of Figures 2-7 through 2-9, even with perfect amplifiers (i.e., zero output saturation voltage to both rails).

In summary, regardless of gain, the basic structure of the common two-op-amp in amp does not allow for CM input voltages of zero when operated on a single supply. The only route to removing these restrictions for single supply operation is to modify the in amp architecture.

The AD627 Single-Supply Two-Op-Amp In Amp

The above-mentioned CM limitations can be overcome with some key modifications to the basic two-op-amp in amp architecture. These modifications are implemented in the circuit shown in Figure 2-10, which represents the AD627 in amp architecture.

In this circuit, each of the two op amps is composed of a PNP common emitter input stage and a gain stage, designated Q1/A1, and Q2/A2, respectively. The PNP transistors not only provide gain but also level-shift the input signal positive by about 0.5 V, thereby allowing the common-mode input voltage to go to 0.1 V below the negative supply rail. The maximum positive input voltage allowed is 1 V less than the positive supply rail.

The AD627 in amp delivers rail-to-rail output swing, and operates over a wide supply voltage range (+2.7 V to ±18 V). Without the external gain setting resistor R_G, the in amp gain is a minimum of 5. Gains

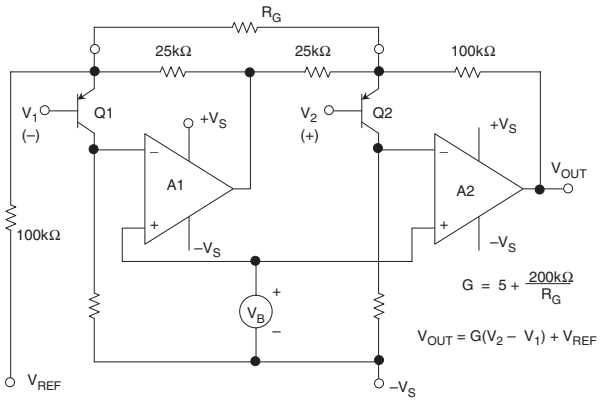


Figure 2-10: The AD627 in amp architecture

up to 1000 can be set with the addition of this external resistor. Common-mode rejection of the AD627B at 60 Hz with a 1 kΩ source imbalance is 85 dB when operating on a single 3 V supply and G = 5.

Even though the AD627 is a two-op-amp in amp, it is worthwhile noting that it is not subject to the same CM frequency response limitations as the basic circuit of Figure 2-7. A patented circuit keeps the AD627 CMR flat out to a much higher frequency than would otherwise be achievable with a conventional discrete two-op-amp in amp.

The AD627 data sheet has a detailed discussion of allowable input/output voltage ranges as a function of gain and power supply voltages (see Reference 7). In addition, interactive design tools that perform calculations relating these parameters for a number of in amps, including the AD627 are available on the ADI Web site.

Key specifications for the AD627 are summarized in Figure 2-11. Although it has been designed as a low power, single-supply device, the AD627 is capable of operating on traditional higher voltage supplies such as ±15 V, with excellent performance.

- Wide Supply Range: +2.7V to ±18V
- Input Voltage Range: $–V_S – 0.1V$ to $+V_S – 1V$
- 85µA Supply Current
- Gain Range: 5 to 1000
- 75µV Maximum Input Offset Volage (AD627B)
- 10ppm/°C Maximum Offset Voltage TC (AD627B)
- 10ppm Gain Nonlinearity
- 85dB CMR @ 60Hz, 1kΩ Source Imbalance (G = 5)
- 3µV p-p 0.1Hz to 10Hz Input Voltage Noise (G = 5)

Figure 2-11: AD627 in amp key specifications

Three-Op-Amp In Amps

A second popular in amp architecture is based on three op amps, and is shown in Figure 2-12. This circuit is typically referred to as the *three-op-amp in amp*.

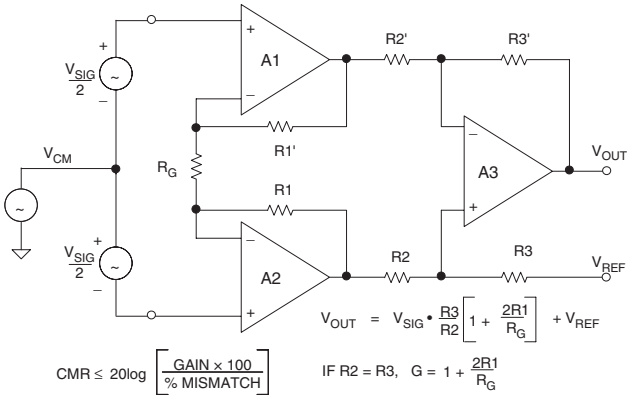


Figure 2-12: The three-op-amp in amp

Resistor R_G sets the overall gain of this amplifier. It may be internal, external, or (software or pin-strap) programmable, depending upon the in amp. In this configuration, CMR depends upon the ratio-matching of R3/R2 to R3'/R2'. Furthermore, common-mode signals are only amplified by a factor of 1, regardless of gain. (No common-mode voltage will appear across R_G, hence, no common-mode current will flow in it because the input terminals of an op amp will have no significant potential difference between them.)

As a result of the high ratio of differential-to-CM gain in A1–A2, CMR of this in amp theoretically increases in proportion to gain. Large common-mode signals (within the A1–A2 op amp headroom limits) may be handled at all gains. Finally, because of the symmetry of this configuration, common mode errors in the input amplifiers, if they track, tend to be canceled out by the subtractor output stage. These features explain the popularity of this three-op-amp in amp configuration—it is capable of delivering the highest performance.

The classic three-op-amp configuration has been used in a number of monolithic IC in amps (see References 8 and 9). Besides offering excellent matching between the three internal op amps, thin film laser trimmed resistors provide excellent ratio matching and gain accuracy at much lower cost than using discrete precision op amps and resistor networks. The AD620 (see Reference 10) is an excellent example of monolithic IC in amp technology. A simplified device schematic is shown in Figure 2-13.

The AD620 is a highly popular in amp and is specified for power supply voltages from ±2.3 V to ±18 V. Input voltage noise is only $9\,nV/\sqrt{Hz}$ @ 1 kHz. Maximum input bias current is only 1 nA, due to the use of superbeta transistors for Q1–Q2.

Overvoltage protection is provided by the internal 400 Ω thin-film current-limit resistors in conjunction with the diodes connected from the emitter-to-base of Q1 and Q2. The gain G is set with a single external R_G resistor, as noted by Eq. 2-4.

$$G = \left(49.4\,k\Omega/R_G\right) + 1 \qquad \text{Eq. 2-4}$$

As can be noted from this expression and Figure 2-13, the AD620 internal resistors are trimmed so that standard 1% or 0.1% resistors can be used to set gain to popular values.

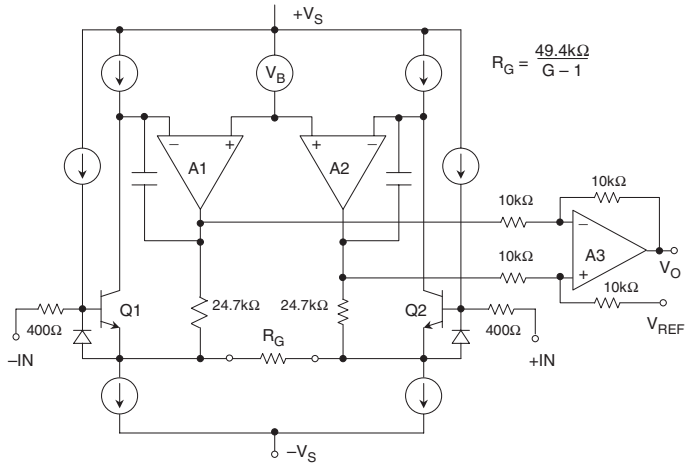


Figure 2-13: The AD620 in amp simplified schematic

As is true in the case of the two-op-amp in amp configuration, single supply operation of the three-op-amp in amp requires an understanding of the internal node voltages. Figure 2-14 shows a generalized diagram of the in amp operating on a single 5 V supply. The maximum and minimum allowable output voltages of the individual op amps are designated V_{OH} (maximum high output) and V_{OL} (minimum low output), respectively.

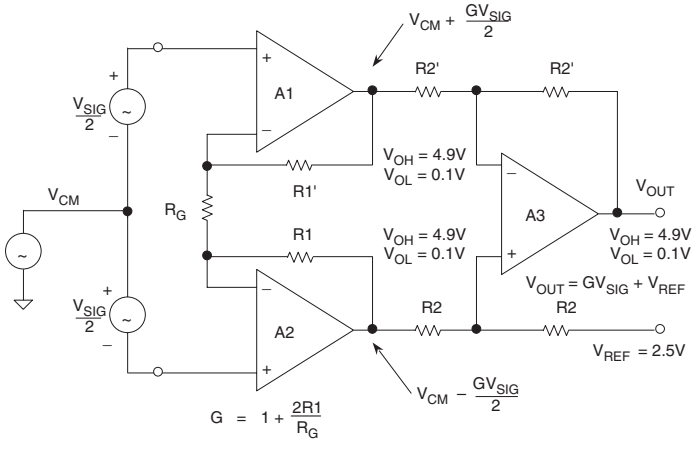


Figure 2-14: Three-op-amp in amp single 5 V supply restrictions

Note that the gain from the common-mode voltage to the outputs of A1 and A2 is unity. It can be stated that *the sum of the common-mode voltage and the signal voltage at these outputs must fall within the amplifier output voltage range*. Obviously this configuration cannot handle input common-mode voltages of either zero volts or 5 V, because of saturation of A1 and A2. As in the case of the two-op-amp in amp, the output reference is positioned halfway between V_{OH} and V_{OL} to allow for bipolar differential input signals.

While there are a number of good single-supply in amps, such as the AD627 discussed above, the highest performance devices are still among those specified for traditional dual-supply operation, i.e., the

just-discussed AD620. For certain applications, even such devices as the AD620, which has been designed for dual supply operation, can be used with full precision on a single-supply power system.

Precision Single-Supply Composite In Amp

One way to achieve both high precision and single-supply operation takes advantage of the fact that many popular sensors (e.g. strain gauges) provide an output signal that is inherently centered around an approximate mid-point of the supply voltage (and/or the reference voltage). Taking advantage of this basic point allows the inputs of a signal conditioning in amp to be biased at "mid-supply." As a consequence of this step, the inputs needn't operate near ground or the positive supply voltage, and the in amp can still be used with all its precision.

Under these conditions, an AD620 dual-supply in amp referenced to the supply mid-point followed by an rail-to-rail op amp output gain stage provides very high dc precision. Figure 2-15 illustrates one such high performance in amp, which operates on a single 5 V supply.

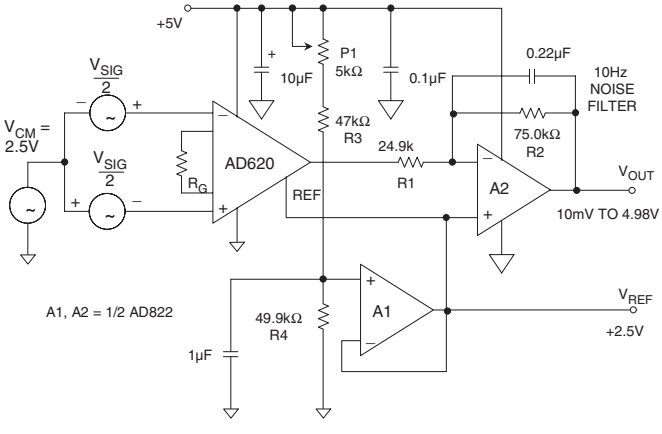


Figure 2-15: A precision single-supply composite in amp with rail-to-rail output

This circuit uses the AD620 as a low-cost precision in amp for the input stage, along with an AD822 JFET-input dual rail-to-rail output op amp for the output stage, comprised of A1 and A2. The output stage operates at a fixed gain of 3, with overall gain set by R_G.

In this circuit, R3 and R4 form a voltage divider which splits the supply voltage nominally in half to 2.5 V, with fine adjustment provided by a trimming potentiometer, P1. This voltage is applied to the input of A1, an AD822 voltage follower, which buffers it and provides a low impedance source needed to drive the AD620's reference pin as well as providing the output reference voltage V_{REF}. *Note that this feature allows a* bipolar V_{OUT} *to be measured with respect to this 2.5 V reference (not to GND).* This is despite the fact that the entire circuit operates from a single (unipolar) supply.

The other half of the AD822 is connected as a gain-of-3 inverter, so that it can output ±2.5 V, "rail-to-rail," with only ±0.83 V required of the AD620. This output voltage level of the AD620 is well within the AD620's capability, thus ensuring high linearity for the front end.

The general gain expression for this composite in amp is the product of the gain of the AD620 stage, and the gain of inverting amplifier:

$$\text{GAIN} = \left(\frac{49.4\,\text{k}\Omega}{R_G} + 1\right)\left(\frac{R2}{R1}\right). \qquad \text{Eq. 2-5}$$

For this example, an overall gain of 10 is realized with R_G = 21.5 kΩ (closest standard value). The table shown in Figure 2-16 summarizes various R_G gain values, and the resulting performance for gains ranging from 10 to 1000.

CIRCUIT GAIN	R_G (Ω)	V_{OS}, RTI (μV)	TC V_{OS}, RTI (μV/°C)	NONLINEARITY (ppm) *	BANDWIDTH (kHz)**
10	21.5k	1000	1000	< 50	600
30	5.49k	430	430	< 50	600
100	1.53k	215	215	< 50	300
300	499	150	150	< 50	120
1000	149	150	150	< 50	30

*Nonlinearity Measured Over Output Range: 0.1V < V_{OUT} < 4.90V
**Without 10Hz Noise Filter

Figure 2-16: Performance summary of the 5 V single-supply AD620/AD822 composite in amp

In this application, the allowable input voltage on either input to the AD620 must lie between 2 V and 3.5 V in order to maintain linearity. For example, at an overall circuit gain of 10, the common-mode input voltage range spans 2.25 V to 3.25 V, allowing room for the ±0.25 V full-scale differential input voltage required to drive the output ±2.5 V about V_{REF}.

The inverting configuration was chosen for the output buffer to facilitate system output offset voltage adjustment by summing currents into the A2 stage buffer's feedback summing node. These offset currents can be provided by an external DAC, or from a resistor connected to a reference voltage.

The AD822 rail-to-rail output stage exhibits a very clean transient response (not shown) and a small-signal bandwidth over 100 kHz for gain configurations up to 300. Note that excellent linearity is maintained over 0.1 V to 4.9 V V_{OUT}.

To reduce the effects of unwanted noise pickup, a filter capacitor is recommended across A2's feedback resistance to limit the circuit bandwidth to the frequencies of interest. This capacitor forms a first order low-pass filter with R2. The corner frequency is 10 Hz as shown, but this may be easily modified. The capacitor should be a high quality film type, such as polypropylene.

The AD623 In Amp

Like the two-op-amp in amp counterparts discussed previously, three-op-amp in amps require special design attention for wide CM range inputs on single power supplies. The AD623 single supply in amp configuration (see Reference 11), shown below in Figure 2-17 offers an attractive solution. In this device PNP emitter follower level shifters Q1 and Q2 allow the input signal to go 150 mV below the negative supply, and to within 1.5 V of the positive supply. The AD623 is fully specified for both single power supplies between 3 V and +12 V, and dual supplies between ±2.5 V and ±6 V.

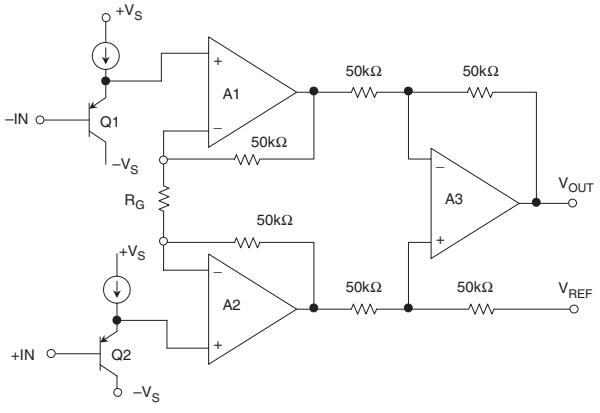


Figure 2-17: AD623 single-supply in amp architecture

The AD623 data sheet (Reference 11, again) contains excellent discussions and data on allowable input/output voltage ranges as a function of gain and power supply voltages. In addition, interactive design tools that perform calculations relating these parameters for a number of in amps, including the AD623, are available on the ADI Web site.

The key specifications of the AD623 are summarized in Figure 2-18.

- Wide Supply Range: +3V to ±6V
- Input Voltage Range: $-V_S - 0.15V$ to $+V_S - 1.5V$
- 575µA Maximum Supply Current
- Gain Range: 1 to 1000
- 100µV Maximum Input Offset Voltage (AD623B)
- 1µV/°C Maximum Offset Voltage TC (AD623B)
- 50ppm Gain Nonlinearity
- 105dB CMR @ 60Hz, 1kΩ Source Imbalance, G≥100
- 3µV p-p 0.1Hz to 10Hz Input Voltage Noise (G = 1)

Figure 2-18: AD623 in amp key specifications

In Amp DC Error Sources

The dc and noise specifications for in amps differ slightly from conventional op amps, so some discussion is required in order to fully understand the error sources.

The gain of an in amp is usually set by a single resistor. If the resistor is external to the in amp, its value is either calculated from a formula or chosen from a table on the data sheet, depending on the desired gain.

Absolute value laser wafer trimming allows the user to program gain accurately with this single resistor. The absolute accuracy and temperature coefficient of this resistor directly affects the in amp gain accuracy and drift. Since the external resistor will never exactly match the internal thin film resistor tempcos, a low TC (<25 ppm/°C) metal film resistor should be chosen, preferably with a 0.1% or better accuracy.

Often specified as having a gain range of 1 to 1000, or 1 to 10,000, many in amps will work at higher gains, but the manufacturer will not guarantee a specific level of performance at these high gains. In practice, as the gain-setting resistor becomes smaller, any errors due to the resistance of the metal runs and bond wires become significant. These errors, along with an increase in noise and drift, may make higher single-stage gains impractical. In addition, input offset voltages can become quite sizable when reflected to output at high gains. For instance, a 0.5 mV input offset voltage becomes 5 V at the output for a gain of 10,000. For high gains, the best practice is to use an in amp as a preamplifier, then use a post amplifier for further amplification.

In a *pin-programmable-gain* in amp such as the AD621, the gain-set resistors are internal, well matched, and the device gain accuracy and gain drift specifications include their effects. The AD621 is otherwise generally similar to the externally gain-programmed AD620.

The *gain error* specification is the maximum deviation from the gain equation. Monolithic in amps such as the AD624C have very low factory trimmed gain errors, with its maximum error of 0.02% at G = 1 and 0.25% at G = 500 being typical for this high quality in amp. Notice that the gain error increases with increasing gain. Although externally connected gain networks allow the user to set the gain exactly, the temperature coefficients of the external resistors and the temperature differences between individual resistors within the network all contribute to the overall gain error. If the data is eventually digitized and presented to a digital processor, it may be possible to correct for gain errors by measuring a known reference voltage and then multiplying by a constant.

Nonlinearity is defined as the maximum deviation from a straight line on the plot of output versus input. The straight line is drawn between the end points of the actual transfer function. Gain nonlinearity in a high quality in amp is usually 0.01% (100 ppm) or less, and is relatively insensitive to gain over the recommended gain range.

The total *input offset voltage* of an in amp consists of two components (see Figure 2-19). *Input* offset voltage, V_{OSI}, is the input offset component that is reflected to the output of the in amp by the gain G. *Output* offset voltage, V_{OSO}, is independent of gain.

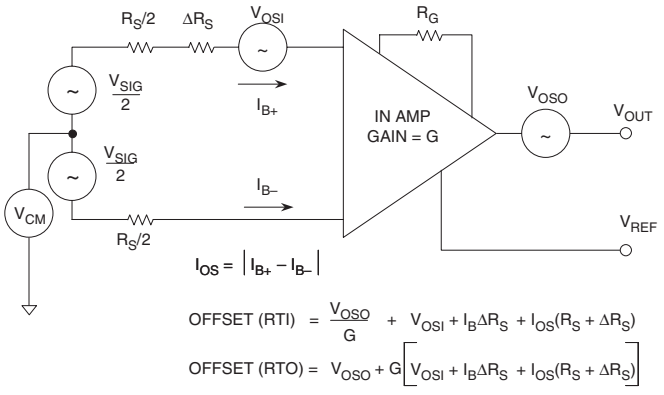


Figure 2-19: In amp offset voltage model

At low gains, output offset voltage is dominant, while at high gains input offset dominates. The output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by a drift specification at a high gain (where output offset effects are negligible).

The total output offset error, referred to the input (RTI), is equal to $V_{OSI} + V_{OSO}/G$. In amp data sheets may specify V_{OSI} and V_{OSO} separately, or give the total RTI input offset voltage for different values of gain.

Input bias currents may also produce offset errors in in amp circuits (Figure 2-19). If the source resistance, R_S, is unbalanced by an amount, ΔR_S, (often the case in bridge circuits), there is an additional input offset voltage error due to the bias current, equal to $I_B\Delta R_S$ (assuming that $I_{B+} \approx I_{B-} = I_B$). This error is reflected to the output, scaled by the gain G.

The input offset current, I_{OS}, creates an input offset voltage error across the source resistance, $R_S + \Delta R_S$, equal to $I_{OS}(R_S + \Delta R_S)$, which is also reflected to the output by the gain, G.

In amp *common-mode error* is a function of both gain and frequency. Analog Devices specifies in amp CMR for a 1 kΩ source impedance unbalance at a frequency of 60 Hz. The RTI common-mode error is obtained by dividing the common-mode voltage, V_{CM}, by the common-mode rejection ratio, CMRR.

Figure 2-20 shows the CMR for the AD620 in amp as a function of frequency, with a 1 kΩ source impedance imbalance.

Power supply rejection (PSR) is also a function of gain and frequency. For in amps, it is customary to specify the sensitivity to each power supply separately, as shown in Figure 2-21 for the AD620. The RTI power supply rejection error is obtained by dividing the power supply deviation from nominal by the power supply rejection ratio, PSRR.

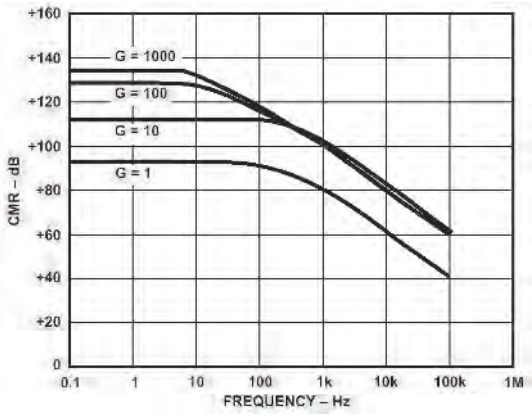


Figure 2-20: AD620 In amp common-mode rejection (CMR) versus frequency for 1 kΩ source imbalance

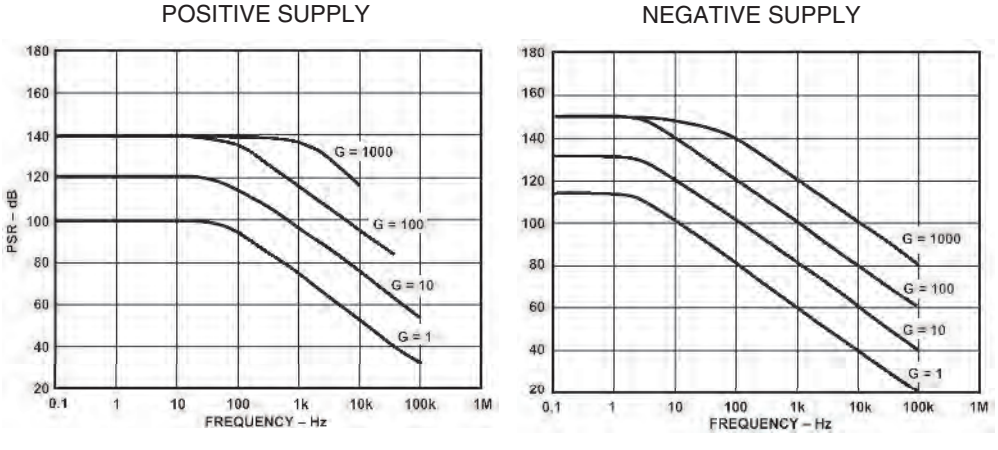


Figure 2-21: AD620 in amp power supply rejection (PSR) versus frequency

Because of the relatively poor PSR at high frequencies, decoupling capacitors are required on both power pins to an in amp. Low inductance ceramic capacitors (0.01 µF to 0.1 µF) are appropriate for high frequencies. Low ESR electrolytic capacitors should also be located at several points on the PC board for low frequency decoupling.

Note that these decoupling requirements apply to all linear devices, including op amps and data converters. Further details on power supply decoupling are found in Chapter 7.

Now that all dc error sources have been accounted for, a worst case dc error budget can be calculated by reflecting all the sources to the in amp input, as is illustrated by the table of Figure 2-22.

It should be noted that the dc errors can be referred to the in amp output (RTO), by simply multiplying the RTI error by the in amp gain.

ERROR SOURCE	RTI VALUE
Gain Accuracy (ppm)	Gain Accuracy × FS Input
Gain Nonlinearity (ppm)	Gain Nonlinearity × FS Input
Input Offset Voltage, V_{OSI}	V_{OSI}
Output Offset Voltage, V_{OSO}	$V_{OSO} \div G$
Input Bias Current, I_B, Flowing in ΔR_S	$I_B \Delta R_S$
Input Offset Current, I_{OS}, Flowing in R_S	$I_{OS}(R_S + \Delta R_S)$
Common Mode Input Voltage, V_{CM}	$V_{CM} \div CMRR$
Power Supply Variation, ΔV_S	$\Delta V_S \div PSRR$

Figure 2-22: In amp dc errors referred to the input (RTI)

In Amp Noise Sources

Since in amps are primarily used to amplify small precision signals, it is important to understand the effects of all the associated noise sources. The in amp noise model is shown in Figure 2-23.

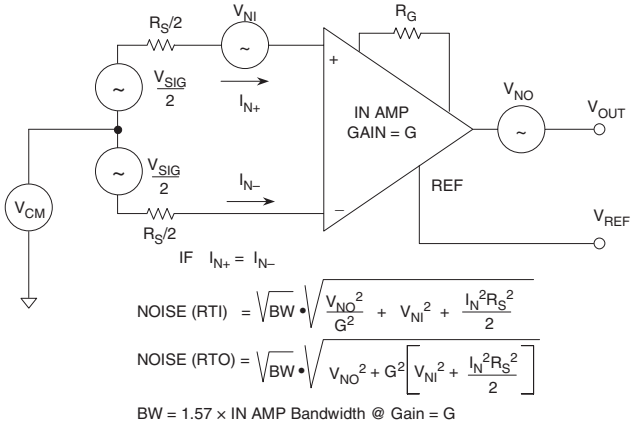


Figure 2-23: In amp noise model

There are two sources of input voltage noise. The first is represented as a noise source, V_{NI}, in series with the input, as in a conventional op amp circuit. This noise is reflected to the output by the in amp gain, G. The second noise source is the output noise, V_{NO}, represented as a noise voltage in series with the in amp output. The output noise, shown here referred to V_{OUT}, can be referred to the input by dividing by the gain, G.

There are also two noise sources associated with the input noise currents I_{N+} and I_{N-}. Even though I_{N+} and I_{N-} are usually equal ($I_{N+} \approx I_{N-} = I_N$), they are *uncorrelated*, and therefore, the noise they each create must be

summed in a root-sum-squares (RSS) fashion. I_{N+} flows through one-half of R_S, and I_{N-} the other half. This generates two noise voltages, each having an amplitude, $I_N R_S/2$. Each of these two noise sources is reflected to the output by the in amp gain, G.

The total output noise is calculated by combining all four noise sources in an RSS manner:

$$\text{NOISE}(\text{RTO}) = \sqrt{\text{BW}}\sqrt{V_{NO}{}^2 + G^2\left(V_{NI}{}^2 + \frac{I_{N+}{}^2 R_S{}^2}{4} + \frac{I_{N-}{}^2 R_S{}^2}{4}\right)} \qquad \text{Eq. 2-6}$$

If $I_{N+} = I_{N-} = I_N$,

$$\text{NOISE}(\text{RTO}) = \sqrt{\text{BW}}\sqrt{V_{NO}{}^2 + G^2\left(V_{NI}{}^2 + \frac{I_N{}^2 R_S{}^2}{2}\right)} \qquad \text{Eq. 2-7}$$

The total noise, referred to the input (RTI) is simply the above expression divided by the in amp gain, G:

$$\text{NOISE}(\text{RTI}) = \sqrt{\text{BW}}\sqrt{\frac{V_{NO}{}^2}{G^2} + \left(V_{NI}{}^2 + \frac{I_N{}^2 R_S{}^2}{2}\right)} \qquad \text{Eq. 2-8}$$

In amp data sheets often present the total voltage noise RTI as a function of gain. This noise spectral density includes both the input (V_{NI}) and output (V_{NO}) noise contributions. The input current noise spectral density is specified separately.

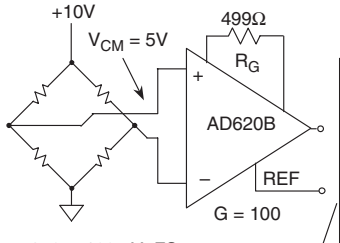
As in the case of op amps, the total in amp noise RTI must be integrated over the applicable in amp closed-loop bandwidth to compute an RMS value. The bandwidth may be determined from data sheet curves that show frequency response as a function of gain.

Regarding this bandwidth, some care must be taken in computing it, as it is often *not* constant bandwidth product relationship, as is true with VFB op amps. In the case of the AD620 in amp family for example, the gain-bandwidth pattern is more like that of a CFB op amp. In such cases, the safest way to predict the bandwidth at a given gain is to use the curves supplied within the data sheet.

In Amp Bridge Amplifier Error Budget Analysis

It is important to understand in amp error sources in a typical application. Figure 2-24 shows a 350 Ω load cell with a full-scale output of 100 mV when excited with a 10 V source. The AD620 is configured for a gain of 100 using the external 499 Ω gain-setting resistor. The table shows how each error source contributes to a total unadjusted error of 2145 ppm. Note, however, that the gain, offset, and CMR errors can all be removed with a system calibration. The remaining errors—gain nonlinearity and 0.1 Hz to 10 Hz noise—cannot be removed with calibration and ultimately limit the system resolution to 42.8 ppm (approximately 14-bit accuracy).

This example is of course just an illustration, but should be useful towards the importance of addressing performance-limiting errors such as gain nonlinearity and LF noise.



AD620B SPECS @ 25°C, ±15V
$V_{OSI} + V_{OSO}/G$ = 55µV max
I_{OS} = 0.5nA max
Gain Error = 0.15%
Gain Nonlinearity = 40ppm
0.1Hz to 10Hz Noise = 280nVp-p
CMR = 120dB @ 60Hz

MAXIMUM ERROR CONTRIBUTION, +25°C
FULLSCALE: V_{IN} = 100mV, V_{OUT} = 10V

V_{OS}	55µV ÷ 100mV	550ppm
I_{OS}	350Ω × 0.5nA ÷ 100mV	1.8ppm
Gain Error	0.15%	1500ppm
Gain Nonlinearity	40ppm	40ppm
CMR Error	120dB 1ppm × 5V ÷ 100mV	50ppm
0.1Hz to 10Hz 1/f Noise	280nV ÷ 100mV	2.8ppm
Total Unadjusted Error	≈ 9 Bits Accurate	2145ppm
Resolution Error	≈ 14 Bits Accurate	42.8ppm

Figure 2-24: AD620B bridge amplifier dc error budget

In Amp Performance Tables

Figure 2-25 shows a selection of precision in amps designed primarily for operation on dual supplies. It should be noted that the AD620 is capable of single 5 V supply operation (see Figure 2-15), but neither its input nor its output are capable of rail-to-rail swings.

These tables allow at-a-glance inspection of key errors, which can be critical in getting the most performance from a system. From Figure 2-25 for example, it can be noted that the use of an AD621 in lieu of the AD620B in the gain-of-100 bridge circuit of Figure 2-24 allows reduction of the gain nonlinearity component of error by a factor of four times. It is also important to separate out errors that can be calibrated out as mentioned above, and those that can only be minimized by device specification improvements. Comparison of the AD620B and the AD622 specifications, for example, shows a higher V_{OS} for the latter. But, since VOS can be calibrated out, the fact that it is higher for the AD622 isn't material to this particular application. The gain nonlinearity between the AD620 and AD622 is the same, so in an auto-cal system, they would likely perform comparably. On the other hand, the AD621B would be preferable for its lower gain nonlinearity, as noted.

	Gain Accuracy *	Gain Nonlinearity	V_{OS} Max	V_{OS} TC	CMR Min	0.1Hz to 10Hz p-p Noise
AD524C	0.5% / P	100ppm	50µV	0.5µV/°C	120dB	0.3µV
AD620B	0.5% / R	40ppm	50µV	0.6µV/°C	120dB	0.28µV
AD621B[1]	0.05% / P	10ppm	50µV	1.6µV/°C	100dB	0.28µV
AD622	0.5% / R	40ppm	125µV	1µV/°C	103dB	0.3µV
AD624C[2]	0.25% / R	50ppm	25µV	0.25µV/°C	130dB	0.2µV
AD625C	0.02% / R	50ppm	25µV	0.25µV/°C	125dB	0.2µV
AMP01A	0.6% / R	50ppm	50µV	0.3µV/°C	125dB	0.12µV
AMP02E	0.5% / R	60ppm	100µV	2µV/°C	115dB	0.4µV

*/P = Pin Programmable
*/R = Resistor Programmable
[1] G = 100
[2] G = 500

Figure 2-25: Precision in amps: data for V_s = ±15 V, G = 1000

In amps specifically designed for single supply operation are also shown, in Figure 2-26. It should be noted that although the specifications in this figure are given for a single 5 V supply, all of the amplifiers are also capable of dual supply operation and are specified for both dual and single supply operation on their data sheets. In addition, the AD623 and AD627 will operate on a single 3 V supply

	Gain Accuracy *	Gain Nonlinearity	V_{OS} Max	V_{OS} TC	CMR Min	0.1Hz to 10Hz p-p Noise	Supply Current
AD623B	0.5% / R	50ppm	100µV	1µV/°C	105dB	1.5µV	575µA
AD627B	0.35% / R	10ppm	75µV	1µV/°C	85dB	1.5µV	85µA
AMP04E	0.4% / R	250ppm	150µV	3µV/°C	90dB	0.7µV	290µA
AD626B[1]	0.6% / P	200ppm	2.5mV	6µV/°C	80dB	2µV	700µA

*/P = Pin Programmable
*/R = Resistor Programmable
[1] Differential Amplifier, G = 100

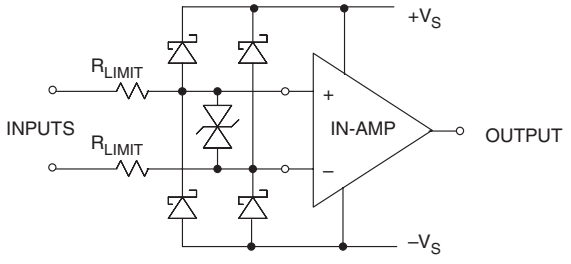
Figure 2-26: Single-supply in amps: data for V_s = 5 V, G = 1000

Note that the AD626 is not a true in amp, but is in fact a differential amplifier with a thin-film input attenuator that allows the common-mode voltage to exceed the supply voltages. This device is designed primarily for high- and low-side current-sensing applications. It will also operate on a single 3 V supply.

In Amp Input Overvoltage Protection

As interface amplifiers for data acquisition systems, in amps are often subjected to input overloads, i.e., voltage levels in excess of the full scale for the selected gain range. The manufacturer's "absolute maximum" input ratings for the device should be closely observed. As with op amps, many in amps have absolute maximum input voltage specifications equal to $\pm V_S$.

In some cases, external series resistors (for current limiting) and diode clamps may be used to prevent overload if necessary (see Figure 2-27). Some in amps have built-in overload protection circuits in the form of series resistors. For example, the AD620 series have thin film resistors, and the substrate isolation they provide allows input voltages that can exceed the supplies. Other devices use series-protection FETs; for example, the AMP02 and the AD524, because they act as a low impedance during normal operation, and a high impedance during overvoltage fault conditions. In any instance however, there are always finite safe limits to applied overvoltage (Figure 2-27).



- Always Observe Absolute Maximum Data Sheet Specs
- Schottky Diode Clamps to the Supply Rails Will Limit Input to Approximately ±V_S ±0.3V, TVSs Limit Differential Voltage
- External Resistors (or Internal Thin-Film Resistors) Can Limit Input Current, but will Increase Noise
- Some In-Amps Have Series-Protection Input FETs for Lower Noise and Higher Input Overvoltages (up to ±60V, Depending on Device)

Figure 2-27: In amp input overvoltage considerations

In some instances, an additional Transient Voltage Suppressor (TVS) may be required across the input pins to limit the maximum differential input voltage. This is especially applicable to three-op-amp in amps operating at high gain with low values of R_G.

A more detailed discussion of input overvoltage and EMI/RFI protection can be found in Chapter 7 of this book.

In Amp Applications

Some representative in amp applications round out this section, illustrating how the characteristics lend utility and efficiency to a range of circuits.

In Amp Bridge Amplifier

In amps are widely used as precision signal conditioning elements. A popular application is a bridge amplifier, shown in Figure 2-28. The in amp is ideally suited for this application because the bridge output is fundamentally balanced, and the in amp presents it with a truly balanced high impedance load. The nominal resistor values in the bridge can range from 100 Ω to several kΩ, but 350 Ω is popular for most precision load cells.

Full-scale output voltages from a typical bridge circuit can range from approximately 10 mV to several hundred mV. Typical in amp gains in the order of 100 to 1000 are therefore ideally suited for amplifying these small voltages to levels compatible with popular analog-to-digital converter (ADC) input voltage ranges (usually 1 V to 10 V full scale).

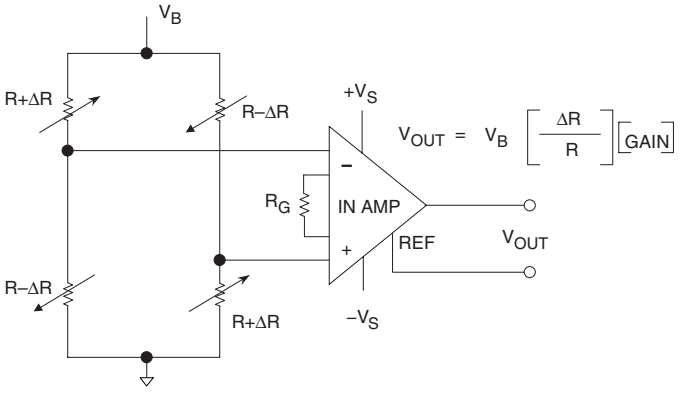


Figure 2-28: Generalized bridge amplifier using an in amp

In addition, the in amp's high CMR at power line frequencies allows common-mode noise to be rejected, when the bridge must be located remotely from the in amp.

Note that a much more thorough discussion of bridge applications can be found in Chapter 4 of this book.

In Amp A/D Interface

Interfacing bipolar signals to single-supply ADCs presents a challenge. The bipolar signal must be amplified and level-shifted into the input range of the ADC. Figure 2-29 shows how this translation can be achieved using the AD623 in amp, when interfacing a bridge circuit to the AD7776 10-bit, 2.5 µs ADC.

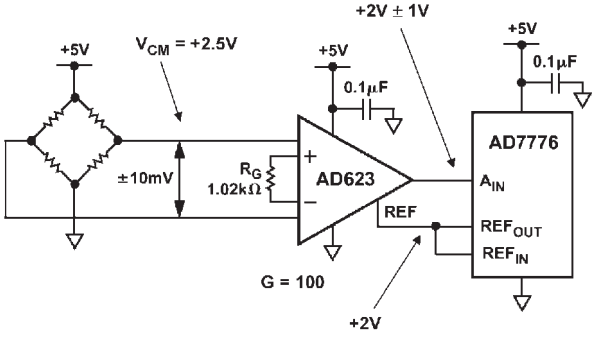


Figure 2-29: Single-supply data acquisition system

The bridge circuit is excited by a 5 V supply. The full-scale output from the bridge (±10 mV) therefore has a common-mode voltage of 2.5 V. The AD623 removes the common-mode component, and amplifies the bridge output by a factor of 100 (R_G = 1.02 kΩ).

This results in an output signal swing of ±1 V. This signal is level-shifted by connecting the REF pin of the AD623 to the 2 V REF_{OUT} of the AD7776 ADC. This sets the common-mode output voltage of the AD623 to 2 V, and the resulting signal into the ADC is +2 V ±1 V, corresponding to the input range of the AD7776.

In Amp Driven Current Source

Figure 2-30 shows a precision voltage-controlled current source using an in amp. The input voltage V_{IN} develops an output voltage, V_{OUT}, equal to GV_{IN} between the output pin of the AD620 and the REF pin. With the connections shown, V_{OUT} is also applied across sense resistor R_{SENSE}, thus developing a load current of V_{OUT}/R_{SENSE}. The OP97 acts as a unity gain buffer to isolate the load from the 20 kΩ impedance of the REF pin of the AD620. In this circuit the input voltage can be floating with respect to the load ground (as long as there exists a path for the in amp bias currents). The high CMR of the in amp allows high accuracy to be achieved for the load current, despite CM voltages.

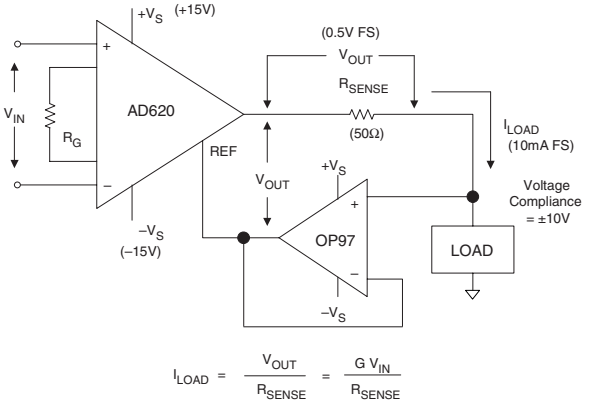


Figure 2-30: Precision voltage-controlled current source using an in amp

The circuit will work for both large and small values of G in the AD620. The most simple form would be to let G = 1 with RG open. In this case, $V_{OUT} = V_{IN}$, and I_{LOAD} is proportional to V_{IN}. But the gain factor of the in amp can readily be used to scale almost any input voltage to a desired current level.

The output load voltage compliance is typically ±10 V when operating on ±15 V power supplies, and load currents up to ±15 mA are allowable, limited by the AD620's drive. A typical operating condition might be a full scale load current of 10 mA, a full-scale V_{OUT} = 0.5 V, and R_{SENSE} = 50 Ω.

For small values of R_{SENSE}, the OP97 buffer could possibly be eliminated provided the resulting error incurred by the loading effect of the AD620 REF pin is acceptable. In this case the load and bottom R_{SENSE} node would be connected directly to the in amp REF pin.

Many other useful variations of the basic circuit exist, and can easily be added. For currents of up to 50 mA, a unity gain, low offset buffer can be added between the AD620 output and the top of R_{SENSE}. This will remove all load current from the AD620, allowing it to operate with greatest linearity.

The circuit is also very useful at very small currents. It will work well with the OP97 down to around 1 μA, before bias current of the op amp becomes a performance limitation. For even lower currents, a precision JFET op amp such as the AD8610 can easily be substituted. This step will allow precise low level currents, down to below 1 nA. Note that the AD8610 must be operated on supplies of ±13 V or less, but this isn't necessarily a problem (the AD620 will still operate well on supplies as low as ±2.5 V).

A factor that may not be obvious is that the output current capability of this current source is bilateral, as it is shown. This makes this form of current source a great advantage over a Howland type current source, which are always problematic with the numerous resistors required, which must be well-matched and stable for good performance. In contrast, the current source of Figure 2-30 is clean and efficient, requires no matched resistors, and is precise over very wide current ranges.

In Amp Remote Load Driver

Often remote loads present a problem in driving, when high accuracy must be maintained at the load end. For this type of requirement, an in amp (or simple differential amplifier) with separate SENSE/FORCE terminals can serve very well, providing a complete solution in one IC. Most of the more popular in amps available today have removed the separate SENSE/FORCE connections, due to the pin limitations of an 8-pin package (AD620, etc.). However, many classic in amps such as the AMP01 do have access to the SENSE/FORCE pins, and can perform remote sensing, as shown in Figure 2-31.

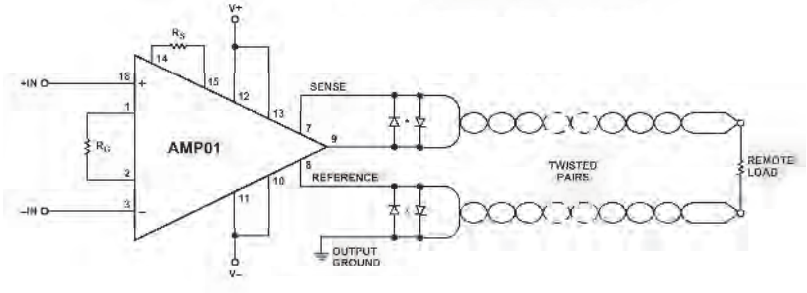


Figure 2-31: Precision in amp remote load driver using FORCE/SENSE connections

In this circuit a quad cable composed of two twisted pairs is used. One pair is dedicated to the load HIGH side, the other to the LO side. At the remote end, the load is connected as shown, with each twisted pair terminated at one end of the load.

Although the full load current still flows in the FORCE (AMP01 Pin 9) and OUTPUT GROUND connections, the resulting drop does not create an error, since the remote sensing of the second lead of each pair is returned back to the driver, and carries comparatively very little current. The reverse-parallel connected diodes are optional, and perform a "safety-valve" function, in case a sense line becomes open-circuit (100 Ω resistors might also be used).

The AMP01 is valuable to this function not simply because of the SENSE/FORCE capability, but because it also is capable of 50 mA output currents and is stable with the capacitive loading presented by a cable. Alternately, a precision differential amplifier like the AMP03 can also be used, at lower current levels.

For additional in amp background and reference material, see References 12 through 15.

References: Instrumentation Amplifiers

1. MIL-PRF-55182G, "Resistors, Fixed, Film, Nonestablished Reliability, Established Reliability, And Space Level, General Specification For," June 9, 1997.
2. Robert Demrow, "Narrowing the Margin of Error," **Electronics**, April 15, 1968, pp. 108–117.
3. Robert Demrow, "Evolution from Operational Amplifier to Data Amplifier," **Analog Devices Application Note**, September, 1968.
4. David Birt, "Electronically Balanced Analogue-Line Interfaces," **Proceedings of Institute of Acoustics Conference**, Windermere, U.K., Nov. 1990.
5. Walt Jung, "Op Amps in Line-Driver and Receiver Circuits, Part 1," **Analog Dialogue**, Vol. 26 No. 2, 1992.
6. W. Jung, A. Garcia, "Op Amps in Line-Driver and Receiver Circuits, Part 2," **Analog Dialogue**, Vol. 27, No. 1, 1993.
7. Data sheet for **AD627 Micropower, Single and Dual Supply Rail-to-Rail Instrumentation Amplifier**, www.analog.com.
8. S. Wurcer, L. Counts, "A Programmable Instrumentation Amplifier for 12-Bit Resolution Systems," **IEEE Journal of Solid-State Circuits**, Vol. SC-17 #6, Dec. 1982, pp. 1102–1111.
9. L. Counts, S. Wurcer, "Instrumentation Amplifier Nears Input Noise Floor," **Electronic Design**, June 10, 1982, p. 177.
10. Data sheet for **AD620 Low Cost, Low Power Instrumentation Amplifier**, www.analog.com
11. Data sheet for **AD623 Single Supply, Rail-to-Rail, Low Cost Instrumentation Amplifier**, www.analog.com.
12. Charles Kitchen and Lew Counts, **A Designer's Guide to Instrumentation Amplifiers**, Analog Devices, 2000.
13. Sections 2, 3, 4, of Walt Kester, Editor, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, Inc., 1999, ISBN: 0-916550-20-6.
14. Walter Borlase, "Application/Analysis of the AD520 Monolithic Data Amplifier," **Analog Devices Application Note**, 1972.
15. Jeff Riskin, **A User's Guide to IC Instrumentation Amplifiers**, **Analog Devices AN244**, January, 1978.

Classic Cameo

Robert Demrow's "Evolution from Operational Amplifier to Data Amplifier"

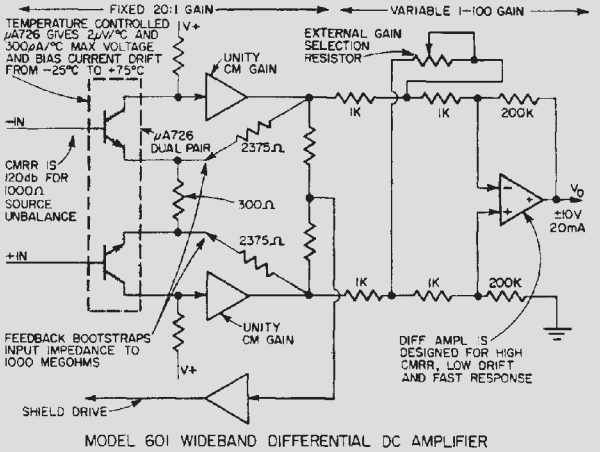


Fig. 16 - Wideband differential DC amplifier Model 601 embodies many of the principles outlined in this article. Input circuit based on uA726 temperature compensated monolithic pair provides high voltage & current stability, uses bootstrapping feedback to create 1000 megohms common mode and 10 megohms differential input impedance. Subsequent circuitry preserves uA726's inherently-wide bandwidth by using low-value resistors, which also permit highest resistance stability, hence best long-term CMRR. Single resistor adjusts closed-loop gain from 20 to 2000; fixed first-stage gain of 20:1 reduces second stage's gain-inequality error: $CMRR_A = A/(A_2 - A_1)$, twentyfold.

As applications engineering manager in the early years of ADI, Robert Demrow published numerous articles and application notes. It is a testament to the quality of these articles that most of them are still germane today—due in no small part to their lucid outlining of fundamental principles.

Demrow's 1968 application note, "Evolution from Operational Amplifier to Data Amplifier" outlined the relevant amplifier operating principles for retrieving analog signals from a noisy environment. It also introduced the ADI Model 601 *data amplifier* (above). Of course, a data amplifier is what we know today as an instrumentation amplifier. Within his Figure 16 can be seen several key operating principles: 1) dual high impedance inputs, as necessary for high CMR, 2) the use of a precision bipolar transistor differential pair front end, for low offset and drift (the µA726),[1] 3) a balanced, three amplifier stage topology.

It is interesting to note that some more popular IC in amps of 2004 utilize many of the same principles—for example, the AD620 family. Back in 1968, Robert Demrow outlined a host of sound design concepts, leading the way to later solid-state developments and the completely monolithic in amp ICs of today.

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[1] James N. Giles, Editor, "The µA726 Temperature-Stabilized Transistor Pair," Chapter 8, **Fairchild Semiconductor Linear Integrated Circuits Handbook**, Fairchild Semiconductor, 1967.

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SECTION 2-2

Programmable Gain Amplifiers

Walt Kester, James Bryant

Most data acquisition systems with wide dynamic range need some method of adjusting the input signal level to the analog-to-digital-converter (ADC). Typical ADC full-scale input voltage ranges lie between 2 V and 10 V. To achieve the rated precision of the converter, the maximum input signal should be fairly near its full-scale voltage.

Transducers, however, have a very wide range of output voltages. High gain is needed for a small sensor voltage, but with a large output, a high gain will cause the amplifier or ADC to saturate. So, some type of predictably controllable gain device is needed. Amplifiers with programmable gain have a variety of applications, and Figure 2-32 lists some of them.

- Instrumentation
- Photodiode circuits
- Ultrasound preamplifiers
- Sonar
- Wide dynamic range sensors
- Driving ADCs (some ADCs have on-chip PGAs)
- Automatic gain control (AGC) loops

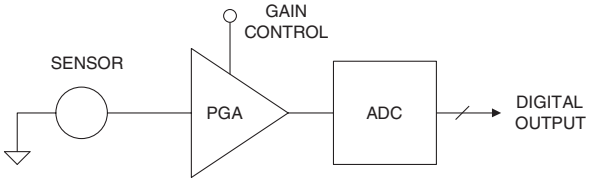
Figure 2-32: Programmable gain amplifier (PGA) applications

Such a device has a gain that is controlled by a dc voltage or, more commonly, a digital input. This device is known as a *programmable gain amplifier*, or PGA. Typical PGAs may be configured either for selectable *decade gains* such as 10, 100, 100, etc., or they might also be configured for *binary gains* such as 1, 2, 4, 8, etc. It is a function of the end system of course, which type might be the more desirable.

It should be noted that a factor common to the above application examples is that the different types of signals being handled is diverse. Some may require wide bandwidth, others very low noise, from either high or low impedance sources. The inputs may be single-ended, or they may be differential, crossing over into the realm of the just-discussed in amps.

The output from the PGA may be required to drive some defined input range of an ADC, or it may be part of a smaller subsystem, such as an AGC or gain-ranging loop. The circuits following fall into a range of categories addressing some of these requirements.

A PGA is usually located between a sensor and its ADC, as shown in Figure 2-33. Additional signal conditioning may take place before or after the PGA, depending on the application. For example, a photodiode needs a current-to-voltage converter between it and the PGA. In most other systems, it is better to place the gain first, and condition a larger signal. This reduces errors introduced by the signal conditioning circuitry.



Used to increase the dynamic range of the system

A PGA with a gain of 1 to 2 theoretically increases the dynamic range by 6dB.

A gain of 1 to 4 gives a 12dB increase, etc.

Figure 2-33: PGAs in data acquisition systems

To understand the benefits of variable gain, assume an ideal PGA with two settings, gains of one and two. The dynamic range of the system is increased by 6 dB. Increasing the gain to a maximum four results in a 12 dB increase in dynamic range. If the LSB of an ADC is equivalent to 10 mV of input voltage, the ADC cannot resolve smaller signals, but when the gain of the PGA is increased to two, input signals of 5 mV may be resolved.

Thus, a central processor can combine PGA gain information with the digital output of the ADC to increase its resolution by one bit. Essentially, this is the same as adding additional resolution to the ADC. In fact, a number of ADCs now have on-chip PGAs for increased dynamic range (AD77xx-series, for example, covered later).

PGA Design Issues

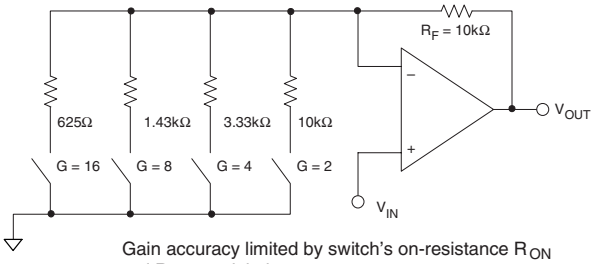
In practice, PGAs aren't ideal, and their error sources must be studied and dealt with. A number of the various PGA design issues are summarized in Figure 2-34.

A fundamental PGA design problem is programming gain accurately. Electromechanical relays have minimal on resistance (R_{ON}), but are unsuitable for gain switching—slow, large, and expensive. CMOS switches are small, but they have voltage-/temperature-dependent R_{ON}, as well as stray capacitance, which may affect PGA ac parameters.

- How to switch the gain
- Effects of the switch on-resistance (R_{ON})
- Gain accuracy
- Gain linearity
- Bandwidth versus frequency versus gain
- Dc offset
- Gain and offset drift over temperature
- Settling time after switching gain

Figure 2-34: PGA design issues

To understand R_{ON}'s effect on performance, consider Figure 2-35, a poor PGA design. A noninverting op amp has four different gain-set resistors, each grounded by a switch, with an R_{ON} of 100 Ω–500 Ω. Even with R_{ON} as low as 25 Ω, the gain of 16 error would be 2.4%, worse than 8-bits. R_{ON} also changes over temperature and switch-switch.



Gain accuracy limited by switch's on-resistance R_{ON} and R_{ON} modulation

R_{ON} typically 100 – 500Ω for CMOS or JFET switch

Even for R_{ON} = 25Ω, there is a 2.4% gain error for G = 16

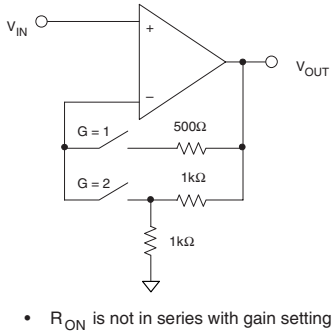
R_{ON} drift over temperature limits accuracy

Must use very low R_{ON} switches (relays)

Figure 2-35: A poorly designed PGA

To attempt "fixing" this design, the resistors might be increased, but noise and offset could then be a problem. The only way to accuracy with this circuit is to use relays, with virtually no R_{ON}. Only then will the few mΩ of relay R_{ON} be a small error vis-à-vis 625 Ω.

It is much better to use a circuit *insensitive* to R_{ON}. In Figure 2-36, the switch is placed in series with the inverting input of an op amp. Since the op amp input impedance is very large, the switch R_{ON} is now irrelevant, and gain is now determined solely by the external resistors. Note: R_{ON} may add a small offset error if op amp bias current is high (if this is the case, it can readily be compensated with an equivalent resistance at V_{IN}).



- R_{ON} is not in series with gain setting resistors
- R_{ON} is small compared to input impedance
- Only slight offset errors occur due to bias current flowing through the switches

Figure 2-36: Alternate PGA configuration minimizes the effects of R_{ON}

PGA Applications

The following section illustrates several PGA circuits using the above and other concepts.

AD526 Software Programmable PGA

The AD526 amplifier uses the just-described PGA architecture, integrating it onto a single chip, as diagrammed in Figure 2-37 (see References 1 and 2). The AD526 has five binary gain settings from 1 to 16, and its internal JFET switches are connected to the inverting input of the amplifier as in Figure 2-37. The gain resistors are laser trimmed, providing a maximum gain error of only 0.02%, and a linearity of 0.001%. The use of the FORCE/SENSE terminals connected at the load ensures highest accuracy (it also allows the use of an optional unity-gain buffer, for low impedance loads).

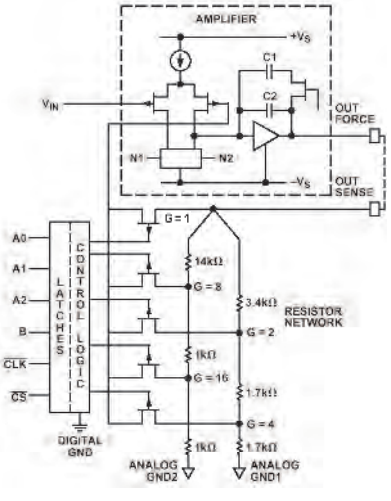


Figure 2-37: AD526 software programmable PGA simplified schematic

Functionally speaking, the AD526 is a programmable, precision, noninverting op amp gain stage, logic programmable over a range of 1 to 16 times V_{IN}. It typically operates from a ±15 V power supply, and has ±10 V output range (like a conventional op amp).

The key specifications for the AD526 are summarized in Figure 2-38.

- Software programmable binary gains from 1 to 16
- Low bias current JFET input stage
- Worst-case gain error: 0.02% (12-bit performance)
- Maximum gain nonlinearity: 0.001%
- Gain change settling time: 5.6µs (G = 16)
- Small signal bandwidth: 4MHz (G = 1), 0.35MHz (G = 16)
- Latched TTL-compatible control inputs

Figure 2-38: AD526 PGA key specifications

Low Noise PGA

This same design concepts can be used to build a low noise PGA as shown in Figure 2-39. It uses a single op amp, a quad switch, and precision resistors. The lower noise AD797 replaces the JFET input op amp of the AD526, but almost any voltage feedback op amp could be used in this circuit. The ADG412 was picked for its R_{ON} of 35 Ω.

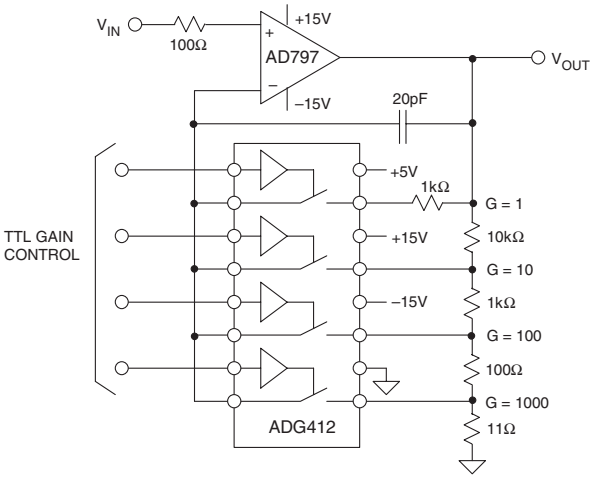


Figure 2-39: A very low noise PGA using the AD797 and the ADG412

The resistors were chosen to give decade gains of 1, 10, 100, and 1000, but if other gains are required, the resistor values may easily be altered. Ideally, a single trimmed resistor network should be used both for initial gain accuracy and for low drift over temperature. The 20 pF feedback capacitor ensures stability and holds the output voltage when the gain is switched. The control signal to the switches turns one switch off a few nanoseconds before the second switch turns on. During this break, the op amp is open-loop. Without the capacitor the output would start slewing. Instead, the capacitor holds the output voltage during switching. Since the time that both switches are open is very short, only 20 pF is needed. For slower switches, a larger capacitor may be necessary.

The PGA's input voltage noise spectral density at a gain of 1000 is only $1.65\,nV/\sqrt{Hz}$ at 1 kHz, only slightly higher than the noise performance of the AD797 alone. The increase is due to the ADG412 noise, and the current noise of the AD797 flowing through R_{ON}.

The accuracy of the PGA is important in determining the overall accuracy of a system. The AD797 has a bias current of 0.9 µA, which, flowing in a 35 Ω R_{ON}, results in an additional offset error of 31.5 µV. Combined with the AD797 offset, the total V_{OS} becomes 71.5 µV (max). Offset temperature drift is affected by the change in bias current and R_{ON}. Calculations show that the total temperature coefficient increases from 0.6 µV/ºC to 1.6 µV/ºC. Note that while these errors are small (and may not matter in the end) it is still important to be aware of them.

In practice, circuit accuracy and gain TC will be determined by the external resistors. Input characteristics such as common mode range and input bias current are determined solely by the AD797. A performance summary is shown below in Figure 2-40.

- R_{ON} adds additional input offset and drift:
  - $\Delta V_{OS} = I_b R_{ON}$ = (0.9μA)(35Ω) = 31.5μV (max)
  - Total V_{OS} = 40μV + 31.5μV = 71.5μV (max)
- Temperature drift due to R_{ON}:
  - At +85°C, ΔV_{OS} = (2μA)(45Ω) = 90μV (max)
- Temperature coefficient total:
  - $\Delta V_{OS} / \Delta T$ = 0.6μV/°C + 1.0μV/°C = 1.6μV/°C (max)
  - Note: 0.6μV/°C is due to the AD797B
- RTI Noise : 1.65nV/$\sqrt{Hz}$ @ 1kHz, G = 1000
- Gain switching time < 1μs, G = 10

Figure 2-40: AD797/ADG412 PGA performance summary

DAC Programmed PGA

Another PGA configuration uses a DAC in the feedback loop of an op amp to adjust the gain under digital control, as shown in Figure 2-41. The digital code of the DAC controls its attenuation with respect to its reference input V_{REF}, acting functionally similar to a potentiometer. Attenuating the feedback signal increases the closed-loop gain.

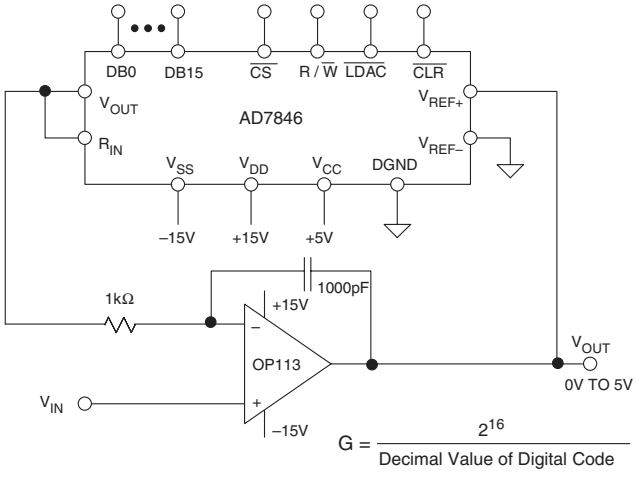


Figure 2-41: Binary gain PGA using a DAC in the feedback path of an op amp

A noninverting PGA of this type requires a multiplying DAC with a voltage mode output. Note that a multiplying DAC is a DAC with a wide reference voltage range, *which includes zero*. For most applications of the PGA, the reference input must be capable of handling bipolar signals. The AD7846 is a 16-bit converter that meets these requirements. In this application, it is used in the standard 2-quadrant multiplying mode.

The OP113 is a low drift, low noise amplifier, but the choice of the amplifier is flexible, and depends on the intended application. The input voltage range depends on the output swing of the AD7846, which is 3 V less than the positive supply, and 4 V above the negative supply. A 1000 pF capacitor is used in the feedback loop for stability.

The gain of the circuit is set by adjusting the digital inputs of the DAC, according to the equation given in Figure 2-41. $D_{0\text{-}15}$ represents the decimal value of the digital code. For example, if all the bits were set high, the gain would be 65,536/65,535 = 1.000015. If the eight least significant bits are set high and the rest low, the gain would be 65,536/255 = 257. The bandwidth of the circuit is a fairly high 4 MHz for a gain of +1. However, this does reduce with gain, and for a gain of 256, the bandwidth is only 600 Hz. If the gain-bandwidth product were constant, the bandwidth in a gain of 256 should be 15.6 kHz; but the internal capacitance of the DAC reduces the bandwidth to 600 Hz.

Performance characteristics of this binary PGA are summarized in Figure 2-42.

- Gain Accuracy:
  - 0.003% (G = +1)
  - 0.1% (G = +256)
- Nonlinearity: 0.001% (G = 1)
- Offset: 100µV
- Noise: 50nV/$\sqrt{\text{Hz}}$
- Bandwidth:
  - 4MHz (G = +1)
  - 600Hz (G = +256)

Figure 2-42: Binary gain PGA performance

The gain accuracy of the circuit is determined by the resolution of the DAC and the gain setting. At a gain of 1, all bits are on, and the accuracy is determined by the DNL specification of the DAC, which is ±1 LSB maximum. Thus, the gain accuracy is equivalent to 1 LSB in a 16-bit system, or 0.003%.

However, as the gain is increased, fewer of the bits are on. For a gain of 256, only bit 8 is turned on. The gain accuracy is still dependent on the ±1 LSB of DNL, but now that is compared to only the lowest eight bits. Thus, the gain accuracy is reduced to 1 LSB in an 8-bit system, or 0.4%. If the gain is increased above 256, the gain accuracy is reduced further. The designer must determine an acceptable level of accuracy. In this particular circuit, the gain was limited to 256.

Differential Input PGAs

There are often applications where a PGA with differential inputs is needed, instead of the single-ended types discussed so far. The AD625 combines an instrumentation amplifier topology similar to the AD620 with external gain switching capabilities to accomplish 12-bit gain accuracy (see Reference 3). An external switch is needed to switch between different gain settings, but its on resistance does not significantly affect the gain accuracy due to the unique design of the AD625.

The circuit in Figure 2-43 uses an ADG409 CMOS switch to switch the connections to an external gain-setting resistor network. In the example shown, resistors were chosen for gains of 1, 4, 16, and 64. Other features of the AD625 are 0.001% nonlinearity, wide bandwidth, and very low input noise.

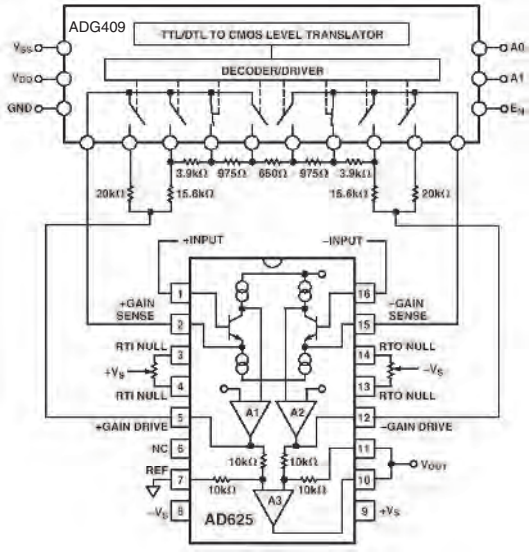


Figure 2-43: A software-programmable gain amplifier

The AD625 is uniquely designed so that the on resistance of the switches does not introduce significant error in the circuit. This can be understood by considering the simplified AD625 circuit shown Figure 2-44. The voltages shown are for an input of +1 mV on +IN and 0 V on –IN. The gain is set to 64 with R_G = 635 Ω and the two resistors, R_F = 20 kΩ.

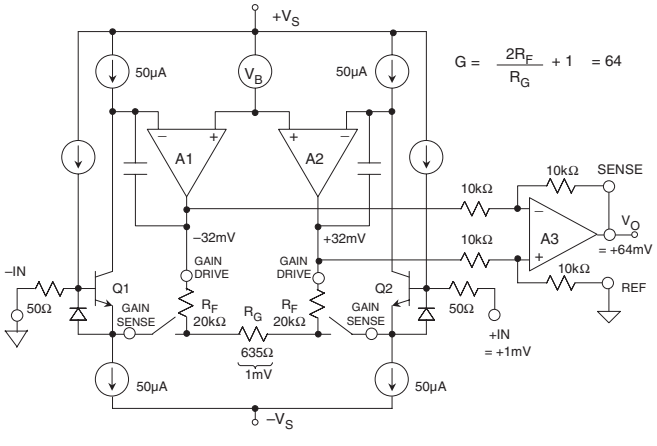


Figure 2-44: AD625 details showing external switches and gain-setting resistors for R_G = 635 Ω, +IN = 1 mV, –IN = 0 V

Since transistors Q1 and Q2 have 50 µA current sources in both their emitters and their collectors, negative feedback around A1 and A2, respectively, will ensure that no net current flows through either *gain sense* pin into either emitter. Since no current flows in the gain sense pins, no current flows in the gain setting switches, and their R_{ON} does not affect either gain or offset. In real life there will be minor mismatches, but the errors are well under the 12-bit level.

The differential gain between the inputs and the A1-A2 outputs is $2R_F/R_G + 1$. The unity-gain difference amplifier and matched resistors removes CM voltage, and drives the output.

Noninverting PGA circuits using an op amp are easily adaptable to single supply operation, but when differential inputs are desired, a single-supply in amp such as the AD623, AD627, or the AMP04 should be used. The AMP04 is used with an external CMOS switch in the single supply in amp PGA shown in Figure 2-45.

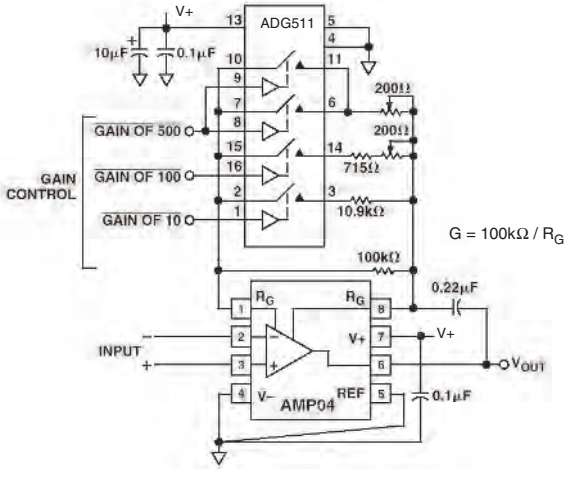


Figure 2-45: Single supply instrumentation PGA using the AMP04 in amp and the ADG511 switch

This circuit has selectable gains of 1, 10, 100, and 500, which are controlled by an ADG511. The ADG511 was chosen as a single supply switch with a low R_{ON} of 45 Ω. A disadvantage of this circuit is that the gain of this circuit is dependent on the RON of the switches. Trimming is required at the higher gains to achieve accuracy. At a gain of 500, two switches are used in parallel, but their resistance causes a 10% gain error in the absence of adjustment.

ADC with Onboard PGA

Certain ADCs (such as the AD77ss measurement series) have built-in PGAs and other conditioning circuitry. Circuit design with these devices is much easier, because an external PGA and its control logic are not needed. Furthermore, all the errors of the PGA are included in the specifications of the ADC, making error calculations simple.

The PGA gain is controlled over the common ADC serial interface, and the gain setting is factored into the conversion, saving additional calculations to determine input voltage.

This combination of ADC and PGA is very powerful and enables the realization of a highly accurate system, with a minimum of circuit design. As an example, Figure 2-46 shows a simplified diagram of the AD7730 sigma-delta measurement ADC which is optimized for digitizing low voltage bridge outputs directly (as low as 10 mV full scale) to greater than 16 bits noise free code resolution, without the need for external signal conditioning circuits.

Additional information and background reading on PGAs can be found in References 4 and 5.

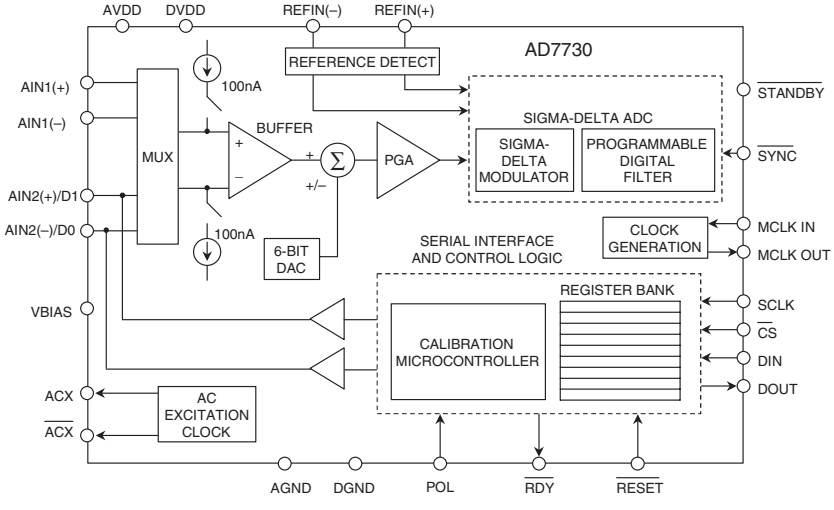


Figure 2-46: AD7730 sigma-delta measurement ADC with on-chip PGA

References: Programmable Gain Amplifiers

1. John Krehbiel, "Monolithic Software Programmable-Gain Amplifier," **Analog Dialogue**, Vol. 21, No. 2, 1987, pp. 12–13.
2. Data sheet for **AD526 Software Programmable Gain Amplifier**, www.analog.com.
3. Data sheet for **AD625 Programmable Gain Instrumentation Amplifier**, www.analog.com.
4. Chapters 2, 3, 8, Walt Kester, Editor, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, 1999, ISBN: 0-916550-20-6.
5. Chapter 2, Walt Kester, Editor, **Linear Design Seminar**, Analog Devices, 1995, ISBN: 0-916550-15-X.

SECTION 2-3

Isolation Amplifiers

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Analog Isolation Techniques

There are many applications where it is desirable, or even essential, for a sensor to have no direct ("galvanic") electrical connection with the system to which it is supplying data. This might be in order to avoid the possibility of dangerous voltages or currents from one half of the system doing damage in the other, or to break an intractable ground loop. Such a system is said to be "isolated," and the arrangement that passes a signal without galvanic connections is known as an *isolation barrier*.

The protection of an isolation barrier works in both directions, and may be needed in either, or even in both. The obvious application is where a sensor may accidentally encounter high voltages, and the system it is driving must be protected. Or a sensor may need to be isolated from accidental high voltages arising downstream in order to protect its environment. Examples include the need to prevent the ignition of explosive gases by sparks at sensors and the protection from electric shock of patients whose ECG, EEG, or EMG is being monitored. The ECG case is interesting, as protection may be required in *both* directions: the patient must be protected from accidental electric shock, but if the patient's heart should stop, the ECG machine must be protected from the very high voltages (>7.5 kV) applied to the patient by the defibrillator that will be used to attempt to restart it. A summary of applications for isolation amplifiers (both analog and digital) is shown in Figure 2-47.

- Sensor is at a High Potential Relative to Other Circuitry (or may become so under Fault Conditions)
- Sensor May Not Carry Dangerous Voltages, Irrespective of Faults in Other Circuitry (e.g. Patient Monitoring and Intrinsically Safe Equipment for use with Explosive Gases)
- To Break Ground Loops

Figure 2-47: Applications for isolation amplifiers

Just as interference, or *unwanted* information, may be coupled by electric or magnetic fields, or by electromagnetic radiation, these phenomena may be used for the transmission of *wanted* information in the design of isolated systems.

The most common isolation amplifiers use *transformers*, which exploit magnetic fields, and another common type uses small high voltage capacitors, exploiting electric fields. *Optoisolators*, which consist of an LED and a photocell, provide isolation by using light, a form of electromagnetic radiation. Different isolators have differing performance: some are sufficiently linear to pass high accuracy analog signals across an isolation barrier. With others, the signal may need to be converted to digital form before transmission for accuracy is to be maintained (note this is a common V/F converter application).

Transformers are capable of analog accuracy of 12 to 16 bits and bandwidths up to several hundred kHz; their maximum voltage rating rarely exceeds 10 kV, and is often much lower. *Capacitively-coupled* isolation amplifiers have lower accuracy, perhaps 12 bits maximum, lower bandwidth, and lower voltage ratings—but they are low cost. Optical isolators are fast and cheap, and can be made with very high voltage ratings (4 kV – 7 kV is one of the more common ratings), but they have poor analog domain linearity and are not usually suitable for direct coupling of precision analog signals.

Linearity and isolation voltage are not the only issues to be considered in the choice of isolation systems. Operating power is of course, essential. Both the input and the output circuitry must be powered and, unless there is a battery on the isolated side of the isolation barrier (which is possible, but rarely convenient), some form of isolated power must be provided. Systems using transformer isolation can easily use a transformer (either the signal transformer or another one) to provide isolated power. It is, however, impractical to transmit useful amounts of power by capacitive or optical means. Systems using these forms of isolation must make other arrangements to obtain isolated power supplies—this is a powerful consideration in favor of choosing transformer-isolated isolation amplifiers: they almost invariably include an isolated power supply.

The isolation amplifier has an input circuit that is galvanically isolated from the power supply and the output circuit. In addition, there is minimal capacitance between the input and the rest of the device. Therefore, there is no possibility for dc current flow and minimum ac coupling. Isolation amplifiers are intended for applications requiring safe, accurate measurement of low frequency voltage or current (up to about 100 kHz) in the presence of high common-mode voltage (to thousands of volts) with high common-mode rejection. They are also useful for line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measurements, where dc and line-frequency leakage must be maintained at levels well below certain mandated minimums. Principal applications are in electrical environments of the kind associated with medical equipment, conventional and nuclear power plants, automatic test equipment, and industrial process control systems.

AD210 Three-Port Isolator

In a basic two-port form of isolator, the output and power circuits are not isolated from one another. A *three-port isolator* (input, power, output) is shown in Figure 2-48. Note that in this diagram, the input circuits, output circuits, and power source are all isolated from one another. This figure represents the circuit architecture of a self-contained isolator, the AD210 (see References 1 and 2).

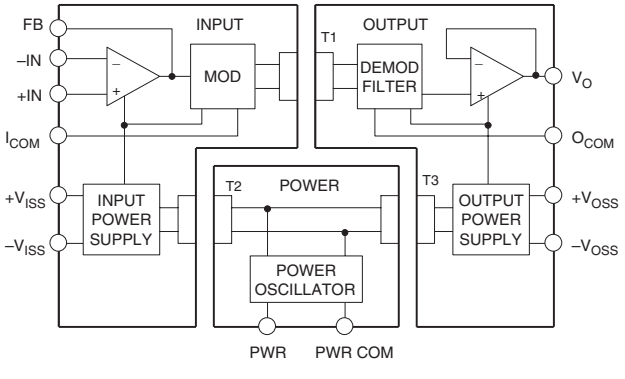


Figure 2-48: AD210 three-port isolation amplifier

An isolator of this type requires power from a two-terminal dc power supply (PWR, PWR COM). An internal oscillator (50 kHz) converts the dc power to ac, which is transformer-coupled to the shielded input section, then converted to dc for the input stage and the auxiliary power output.

The ac carrier is also modulated by the input stage amplifier output, transformer-coupled to the output stage, demodulated by a phase-sensitive demodulator (using the carrier as the reference), filtered, and buffered using isolated dc power derived from the carrier. The AD210 allows the user to select gains from 1 to 100, using external resistors with the input section op amp. Bandwidth is 20 kHz, and voltage isolation is 2500 V rms (continuous) and ±3500 V peak (continuous).

The AD210 is a three-port isolation amplifier, thus the power circuitry is isolated from both the input and the output stages and may therefore be connected to either (or to neither), without change in functionality. It uses transformer isolation to achieve 3500 V isolation with 12-bit accuracy.

Key specifications for the AD210 are summarized in Figure 2-49.

- Transformer Coupled
- High Common-Mode Voltage Isolation:
  - 2500V RMS Continuous
  - ±3500V Peak Continuous
- Wide Bandwidth: 20kHz (Full Power)
- 0.012% Maximum Linearity Error
- Input Amplifier: Gain 1 to 100
- Isolated Input and Output Power Supplies, ±15V, ±5mA

Figure 2-49: AD210 isolation amplifier key specifications

Motor Control Isolation Amplifier

A typical isolation amplifier application using the AD210 is shown in Figure 2-50. The AD210 is used with an AD620 instrumentation amplifier in a current-sensing system for motor control. The input of the AD210, being isolated, can be directly connected to a 110 V or 230 V power line without protection being necessary. The input section's isolated ±15 V powers the AD620, which senses the voltage drop in a small value current sensing resistor. The AD210 input stage op amp is simply connected as a unity-gain follower, which minimizes its error contribution. The 110 V or 230 V rms common-mode voltage is ignored by this isolated system.

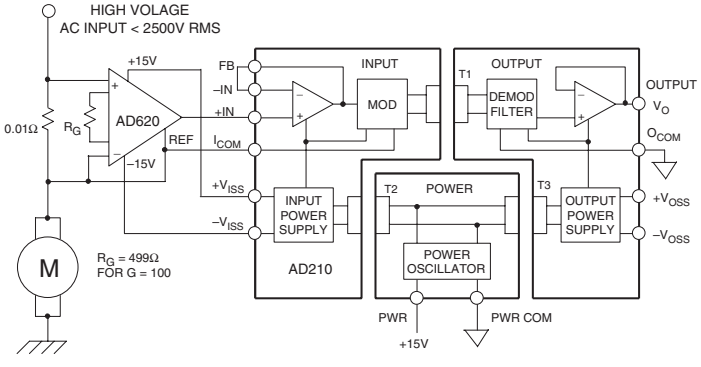


Figure 2-50: Motor control current sensing

Within this system the AD620 preamp is used as the system scaling control point, and will produce and output voltage proportional to motor current, as scaled by the sensing resistor value and gain as set by the AD620's R_G. The AD620 also improves overall system accuracy, as the AD210 V_{OS} is 15 mV, versus the AD620's 30 μV (with less drift also). Note that if higher dc offset and drift are acceptable, the AD620 may be omitted and the AD210 connected at a gain of 100.

Optional Noise Reduction Post Filter

Due to the nature of this type of carrier-operated isolation system, there will be certain operating situations where some residual ac carrier component will be superimposed upon the recovered output dc signal. When this occurs, a low impedance passive RC filter section following the output stage may be used (if the following stage has a high input impedance, i.e., nonloading to this filter). Note that will be the case for many high input impedance sampling ADCs, which appear essentially as a small capacitor. A 150 Ω resistance and 1 nF capacitor will provide a corner frequency of about 1 kHz. Note also that the capacitor should be a film type for low errors, such as polypropylene.

AD215 Two-Port Isolator

The AD215 is a high speed, two-port isolation amplifier, designed to isolate and amplify wide bandwidth analog signals (see Reference 3). The innovative circuit and transformer design of the AD215 ensures wideband dynamic characteristics, while preserving dc performance specifications. An AD215 block diagram is shown in Figure 2-51.

The AD215 provides complete galvanic isolation between the input and output of the device, which also includes the user-available front-end isolated bipolar power supply. The functionally complete design,

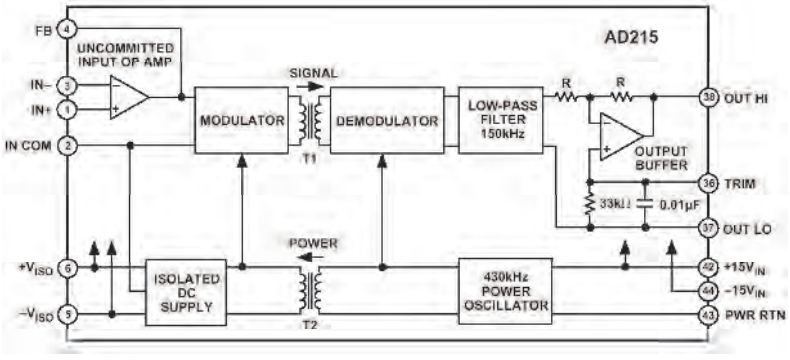


Figure 2-51: AD215 120kHz low distortion two-port isolation amplifier

powered by a ±15 V dc supply on the output side, eliminates the need for a user supplied isolated dc/dc converter. This permits the designer to minimize circuit overhead and reduce overall system design complexity and component costs.

The design of the AD215 emphasizes maximum flexibility and ease of use in a broad range of applications where fast analog signals must be measured under high common-mode voltage (CMV) conditions.

The AD215 has a ±10 V input/output range, a specified gain range of 1 V/V to 10 V/V, a buffered output with offset trim and a user-available isolated front end power supply which produces ±15 V dc at ±10 mA. The key specifications of the AD215 are summarized in Figure 2-52.

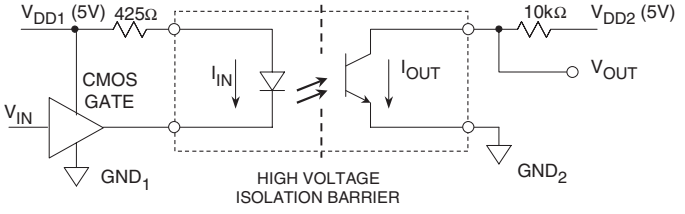
- Isolation voltage: 1500V rms
- Full power bandwidth: 120kHz
- Slew rate: 6V/µs
- Harmonic distortion: –80dB @ 1kHz
- 0.005% maximum linearity error
- Gain range: 1 to 10
- Isolated input power supply: ±15V @ ±10mA

Figure 2-52: AD215 isolation amplifier key specifications

Digital Isolation Techniques

Analog isolation amplifiers find many applications where a high isolation is required, such as in medical instrumentation. Digital isolation techniques provide similar galvanic isolation, and are a reliable method of transmitting digital signals without ground noise.

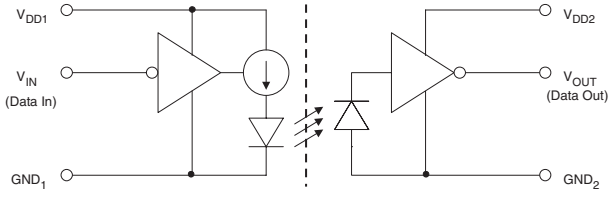
Optocouplers (also called optoisolators) are useful and available in a wide variety of styles and packages. A typical optocoupler based on an LED and a phototransitor is shown in Figure 2-53. A current of approximately 10 mA drives an LED transmitter, with light output is received by a phototransistor. The light produced by the LED saturates the phototransistor. Input/output isolation of 5000 V rms to 7000 V rms is common. Although fine for digital signals, optocouplers are too nonlinear for most analog applications. Also, since the phototransistor is being saturated, response times can range from 10 µs to 20 µs in slower devices, limiting high speed applications.



- Uses Light for Transmission over a High Voltage Barrier
- The LED is the Transmitter, and the Phototransistor is the Receiver
- High Voltage Isolation: 5000V to 7000V rms
- Nonlinear — Best for Digital or Frequency Information
- Rise and Fall times can be 10µs to 20µs in Slower Devices
- Example: Siemens ILQ-1 Quad (www.siemens.com)

Figure 2-53: Digital isolation using LED/phototransistor optocouplers

A much faster optocoupler architecture is shown in Figure 2-54, and is based on an LED and a photodiode. The LED is again driven with a current of approximately 10 mA.



- 5V Supply Voltage
- 2500V rms I/O Withstand Voltage
- Logic Signal Frequency: 12.5MHz Maximum
- 25MBd Maximum Data Rate
- 40ns Maximum Propagation Delay
- 9ns Typical Rise/Fall Time
- Example: Agilent HCPL-7720
- (www.semiconductor.agilent.com)

Figure 2-54: Digital isolation using LED/photodiode optocouplers

This produces a light output sufficient to generate enough current in the receiving photodiode to develop a valid high logic level at the output of the transimpedance amplifier. Speed can vary widely between opto-couplers, and the fastest ones have propagation delays of 20 ns typical, and 40 ns maximum, and can handle data rates up to 25 MBd for NRZ data. This corresponds to a maximum square wave operating frequency of 12.5 MHz, and a minimum allowable passable pulse width of 40 ns.

AD260/AD261 High Speed Logic Isolators

The AD260/AD261 family of digital isolators operates on a principle of transformer-coupled isolation (see Reference 4). They provide isolation for five digital control signals to/from high speed DSPs, microcontrollers, or microprocessors. The AD260 also has a 1.5 W transformer for a 3.5 kV rms isolated external dc/dc power supply circuit.

Each line of the AD260 can handle digital signals up to 20 MHz (40 MBd) with a propagation delay of only 14 ns which allows for extremely fast data transmission. Output waveform symmetry is maintained to within ±1ns of the input so the AD260 can be used to accurately isolate time-based pulsewidth modulator (PWM) signals.

A simplified schematic of one channel of the AD260/AD261 is shown in Figure 2-55. The data input is passed through a Schmitt trigger circuit, through a latch, and a special transmitter circuit which differentiates the edges of the digital input signal and drives the primary winding of a proprietary transformer with a "set-high/set-low" signal. The secondary of the isolation transformer drives a receiver with the same "set-hi/set-low" data, which regenerates the original logic waveform. An internal circuit operating in the background interrogates all inputs about every 5 µs, and in the absence of logic transitions, sends appropriate "set-hi/set-low" data across the interface. Recovery time from a fault condition or at power-up is thus between 5 µs and 10 µs.

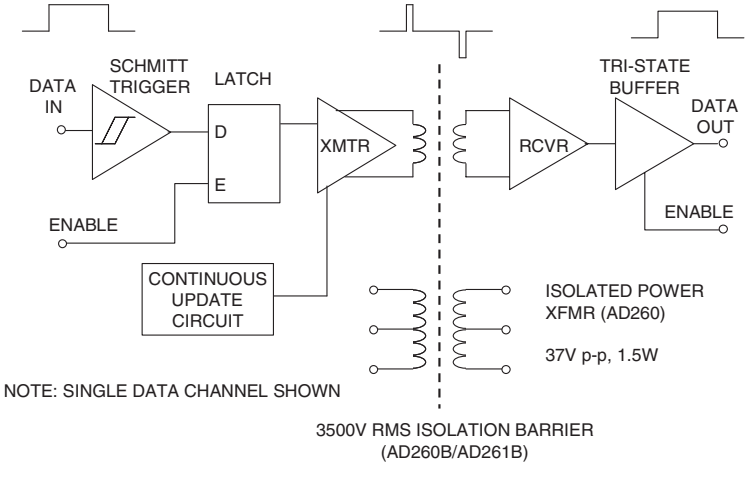


Figure 2-55: AD260/AD261 digital isolators

The power transformer (available on the AD260) is designed to operate between 150 kHz and 250 kHz and will easily deliver more than 1 W of isolated power when driven push-pull (5 V) on the transmitter side. Different transformer taps, rectifier and regulator schemes will provide combinations of ±5 V, 15 V, 24 V, or even 30 V or higher.

The transformer output voltage when driven with a low voltage-drop drive will be 37 V p-p across the entire secondary with a 5 V push-pull drive. Figure 2-56 summarizes the key specifications of the AD260/261 series.

- Isolation Test Voltage to 3500V rms (AD260B/AD261B)
- Five Isolated Digital Lines Available in six Input/Output Configurations
- Logic Signal Frequency: 20MHz Max.
- Data Rate: 40MBd Max.
- Isolated Power Transformer: 37V p-p, 1.5W (AD260)
- Waveform Edge Transmission Symmetry: ±1ns
- Propagation Delay: 14ns
- Rise and Fall Times < 5ns

Figure 2-56: AD260/AD261 digital isolator key specifications

The availability of low cost digital isolators such as those previously discussed solves most system isolation problems in data acquisition systems as shown in Figure 2-57. In the upper example, digitizing the signal first, then using digital isolation eliminates the problem of analog isolation amplifiers. While digital isolation can be used with parallel output ADCs provided the bandwidth of the isolator is sufficient, it is more practical with ADCs that have *serial* outputs. This minimizes cost and component count. A 3-wire interface (data, serial clock, framing clock) is all that is required in these cases.

An alternative (lower example) is to use a voltage-to-frequency converter (VFC) as a transmitter and a frequency-to-voltage converter (FVC) as a receiver. In this case, only one digital isolator is required.

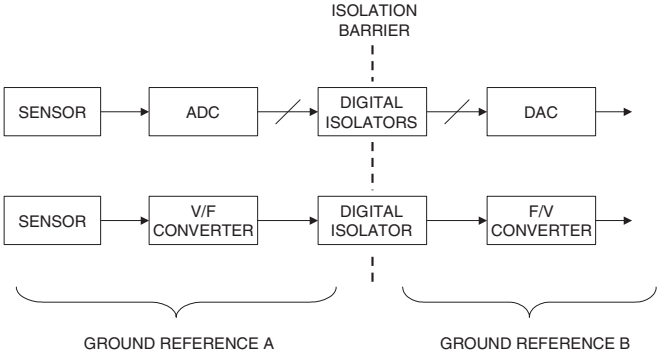


Figure 2-57: Practical application of digital isolation in data acquisition systems

References: Isolation Amplifiers

1. James Conant, "Precision Wideband Three-Port Isolation Amplifier," **Analog Dialogue**, Vol. 20, No. 2, 1986, p. 14.
2. Data sheet for **AD210 Precision, Wide Bandwidth 3-Port Isolation Amplifier**, www.analog.com.
3. Data sheet for **AD215 120 kHz Bandwidth, Low Distortion, Isolation Amplifier**, www.analog.com.
4. Data sheets for **AD260 and AD261 High Speed Logic Isolators**, www.analog.com.
5. Chapters 2, 3, 8, Walt Kester, Editor, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, 1999, ISBN: 0-916550-20-6.
6. Chapter 2, Walt Kester, Editor, **Linear Design Seminar**, Analog Devices, 1995, ISBN: 0-916550-15-X.
7. Chapter 10, Walt Kester, Editor, **Mixed-Signal and DSP Design Techniques**, Analog Devices, 2000, ISBN: 0-916550-23-0.