vation as far as the end product of most hi-fi systems most of the time is concerned. If it were not so, we could more frequently enjoy artistic subtleties and differences without the intrusion of technology. I also agree with him that there are many amplifiers around that fall short of the ideal performance, as judged subjectively. But I must end by repeating that I am in no doubt at all that the best amplifiers, unlike some other links in the overall chain, easily meet the requirements for subjectively perfect sound reproduction. Nevertheless, designers, including myself, will continue to bring out new designs, for there are so many reasons for doing this other than basic sound quality – power ratings, reliability, production economy, versatility of functions, etc.

Peter J. Baxandall
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Worcs

*As some readers will have spotted, the editor inadvertently left out two resistors, one in each input to the monitoring system.

LOGIC DESIGN

THERE is an important principle that was not brought up in the fourth article of the "Logic design" series by Holdsworth and Zissos (May 1977 issue).

The realization of the circuit for the alarm bell output in Fig. 14 (f) is more complex than need be. Two of the cells in the merged state diagram Fig. 14 (d) indicate unstable states in which the circuit cannot remain. Therefore the outputs in these two states do not matter and the b output can be high. This simplifies the circuit from:

$$b = \bar{A}f\bar{a} + A\bar{f}\bar{a}$$

to

$$b = \bar{A}f + A\bar{f}$$

In this example there is not a great saving in hardware; two 2-input Nand gates are used instead of two 3-input Nand gates, but in more complex problems the savings could be significant.

One must take care in the use of this simplification as there is a delay in the transition from the unstable to the stable state. This results in an output spike of short duration which could affect a following circuit. This spike is far too short to operate the alarm bell in the illustrated problem.

A. R. Harris
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Professor Zissos and Mr Holdsworth reply:
We agree with Mr Harris that a further reduction of the bell equation is possible by using the circuit conditions, $A=0$, $f=1$ and $a=1$ and $A=1$, $f=0$ and $a=1$ for simplification purposes. The bell equation then reduced to

$$b = \bar{A}f + A\bar{f}$$

However, in this circuit a spike will not occur as a consequence of using this simplification and it is essential for the bell to ring particularly when a fault occurs to draw the attention of the operator to its occurrence.

When the transition S_{01} to S_{23} is made (Fig 14(d) the input signals required are $f=1$ and $a=1$. By virtue of the design specification these signals must occur in the sequence $f=1$ followed by $a=1$. Initially the circuit will take up the condition $A=0$, $f=1$ and $a=0$ and the bell rings as required. The transition then takes place when a becomes 1. During the transition from S_{01} to S_{23} $f=1$ and $a=1$ and $b=0$. When the transition has been completed $A=1$, $f=1$ and $a=1$ and again $b=0$ as required.

Similar conclusions may be drawn regarding the transition from S_{23} to S_{01}.

Perhaps it should be noted that, due to an authors' error, state S_{23} has been marked incorrectly as S_{02} and the bell signal in this state should be $f\bar{a}$.

B. Holdsworth and L. Zissos

Editor's note: The following remarks were unfortunately omitted from the authors' reply to Mr R. M. Hutton's letter on minimisation in logic design in the December 1977 issue. Apologies to the correspondents.

We are not at all sure what is debatable about Example L, nor can we agree with your statement that in this example we have demonstrated the vulnerability of our method. We are aware that a change of state assignment will lead to a different solution. All other known methods of logic design are vulnerable in precisely the same way and it is up to the logic designer to examine all possible solutions if he wishes to find the simplest solution. This is perfectly easy to do in the case of a four-state state diagram but becomes increasingly more difficult as the number of state variables increases. If minimal solutions are not vital it is probably more economically sound to reduce the design time.

With respect to the relative advantages of mapping techniques in comparison with algebraic methods this is really a question of which method the designer is familiar with. Certainly students we have taught do not find algebraic methods any more difficult to use than mapping techniques and vice versa. If you refer back to article 1 on Boolean algebra you will find that there are a very limited number of rules to remember. We would not press a claim either way with respect to this point and would suggest that the designer should use the method he is most familiar with.

B. Holdsworth and L. Zissos

THE DECATRON

READING T. R. Thompson's letter (November 1977 issue) about the 3NF valve "integrated circuit," brought to mind the old "Decatron" tubes, which are still available (if you know where to look). These, of course, are the equivalent of a decade counter-decoder-driver and display all in one! They haven't even done that in semiconductor i.cs to my knowledge.

R. E. Williams
Tilsworth
Beds

Letters commenting on Eric F. Taylor's articles "Distortion in low-noise amplifiers" (August and September 1977) will be published in a later issue.