Letters

Hourly Chime

Regarding Hourly Chime for Digital Clock article in May '85 issue. (a) can I use 1Hz output of 5387 IC (colon display) instead of IC4, and (b) can this circuit be used for alarm? If so, how?

AMARJEET SINGH BAJWA
Kapurthala

□ It may please be pointed out to other readers that pin 2 of 7805 should be connected to ground, otherwise the chime would not work. In the circuit diagram the elements of 7408 (Quad 2 input AND gate) have been drawn as NAND gate. This may lead to confusion. The use of R14 (1.5k) is probably not essential. Though included in the parts list, C5 (0.22μF) has not been shown in the circuit or in the component layout.

In the component layout, collector and emitter of T1 have been wrongly marked. Capacitors C5, C10 and C11 have not been shown in the layout. One of the speaker connections has not been shown properly.

Readers may try the resistors 1k, 2.2k, 3.9k and 8.2k for R16, R17, R18 and R15 respectively. Those who require more volume from the chime may refer to May '84 issue of EFY (p. 11) and use a 1k resistor and SL100 transistor for driving the speaker.

Transistors BC147 have been shown in the circuit and in the parts list. But CIL147, which is probably equivalent, ha been shown in the layout. The readers may use either of them.

J.N. RAY
Calcutta

□ Let me offer some alternatives which I hope will provide useful stimulation to further thinking on this subject.

The sketch below shows the schematics of the ideas, the original circuit of chime can remain as published—except for the wiring of the reset terminals of ICs 4, 5 and 6. For deriving hourly pulses, the decoder suggested by me utilises the fact that in a digital clock the display indicating tens of minutes has segments b and e both off at the display of '5'. One of them or both are high in all other cases. As such at the striking of an hour when the minutes change from '59' to '00', the 'b OR e' becomes high and this can supply a negative going pulse each hour. For this purpose a simple decoder consisting of two diodes, one transistor, four resistances and a capacitor is suggested, which is self-explanatory.

Now unless one plans to have more than one cycle of 7493 for hour striking chimes, the facility of built-in reset terminals of the various ICs can be utilised for controlling the chiming. The 7493 (IC5) resets when both its reset terminals (pins 2 and 3) are brought to high and will start counting only when one of these is brought to ground.

In the proposed circuit the reset terminal of 7493 (pin 3) is wired in such a way that when the counter reaches the count of (binary) 1111 (i.e. when all the outputs of IC5 are high) pin 3 becomes high, in all other cases it is pulled low by appropriate (low) output and diode. Also, when pin 3 (of IC5) is high, the ICs 4 and 6 are disabled by NAND gates B and C wired as NOT gates by bringing down the terminals numbered 4 of these ICs (4 and 6) to ground. When pin 3 of IC5 is low, the ICs 4 and 6 are enabled and the chime works as in the original circuit, and when the output of IC5 reaches the count of (binary) 1111, pin 3 (of IC5) goes high and the chime stops on account of ICs 4 and 6 becoming disabled by their low going reset terminals, and the input to NAND gate D (wired as NOT gate) becomes low making its output high. This gate D helps in maintaining the output of IC5 as this IC is triggered by falling edge only and a high-going pin 14 of IC5 does not matter. This steady state (i.e. ICs 4 and 6 reset and IC5 parked at count 1111) will be maintained till the next hourly negative going pulse is received at the input of NAND gate A, bringing down to earth the pin no. 2 of IC5 momentarily.

As the (reset) pin no. 3 of IC5 was already high and pin 2 also becomes high (even though momentarily) the IC5 resets to the binary output of '0000'. The chime starts working and once again stops when the output of IC5 reaches the binary count of 1111 waiting for the next hourly pulse to operate it.

The unused input terminal of NAND gate C is to be used for suppressing chiming during displaying of alarm, seconds, sleep etc. The detailed circuit cannot be included here for shortage of space.

P.V. SINGH
Bhilai

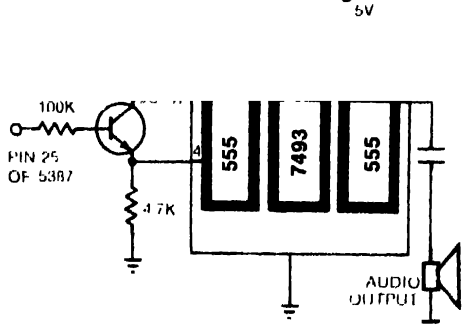
The author, Mr A. Kadarkari, replies:

Regarding Mr Bajwa's letter, 1Hz output of the clock IC 5387 cannot be used as such. Proper voltage and current translators are required. The requirements are listed below:

MOS IC5387 (Vcc 12V)		TTL IC7493	
V_{OH}	9V	$V_{IH} \leq$	5.5V
I_{OH}	10μA	I_{IH}	80μA
V_{OL}	1V$_{max}$	$V_{IL} \leq$	0.8V
I_{OL}	-24mA	I_{IL}	-1.6mA

So inbetween these two ICs a 9V to 5.5V translator cum buffer (MOS to TTL interface) should be provided to meet the 7493 clock input requirements. Moreover, in the published circuit, to get the flexibility of changing the tone rate according to one's taste, a separate oscillator was used.

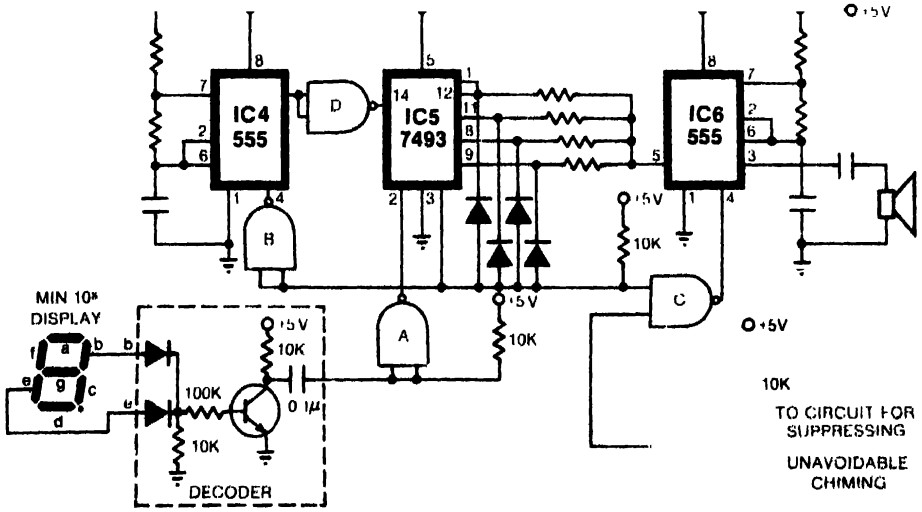
My circuit will give sixteen different tones for every hour. It can be used as a pleasing alarm if properly interfaced with the alarm output pin (25) of 5387. The circuit given below may be used:



The mistakes pointed out by Mr J.N. Ray—like pin 2 of 7805 not being grounded, 7408 drawn as NAND gate etc.—are all correct and may please be corrected.

The resistance (pull up resistance) R14 (1.5k) is essentially required. Otherwise, the driver transistor SL100 won't get saturated. This in turn won't supply adequate power to the chime circuit to operate.

I appreciate Mr P.V. Singh's interesting idea. This is one of the possible ways to get the decoded pulse for the hourly strobing signal. It may work. The readers may construct, test and make use of this.



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