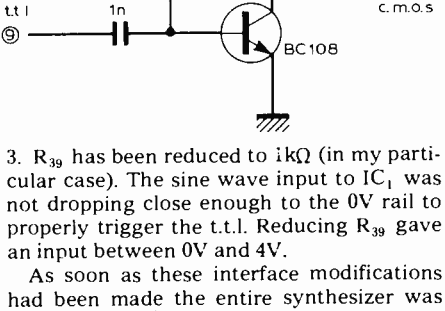
F.M. TRANSCEIVER SYNTHESIZER

I have recently completed construction of the synthesizer portion of T. D. Forrester's f.m. transceiver (November and December 1977) which works very well now that the following modifications have been incorporated.

1. The v.c.o. was found to oscillate at a minimum frequency of 30MHz (i.e. 0V on D_{17}, L_1 slug fully in) with 10 turns on L_1. Turns have been increased to 20 and D_{18} removed.

2. The 4059 was not being clocked by the 74LS74, even at 15V. Experiment showed that the 4059 required a pulse input of at least 70% V_{cc} before it would clock, which could not be directly supplied by the t.t.l. The accompanying buffer circuit was therefore introduced between the t.t.l. output and the 4059 input.



3. R_{39} has been reduced to 1kΩ (in my particular case). The sine wave input to IC_1 was not dropping close enough to the 0V rail to properly trigger the t.t.l. Reducing R_{39} gave an input between 0V and 4V.

As soon as these interface modifications had been made the entire synthesizer was powered from a stabilized 12V supply and the v.c.o. locked to around the programmed frequency. A trimmer was then inserted in one leg of the crystal to set the v.c.o. to exactly the required frequency.

I hope these suggestions may help others constructing this project and would be interested to hear of other modifications. Also, thanks to G4DPM who assisted with the above work.

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