Notes on CobraNet Clocking Modes

Steve Gray, Cirrus Logic, Inc.

CobraNet is used in most cases with its default audio clocking mode (0x00) allowing automatic synchronization of audio clocks network wide. However, the clocking circuitry of a CobraNet device can be configured to operate in a number of ways which are specified by the values written to the *syncConductorClock* and *syncPerformerClock* Management Interface variables. These two MI variables are used to *independently* set the clocking mode of an interface depending on whether it is operating as a Conductor or a Performer and can be set using SNMP or via the Host Management Interface (HMI).

Please see the CobraNet Programmer's Reference Manual and the CobraNet Hardware User's manual for more information on the variables, SNMP and the HMI interface.

The core clock circuitry of a CobraNet interface is depicted below in Fig.1. Note that not all inputs and outputs to the clock module are used at the same time in all modes. Operation of the circuitry, and activity on each path, are dependant on the clock mode selected.
These different clocking modes can be used in many ways depending on the requirements of a particular application. Common use of the different modes is described in this document.

Important concepts regarding CobraNet Clocking:
All devices in a CobraNet network must operate within the same clock domain. It is therefore a requirement that, regardless of clock mode used, all audio clocks on the network should be derived from the same master clock in order to insure that they remain synchronized. This is accomplished automatically when using the default clock mode 0x00 and when any digital devices attached to the CobraNet interface receive their audio clocks from the CobraNet interface.

- Any device that does not derive its audio clock from the CobraNet interface must be connected to the CobraNet interface using a sample rate converter.
- Any CobraNet interface that uses one of the external clocking modes must use external clocks that are synchronous with the network audio clock.

The basic clock circuit topology within a CobraNet interface is as appears in Figs.1 and 2. Not all paths are used by all modes at the same time. The user-available external clock connections are REFCLK, MCLK_IN, MCLK_OUT, FS1 and SCLK. The other connections are internal to the interface and utilized by the interface's firmware in response to the particular mode in use. The five audio clock modes are:

- 0x00 – Internal (normal default mode)
- 0x10 - Internal with External Sample Synchronization
- 0x01 - External Word Clock
- 0x04 - External Master Clock
- 0x14 - External Master Clock with External Sample Synchronization

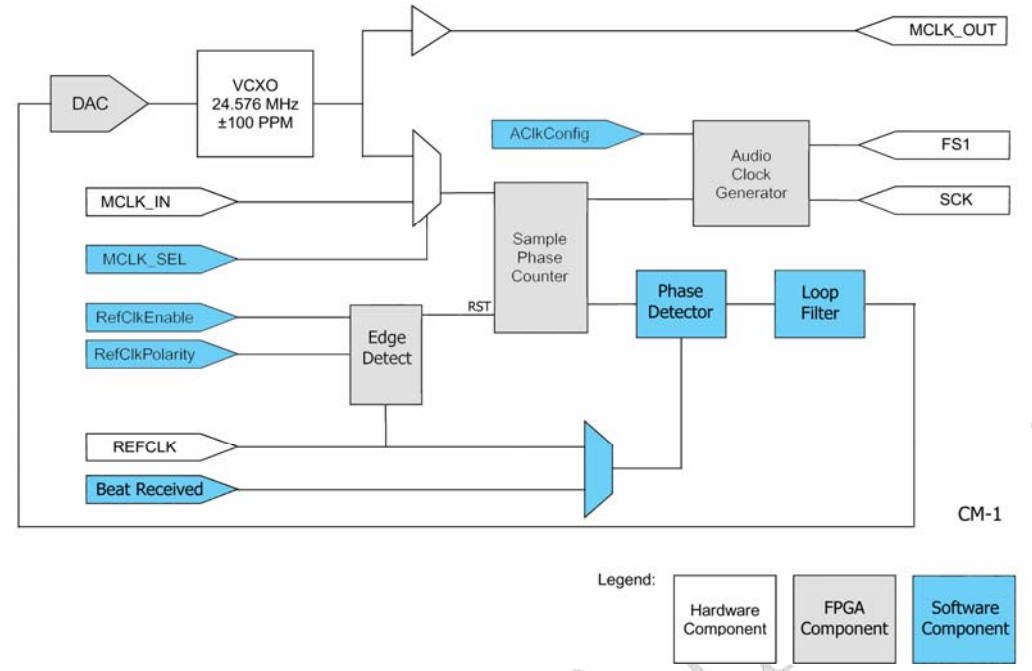

Fig. 1 - CobraNet Clock Circuit for CM-1 Module

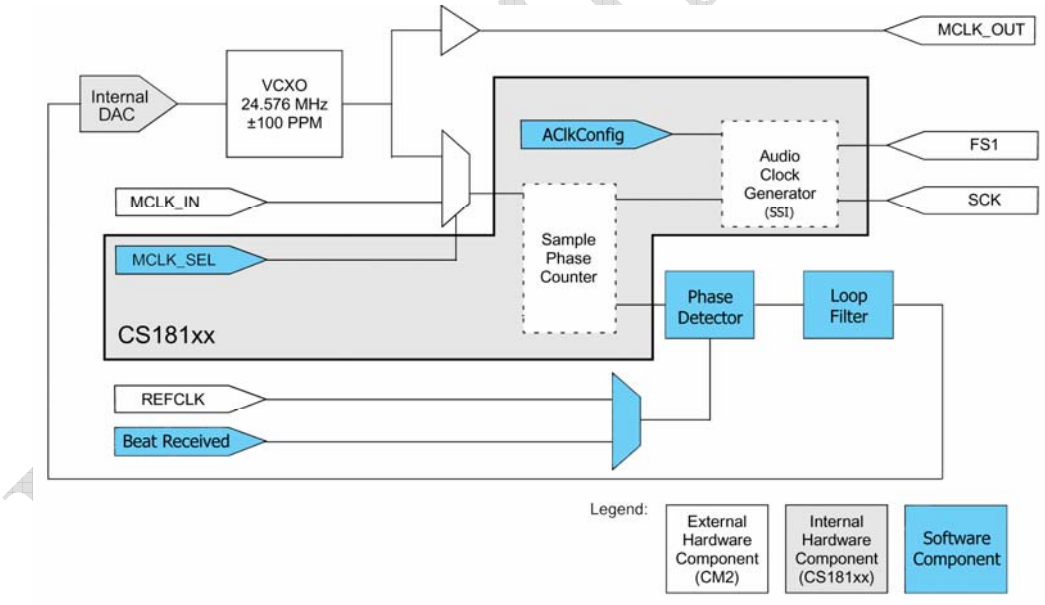

Fig. 2 - CobraNet Clock Circuit for CM-2 Module and Semiconductors

0x00 Mode - Internal Mode

This is the default clock mode of a CobraNet interface.

As Conductor:

The master audio clock (MCLK) is generated by the VXCO parked at its center frequency. Word clock (FS1) and bit clock (SCLK) are derived directly from MCLK.

As Performer:

The master audio clock (MCLK) is generated by the VXCO which receives frequency adjustments from the beat packets received from the Conductor node over the network interface, insuring that the Performer's clock is in sync with the Conductor. Word clock (FS1) and bit clock (SCLK) are derived from MCLK

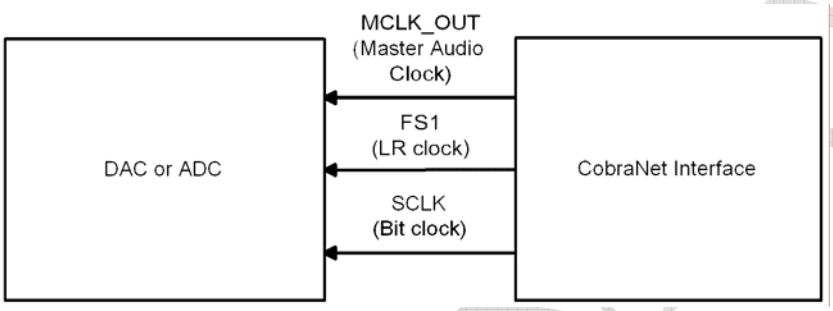

Fig. 3 - 0x00 Mode Typical connections

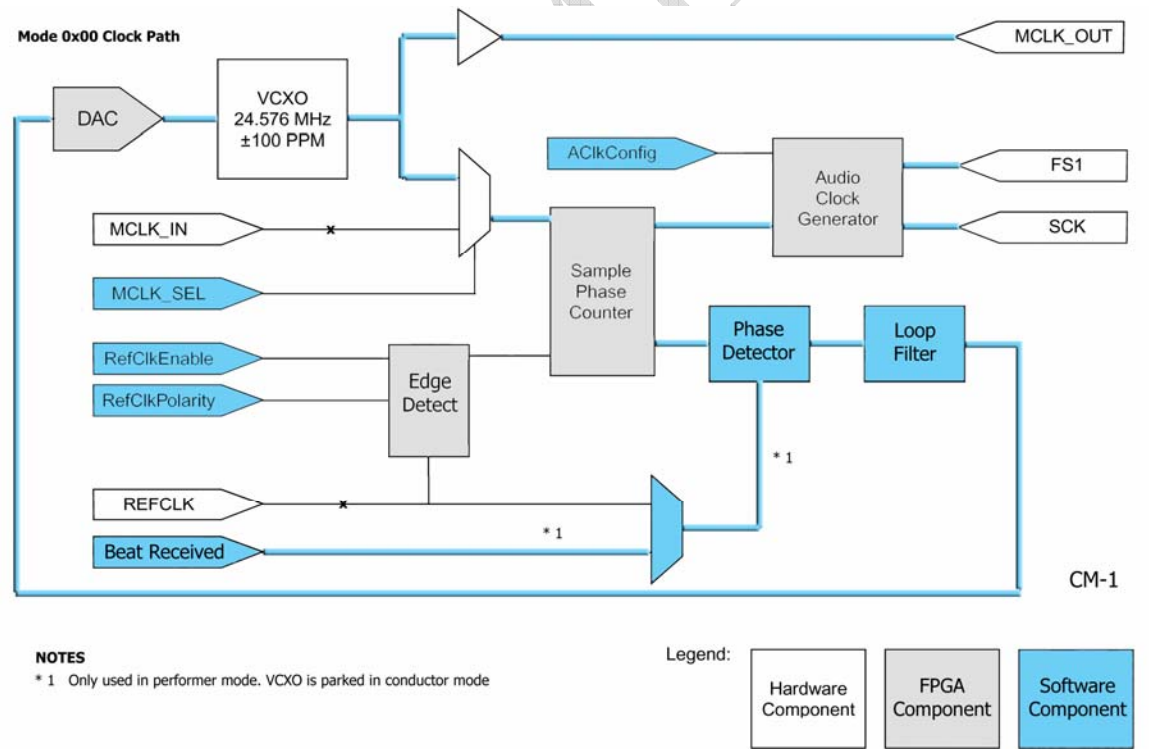

Fig. 4 - Clock circuit as used by Mode 0x00 with CM-1 module

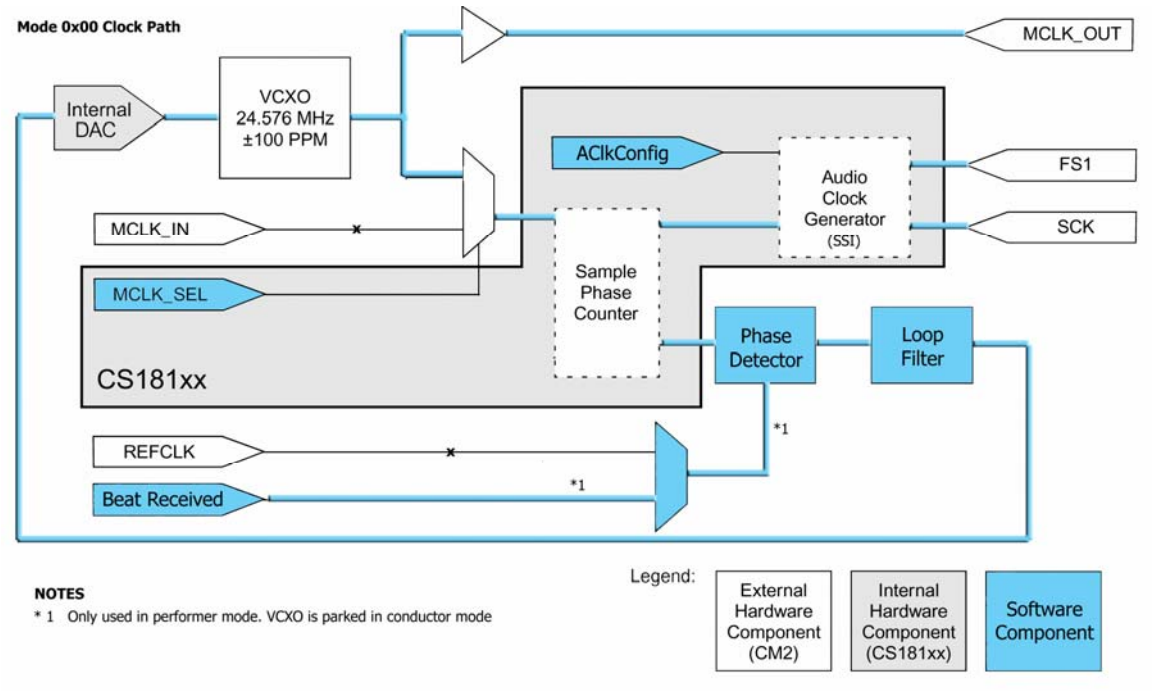

Fig. 5 - Clock circuit as used by Mode 0x00 with CM-2 and semiconductors

0x10 Mode - Internal Mode with External Sample Synchronization

**** NOTE:** This mode will not work properly with CM-2 modules or semiconductor based designs due to the absence of the edge detect circuit in the semiconductor

This mode is similar to Internal Mode (0x00) but allows synchronization of the derived SCLK and FS1 signals with external clock circuits. It is typically used when it is necessary to synchronize CobraNet clocks with existing external clock circuitry.

As Conductor:

MCLK, FS1 and SCLK are all generated as in 0x00 Mode. But the REFCLK input is used to align the clock edges of the generated MCLK, insuring that the audio clocks generated externally are kept in sync with the CobraNet interface's audio clocks. This mode does not alter the clock frequency and implies that the REFCLK input should be derived from the MCLK_OUT supplied by the CobraNet interface. See Figure 6.

As Performer:

MCLK is generated by the VXCO which receives frequency adjustments from the beat packets received over the network interface as in 0x00 Mode. FS1 and SCLK are derived from MCLK. As above in conductor mode, the REFCLK input is used to insure that the external and CobraNet generated audio clocks are in sync.

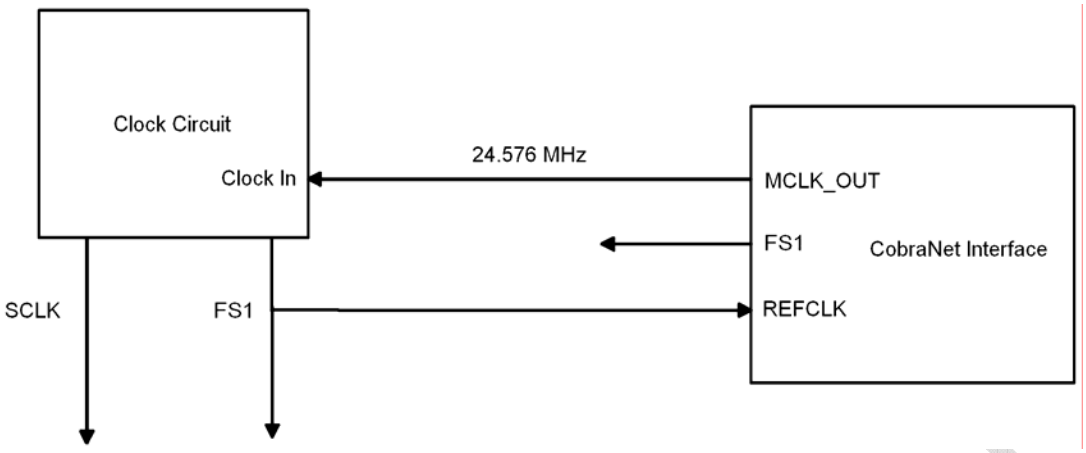

Fig. 6 - 0x10 Mode Typical Connections
Synchronization of CobraNet Clocks with external clock circuitry

0x01 Mode – External Word Clock Mode

This mode allows synchronization of all CobraNet clocks with an externally supplied word clock. The external clock can be any integral division of FS1 from 750Hz to 48 kHz. This is most often used to synchronize a CobraNet network with a house sync signal whereby the Conductor will supply the network clock and operate in this mode with Performer Nodes operating in 0x00 Mode.

As Conductor:

The VCXO generating MCLK is steered to synchronize with REFCLK. FS1 and SCLK are derived from MCLK.

As Performer:

The VCXO generating MCLK is steered to synchronize with REFCLK. FS1 and SCLK are derived from MCLK.

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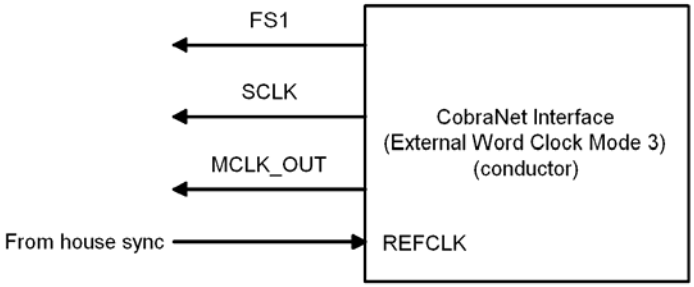

Fig. 7 - 0x01 Mode Typical Connection – External Sync Attached to Conductor.
Used to Provide Synchronized Audio Clocks via Ethernet

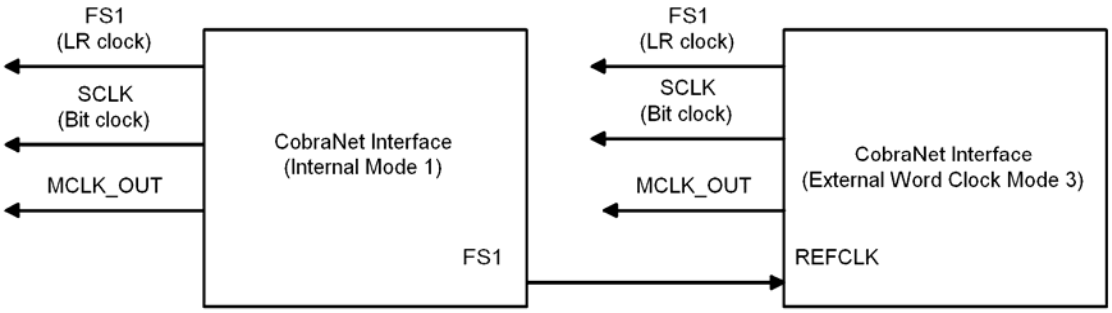

Fig. 10 – 0x01 Mode Typical Connection – External Sync used to synchronize clocks between multiple CobraNet Interfaces

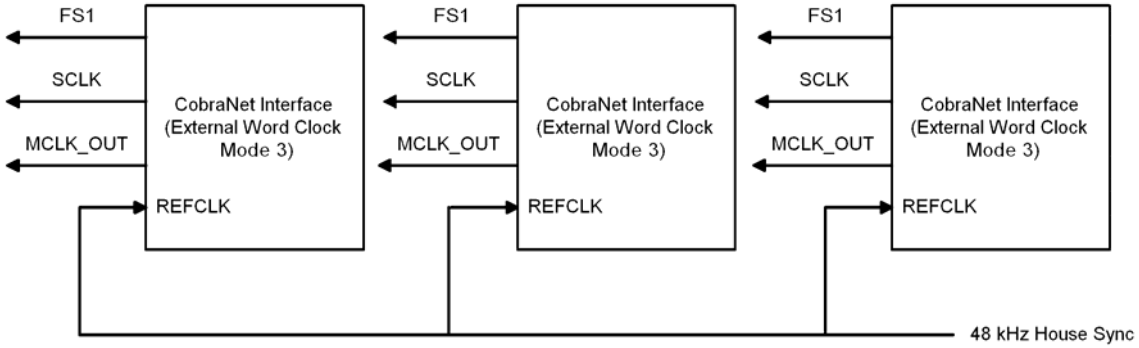

Fig. 11 – 0x01 Mode Typical Connection - Synchronization of All Nodes with an External House Sync Signal. All nodes should be on house synch

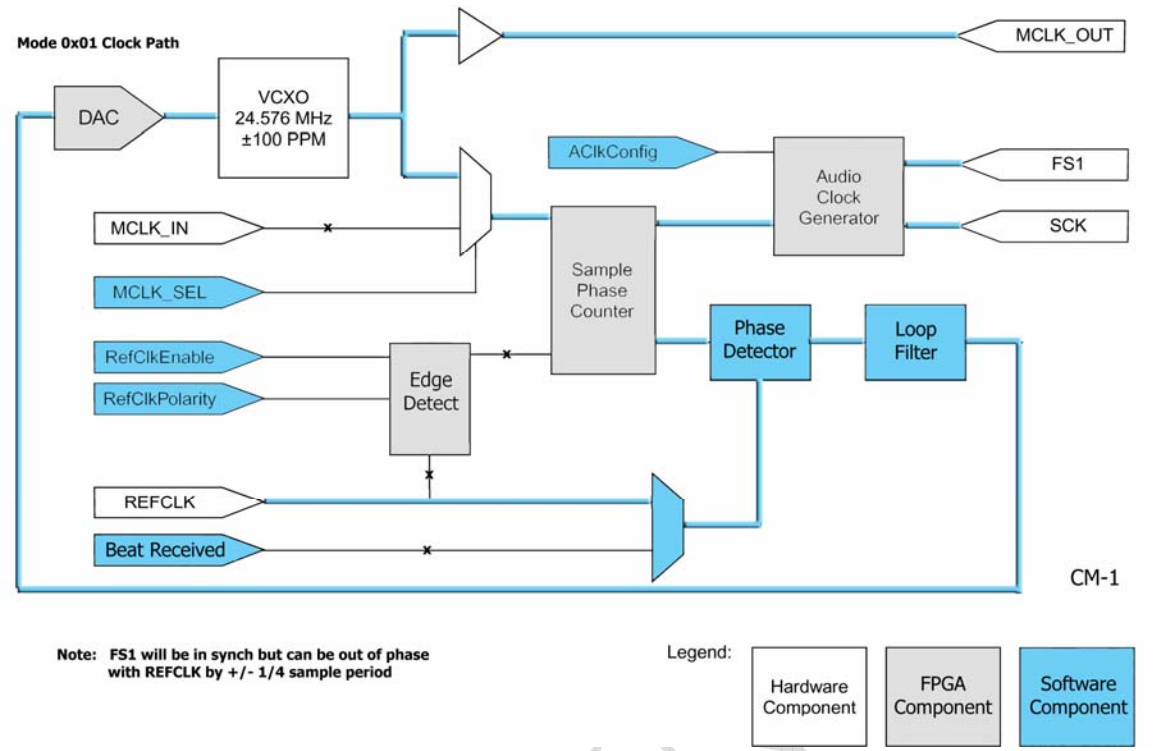

Fig. 12 - Clock circuit as used by Mode 0x01 with CM-1 modules

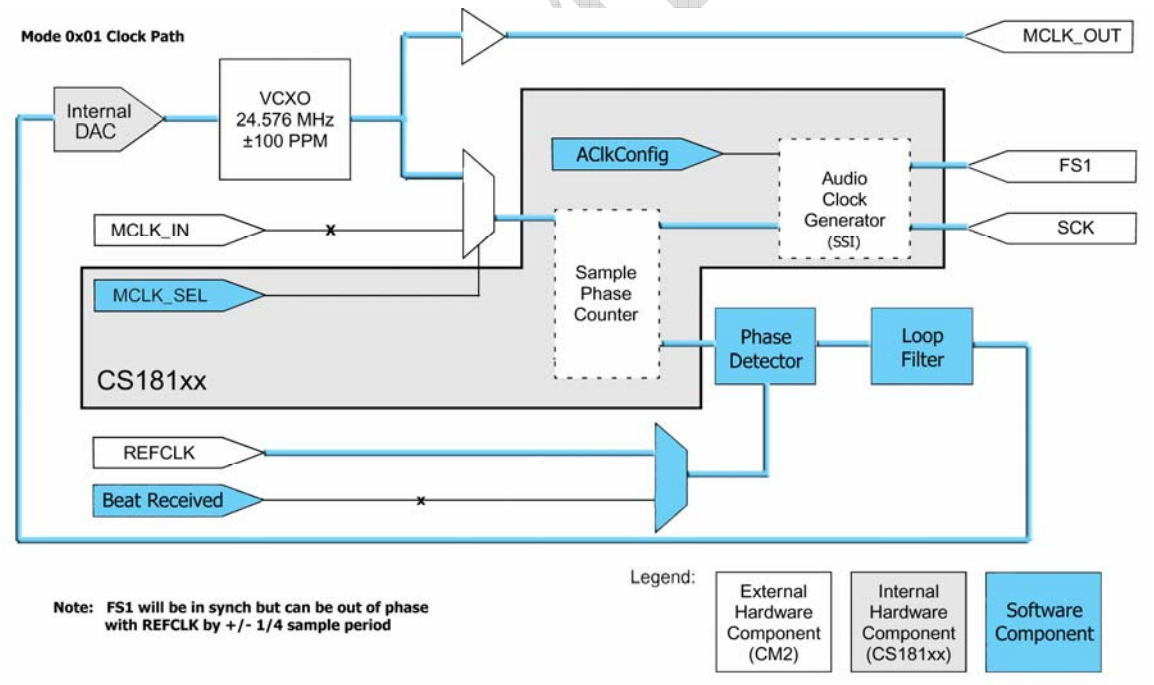

Fig. 13- Clock circuit as used by Mode 0x01 with CM-2 and semiconductors

0x04 Mode – External Master Clock Mode

In this mode all clocks are derived from an externally supplied master clock of 24.576 MHz. This mode is provided as it is easy to accomplish using the existing clock circuitry. It is most useful when trying to synchronize one or more CobraNet devices to a distributed Master Clock. However it has little practical utility as it is difficult to properly distribute a clock of this frequency and it also does not provide a means to insure synchronization of the audio clocks (SCLK, FS1). Note that MCLK_OUT is not a copy of MCLK_IN. MCLK_OUT is derived from the VCXO, which is not controlled in this mode and is not synchronous with the supplied MCLK_IN.

As Conductor:
MCLK is sourced directly from MCLK_IN. FS1 and SCLK are derived from MCLK_IN.
As Performer:
MCLK is sourced directly from MCLK_IN. FS1 and SCLK are derived from MCLK_IN.

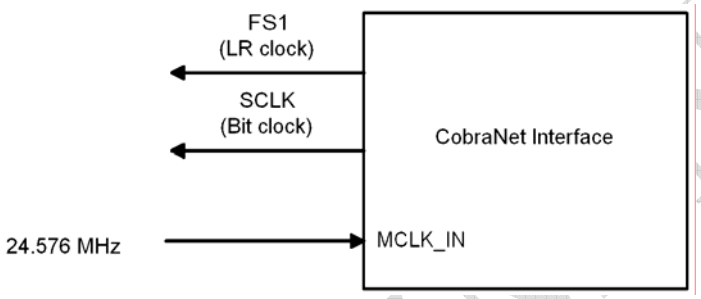

Fig. 14 – 0x04 Mode typical Connection - Synchronization to an externally supplied master clock

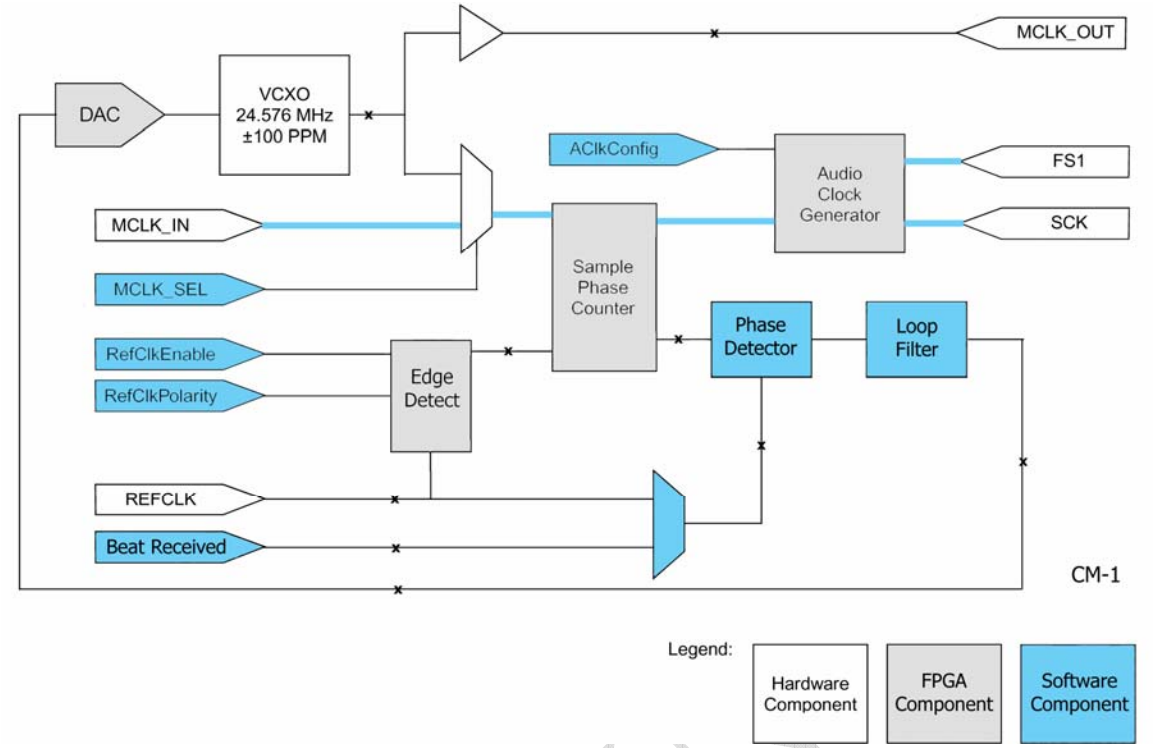

Fig. 15- Clock circuit as used by Mode 0x04 with CM-1 module

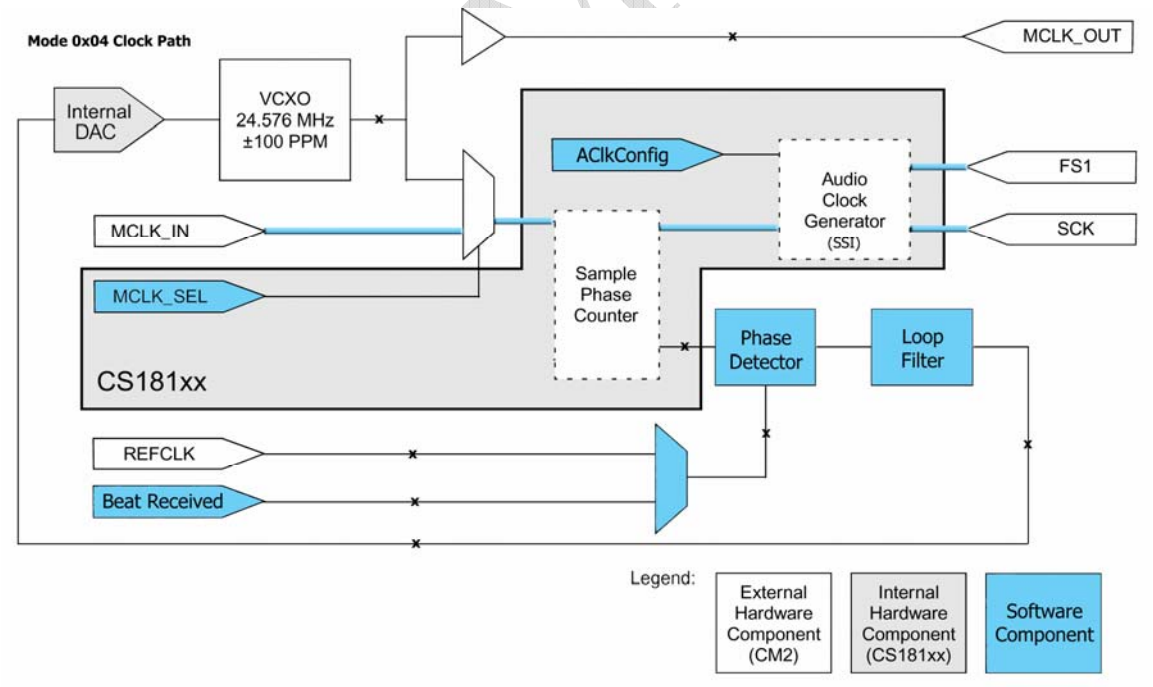

Fig. 16- Clock circuit as used by Mode 0x04 with CM-2 and semiconductors

0x14 Mode – External Master Clock Mode with External Sample Clock Synchronization

**** NOTE:** This mode is not properly supported when used with CM-2, CS1810xx or CS4961xx devices. See Appendix

In this mode all clocks are derived from an externally supplied master clock of 24.576 MHz. This mode is provided primarily to allow synchronization of multiple CobraNet interfaces within the same chassis. Or can be used, as in 0x10 Mode, to synchronize external clock circuitry derived from an external master clock. Note that MCLK_OUT is generated by the VCXO in this mode and is not a copy of MCLK_IN.

As Conductor:
MCLK is supplied by the MCLK_IN input. FS1 and SCLK are derived from MCLK_IN. As in 0x10 Mode, REFCLK is used to synchronize the clocks.
As Performer:
MCLK is supplied by the MCLK_IN input. FS1 and SCLK are derived from MCLK_IN. As in 0x10 Mode, REFCLK is used to synchronize the clocks.

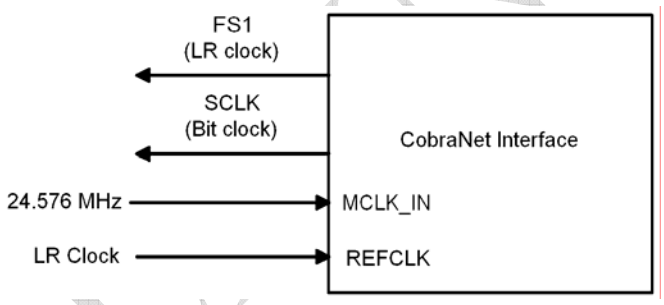

Fig. 17 - 0x14 Mode Typical Connection - Synchronization to an externally supplied master clock and word clock

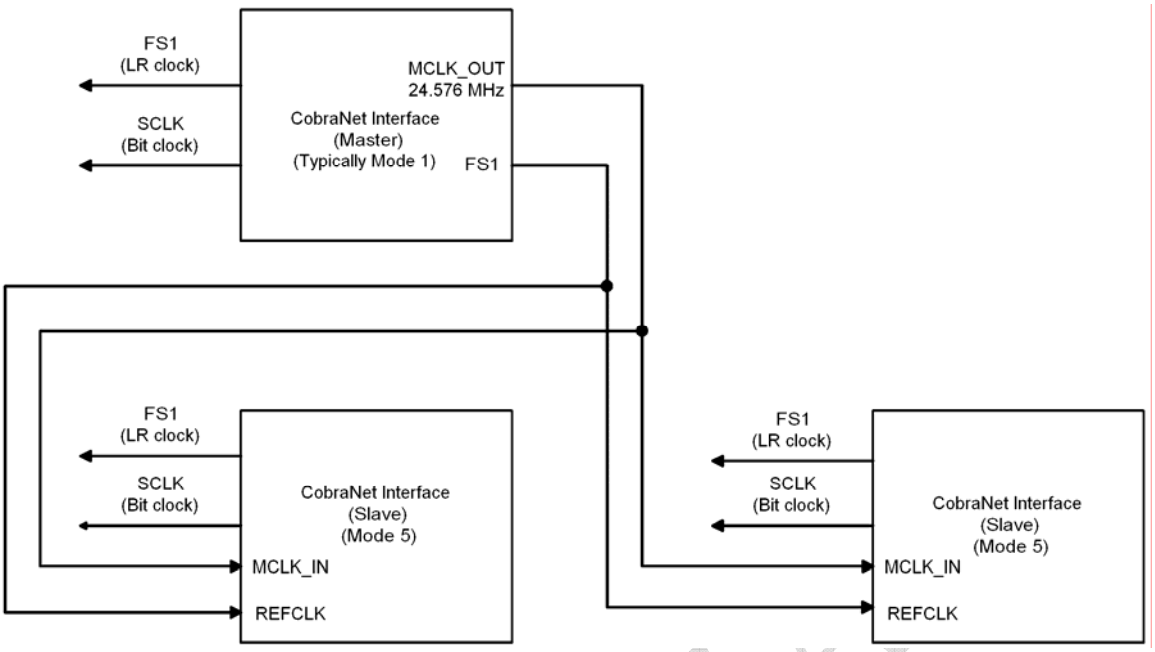

Fig. 18 - 0x14 Mode Typical Connection – Master and Ref clock supplied to slave interfaces within same chassis.

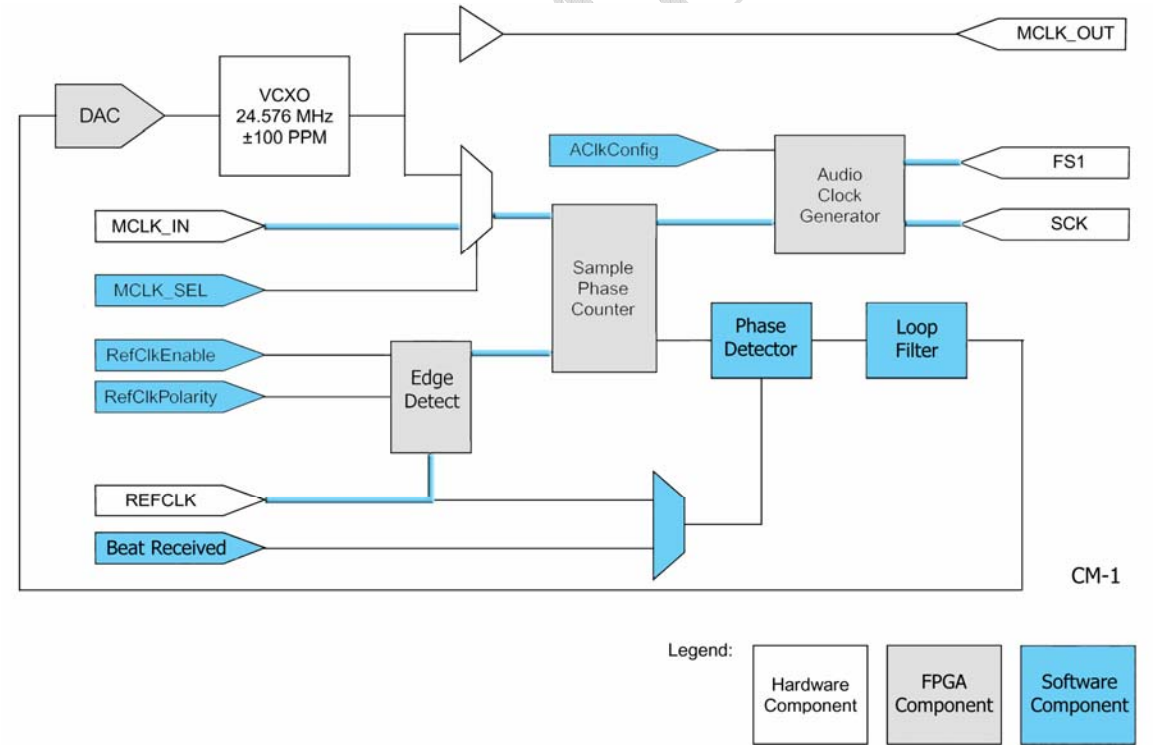

Fig. 19 - Clock circuit as used by Mode 0x14 with CM-1 module

Appendix

Using 0x10 Mode with CS1810xx, CS4961xx or CM-2

0x10 Mode is used when the designer wishes to synchronize the CobraNet clocks with an externally supplied word clock (FS1). This is not possible to do with CM-2 and Silicon based designs. The best that can be achieved is to use the circuitry below to insure that the audio clocks of the CobraNet interface are in phase with the audio clocks of the existing circuit. In this case the master clock will be derived from the CobraNet device by using the circuitry as shown in Figure 20 with the interface set to operate in clock Mode 0x00. Any clocks required by the design can be taken from the loadable counter taps and these clocks will be in phase with the audio clocks (FS1 and SCLK) generated by the CobraNet device. The Data In load value can be adjusted to insure phase alignment if necessary.

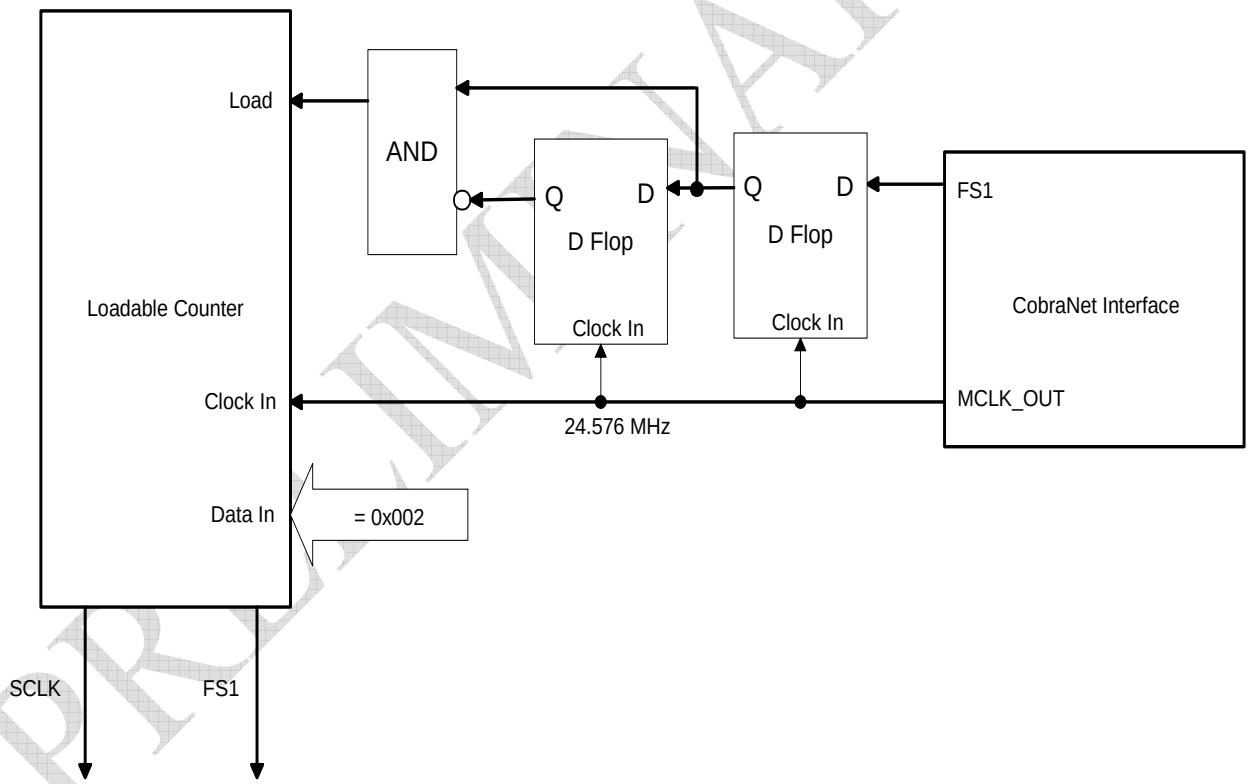

Fig. 20 - 0x10 Mode Circuitry for use with CM-2, CS1810xx or CS4961xx

Using 0x14 Mode with CS1810xx, CS4961xx or CM-2

0x14 Mode is used when the designer wishes to synchronize external clock circuitry and the CobraNet interface with an externally supplied master clock. Normally the CobraNet audio clocks would be synchronized with an externally supplied FS1. This is not possible to do with CM-2 and Silicon based designs. The best that can be achieved is to use the circuitry below to insure that the existing audio clocks are synchronized and in phase with the audio clocks (FS1, SCLK) supplied by the CobraNet device by using the circuitry as shown in Figure 21 with the interface set to operate in clock Mode 0x04. Any clocks required by the design can be taken from the loadable counter taps and these clocks will be in phase with the audio clocks (FS1 and SCLK) generated by the CobraNet device. The Data In load value can be adjusted to insure phase alignment if necessary.

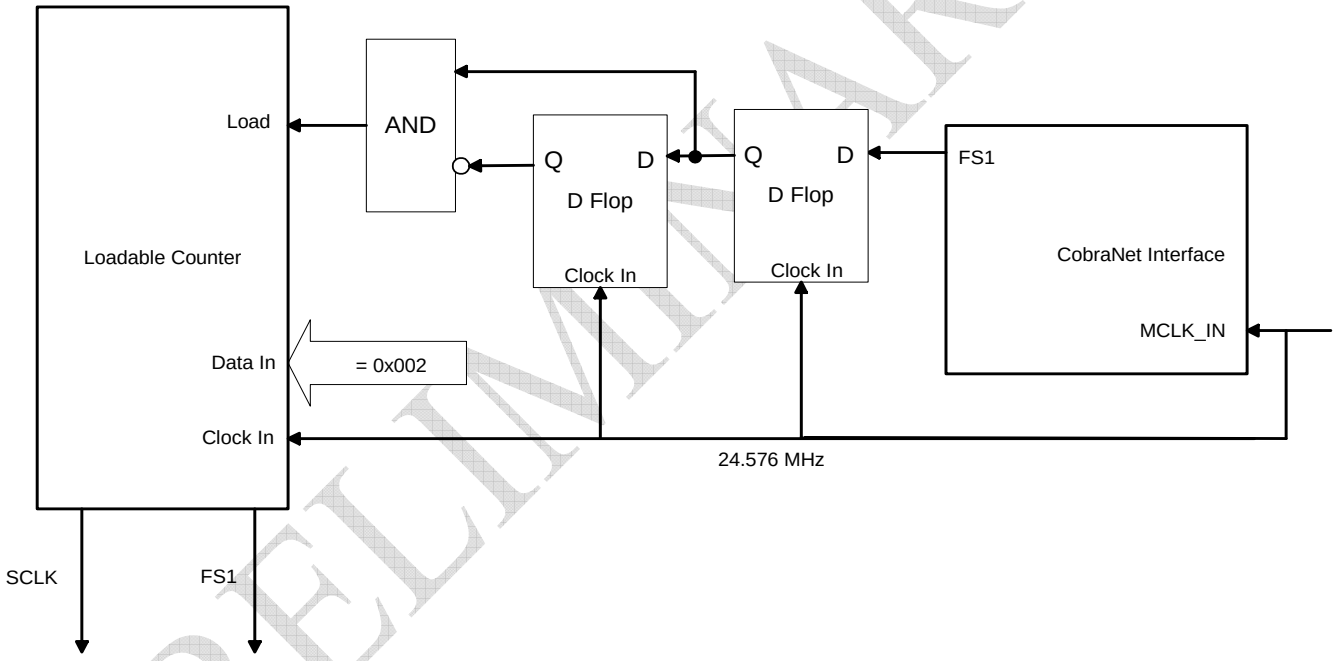

Fig. 21 - 0x14 Mode Circuitry for use with CM-2, CS1810xx or CS4961xx