



*National Semiconductor*

## **Bridge/Parallel Amplifier (BPA-200) Documentation**

National Semiconductor Corporation  
Audio Product Line  
September 19, 1997



## Table of Contents:

I. Objective & Background.....	3
II. Conclusion.....	3
III. Thermal Background.....	4
- Typical Characteristic Data	
- Single-ended Amplifier $P_{dmax}$ Equation	
- Bridged-output Amplifier $P_{dmax}$ Equation	
- Thermal Testing Conditions	
- Electrical Design Notes	
IV. BPA-200 Audio Testing.....	7
- Linearity Tests	
- Output Power Tests	
- Noise Floor Tests	
V. Schematics.....	12
- Basic Bridge/Parallel Amplifier Schematic	
- Servo Circuits	
- Power Supply Circuit	
- Detailed Bridge/Parallel Amplifier Schematic	
VI. Parts List & Vendors.....	16



## I. Objective & Background:

The objective of this amplifier was to provide a conservatively designed, reliable high-power amplifier solution to our customers. While an LM3886 from National's **Overture™** Series is capable of providing about 50W into an 8Ω load, there are many applications that require much higher output power levels (>100W) that the LM3886 alone cannot satisfy. This document provides a 200W solution using multiple LM3886s and a design concept to reach even higher output power levels.

While bridged amplifier configurations double the output swing across the load and thus theoretically increase output power by a factor 4, at that same time they quadruple the amount of power dissipation. This configuration is not a conservative design solution since the small footprint of Overture ICs makes heat dissipation difficult. The higher power dissipation causes the small ICs to run hotter, increasing the sensitivity of **SPiKe™** Protection and the IC's heatsinking requirements.

The parallel amplifier is another configuration that can be used to obtain higher output power levels by combining two IC outputs and doubling output current drive capability. However, integrated amplifiers are made to drive common off-the-shelf speakers which have load impedances of 4 and 8 ohms. The parallel amplifier using Overture ICs is ineffective in obtaining higher output power levels with 8Ω loads because the ICs are voltage supply limited. Driving a 4 ohm load is effective, but integrated amplifiers must satisfy both 4 and 8 ohm load impedances. If load impedance is not an issue, the parallel topology provides a great way of achieving higher power levels while keeping within IC power dissipation limits. The main advantage of the parallel configuration is its ability to divide total power dissipation between ICs, since each amplifier is providing half of the load current.

## II. Conclusion:

If the bridged and parallel configurations are combined, the outcome is a high-power amplifier solution that exceeds the capabilities of one IC alone, while maintaining reasonable power dissipation levels within each IC. The bridged portion doubles the output voltage swing and quadruples the total power dissipation while the parallel portion halves the current between each IC set and divides the total power dissipation between each of the four ICs. The result is higher system output power with each IC not exceeding its individual power dissipation capabilities. Higher output power levels are attained, while the ICs run at a normal temperature, keeping long-term reliability high. The basic schematic of the Bridge/Parallel Amplifier is shown in Figure 7.

The data in the following sections will exemplify that the bridge/parallel solution using multiple power ICs can meet high fidelity specifications while reaching power levels from up to 300W. The low noise and excellent linearity traits of the monolithic IC are transferred to the "booster solution," making the circuit even more attractive. In addition, the protection mechanisms within the IC, which are not easily designed discretely, add further value to the booster solution.

While the data show what specs can be achieved by the configuration, as always, good design practices need to be followed to achieve the stated results. In addition to good electrical and layout design practices, the thermal design is equally critical with Overture ICs. The following section

will expand on the thermal design aspects of Overture ICs. While the bridge/parallel configuration is only one of many that can be made to obtain higher output power levels, the concept of "design by power dissipation" is equally applicable to other types of booster circuits.

The BPA-200 schematics, and test results exemplify what can be achieved with proper component selection, thermal design, and layout techniques. The BPA-200 is only an example and is not intended for sale. This documentation is intended to show obtainable results and give general guidance of conceptual design.

### **III. Thermal Background:**

The voltage and current ratings of a power semiconductor are typically the first specs considered in designing high power amplifiers. The same is true for an integrated monolithic power amplifier. However, power dissipation ratings are equally important to the long-term reliability of the power amplifier design. When using a monolithic IC in its intended application and within its specified capabilities, the thermal design is relatively straightforward. When an IC is used beyond its capabilities, as in booster circuits, power dissipation issues become more critical and not as straight-forward. Therefore, the designer must understand the IC's power dissipation capabilities before using the IC in a booster configuration.

#### **-Typical Characteristic Data**

The power dissipation capabilities of a power IC are either specified in the datasheet or can be derived from its guaranteed output power specification. While the power dissipation rating for the LM3886T is 125W, this number can be misleading. Its power dissipation specification is derived from the IC's junction-to-case thermal resistance,  $\theta_{JC}=1\text{ }^{\circ}\text{C/W}$ , the maximum junction temperature,  $T_J=150^{\circ}\text{C}$ , and the ambient air,  $T_A=25^{\circ}\text{C}$ . As stated in the datasheet, the device must be derated based on these parameters while operating at elevated temperatures. The heatsinking requirements for the application are based on these parameters so that the IC will not go into Thermal Shutdown (TSD). The real problem for Overture ICs, however, comes from the sensitivity of the output stage's unique SPiKe Protection which dynamically monitors the output transistor's temperature. While the thermal shutdown circuitry is enabled at  $T_J=150^{\circ}\text{C}$ , SPiKe circuitry is enabled at  $T_J=250^{\circ}\text{C}$  for instantaneous power spikes in the output stage transistor. As the overall temperature of the IC increases, SPiKe circuitry becomes even more sensitive causing it to turn on before the 125W limit is reached. TSD circuitry will continue to function globally for the IC in conjunction with SPiKe circuitry. However, protection circuitry should not be activated under normal operating conditions. The question then becomes, what is the power dissipation limit for the IC such that SPiKe circuitry is not enabled? Knowing the power dissipation limit and keeping the case temperature of the IC as cool as possible will expand the output power capability without activating SPiKe Protection.

The other way to determine IC power dissipation capabilities is to analyze the output power specification in the datasheet. In the case of the LM3886T, there are two output power specification guarantees: 60W(min) into a  $4\Omega$  load using  $\pm 28\text{V}$  supplies and 50W(typ) into an  $8\Omega$  load from  $\pm 35\text{V}$  supplies. Using these two conditions and the theoretical maximum power dissipation equation

shown below, results in the following maximum power dissipation:

**- Single-ended Amplifier P<sub>dmax</sub> Equation**

$$P_{dmax} = V_{cctot}^2 / 2\pi^2 R_L$$

Non-Isolated LM3886T:

$$V_{cc} = \pm 28V, R_L = 4\Omega$$

$$P_{dmax} = V_{cctot}^2 / 2\pi^2 R_L = (\pm 28V)^2 / 2\pi^2 (4\Omega) = 39.7W \text{ not including quiescent power dissipation.}$$

$$P_{dmax} = 39.7W$$

$$V_{cc} = \pm 35V, R_L = 8\Omega$$

$$P_{dmax} = V_{cctot}^2 / 2\pi^2 R_L = (\pm 35V)^2 / 2\pi^2 (8\Omega) = 31.0W \text{ not including quiescent power dissipation.}$$

$$P_{dmax} = 31.0W$$

These results show that the IC can handle a maximum of  $\approx 40W$  of continuous power dissipation without SPiKe Protection being turned on under continuous sinusoidal input with proper heat-sinking. The same theory applies to other Overture ICs as well, like the LM3876T, which is capable of dissipating 31W with proper heatsinking. It should be noted that the results shown above are for the Non-Isolated Power Package, where the back of the package is tied to the silicon substrate, or -Vee. The Isolated Power Package has overmolded plastic on the back keeping the package electrically isolated from the silicon substrate. This extra amount of plastic increases the package thermal resistance from 1°C/W for the non-isolated version to  $\approx 2^\circ C/W$  for the isolated version. The result of increased thermal resistance is poorer power dissipation, so the numbers stated above are somewhat lower for the isolated package.

Comparing the above maximum power dissipation in single-ended mode to the bridged-mode under the same electrical conditions shows that the IC's electrical conditions would need to be derated to keep within its power dissipation capabilities. Using the bridged-output P<sub>dmax</sub> equation shown below gives us the following results:

**- Bridged-output Amplifier P<sub>dmax</sub> Equation**

$$P_{dmax} = 4V_{cctot}^2 / 2\pi^2 R_L = 2V_{cctot}^2 / \pi^2 R_L$$

The bridged-output P<sub>dmax</sub> equation represents the bridged amplifier solution. If a dual amplifier IC is used like the LM1876T, then the total P<sub>dmax</sub> would need to be dissipated in the single IC package. However, if two individual ICs are used, like two LM3886Ts, then the total power dissipation is divided between each IC.

Two Non-Isolated LM3886Ts:

$$V_{cc} = \pm 28V, R_L = 4\Omega$$

$$P_{dmax} = 4V_{cctot}^2 / 2\pi^2 R_L = 4(\pm 28V)^2 / 2\pi^2 (4\Omega) = 158.8W$$

$$P_{dmax} = 158.8W$$

$$P_{dmax}/IC = 79.4W$$



Therefore, using a bridged configuration,  $V_{cc}$  would have to be equal to  $\pm 20V$  to keep the IC's power dissipation within 40W when driving a  $4\Omega$  load! This equates to about 110W of output power in bridged-mode driving a  $4\Omega$  load. There is a major point to note here: this whole analysis assumes that the IC is being tested at the worst case power dissipation point using a continuous sinusoidal input stimulus. For "audio" applications, the average music power dissipation is much less than the maximum power dissipation created by a sinusoidal input. Therefore, a bridged configuration is feasible, depending on how conservative you want your design to be and whether you have enough thermal support to keep SPiKe protection from being activated. It also depends on whether or not you need to meet industry rating standards like EIA or IEC.

In certain situations, the bridged solution will work, but more caution needs to be applied along with better thermal management. The proposed bridge/parallel solution will provide a more robust design than the bridged circuit, allowing higher output power levels to be obtained.

In addition to better heatsinking, the application of a small fan can substantially increase the IC's continuous power dissipation capabilities for either solution. While the air flow of the fan used to take the data is not known, its air flow seemed to be consistent with a typical computer fan. The IC maximum power dissipation data is summarized below in Table 1. The data shown below should only be used as a guideline of possible IC power dissipation capability. Your electrical design parameters and thermal management may be different, changing the achievable results. As always, lab testing is recommended to verify any solution.

Power IC	Pdmax (No Fan)	Pdmax (With Fan)
LM3886T	40W	60W
LM3886TF	30W	45W

Table 1. Power Dissipation Results

**- Thermal Testing Conditions**

The data summarized in Table 1 was obtained by using the bridge/parallel configuration and the following conditions: The system was warmed up for an hour using a power dissipation of 30W per device with a  $4\Omega$  load. Four different temperature points were measured after stabilizing, then the supply voltages were incremented while insuring that SPiKe Protection was not enabled during each test by monitoring each amplifier output. The supply voltages continued to be incremented until SPiKe protection or thermal shutdown was enabled, providing the IC's power dissipation limits under those operating conditions.

The input stimulus was a 20Hz sinewave with an amplitude corresponding to the worst case power dissipation for the given load and supply voltage. The ICs were evenly spread out along the heatsink with dimensions of: 3.25" high x 13.25" long x 1.3125" deep. The main body of the heatsink was 0.25" thick with (10) 1.0625" deep fins. Unfortunately, the fins ran horizontally, which hindered heat radiation without a fan, but helped with air flow and heat dissipation when a fan was used.



This same testing procedure can be used for any number of booster circuits, including variations of the bridge/parallel circuit where numerous ICs are paralleled to reduce power dissipation, allowing low impedance loads to be driven to obtain even higher output power levels.

#### - Electrical Design Notes

The following electrical design notes will aid in obtaining a high-performance amplifier solution:

- Input resistor values, should be equal and have a 0.1% tolerance to minimize amplifier noise. These resistor pairs are: Rb1 & Ri1, Rb2 & Ri2, Ri3 & RC3, and Ri4 & RD3, as shown in Figure 11.

- 0.1% tolerance resistors for close gain matching should be used to minimize offset voltages when not using servo circuits.

- 1% tolerance high wattage ballast resistors are required when paralleling outputs to keep differently biased outputs from fighting each other. The wattage rating is dependent upon the amount of current expected to flow from each output and the resistance of the ballast resistor;  $P=I^2R$ . A good resistance value is  $0.1\Omega$ . Amplifier efficiency is lost if this resistor value is too large like  $1\Omega$ , since 10A times  $1\Omega$  is 10V of output voltage drop!

- Low output offset voltage servo op amp is required to minimize solution output offset voltage.

- An input buffer is required because of the low input impedance from paralleling of the inputs. Higher valued gain setting resistors could be used at the risk of increasing noise susceptibility. The proposed solution provides the easiest way around gain resistor matching and providing a high input impedance.

#### IV. BPA-200 Audio Testing:

The following graphs represent the performance level attainable from the bridge/parallel circuit when well laid out and properly heatsinked. The testing focused on maximum output power capabilities, amplifier linearity and noise level.

##### - Linearity Tests

The linearity of the amplifier is represented by the low THD+N values shown in Figures 1 and 2. Figure 1 represents the THD+N vs Frequency for 1W, 56W, and 200W power levels. Figure 2 represents the THD+N vs Output Power Level for 20Hz, 1kHz, and 20kHz. The THD+N between 20Hz and 1kHz is less than 0.004% from 1W to the clipping point. The 20kHz THD+N is less than 0.02% from 1W to the clipping point. The continuous clipping point power is around 210W while the power at 10% THD is 300W. These THD graphs were obtained using relative THD units, which indicates that the noise level for the amplifier is quite low. Typically, the noise level becomes a significant THD+N contributor at low power levels and shows up as a linearly decreasing function of increasing input signal amplitude. In Figure 2, the THD+N decreases from 0.004% to 0.001% from 1W to the clipping point for frequencies between 20Hz and 1kHz. The THD+N decreases from 0.02% to 0.009% from 1W to 50W and rises thereafter up to about 0.015%.

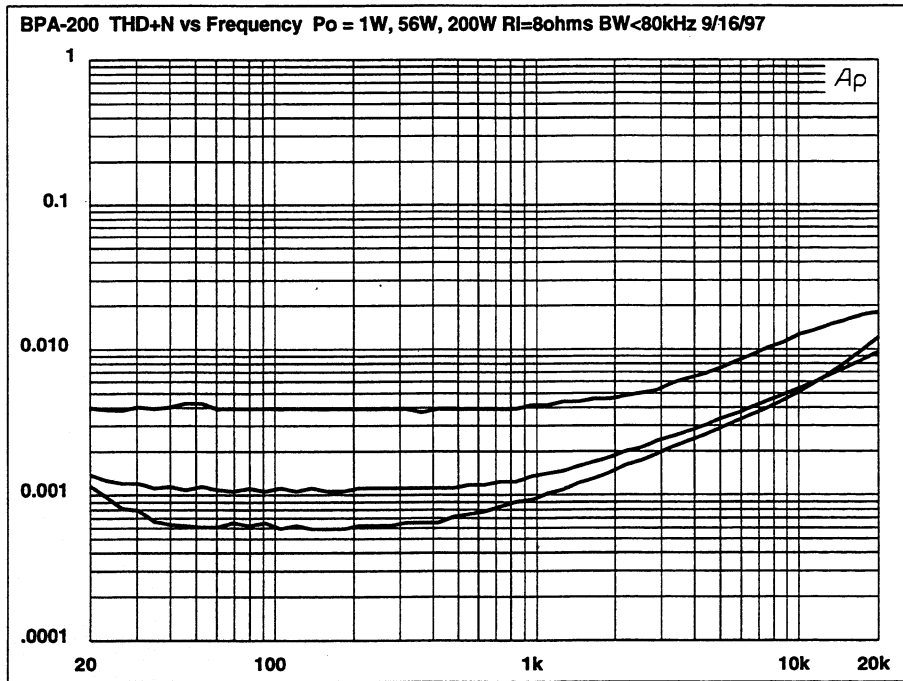


Figure 1. THD+N vs Frequency

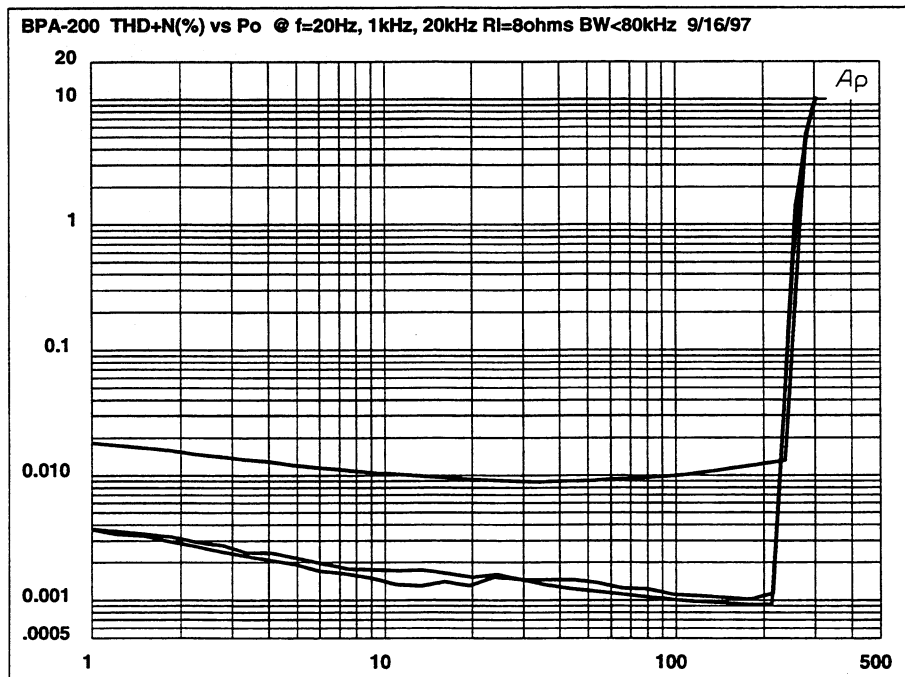


Figure 2. THD+N vs Output Power





### - Output Power Tests

Although the amplifier was designed based on thermal dissipation capabilities using continuous sinusoidal inputs, the output power levels attainable are significantly greater with pulsed waveforms that more accurately reflect music material. The continuous clipping point power and burst power levels are shown in Table 2 below:

Load Impedance	Continuous Clipping Point Power	Burst Clipping Point Power
8Ω	225W	295W
4Ω	335W	450W

Table 2. BPA-200 Maximum Output Power Levels

The burst power levels were obtained using a 20Hz sinewave with two cycles on and twenty cycles off. The output power capability of the BPA-200 is further substantiated by the power bandwidth measurement. The amplifier is capable of producing 200W continuously into an 8Ω load up to  $f = 90.5\text{kHz}$  with little change in THD+N. The graph in Figure 3 shows the power bandwidth measurement. Also notice that the low frequency power in the graph is not rolled off as would normally occur with a DC blocking capacitor. The servo circuits allow the low frequency power to remain constant down to DC without high output offset voltage.

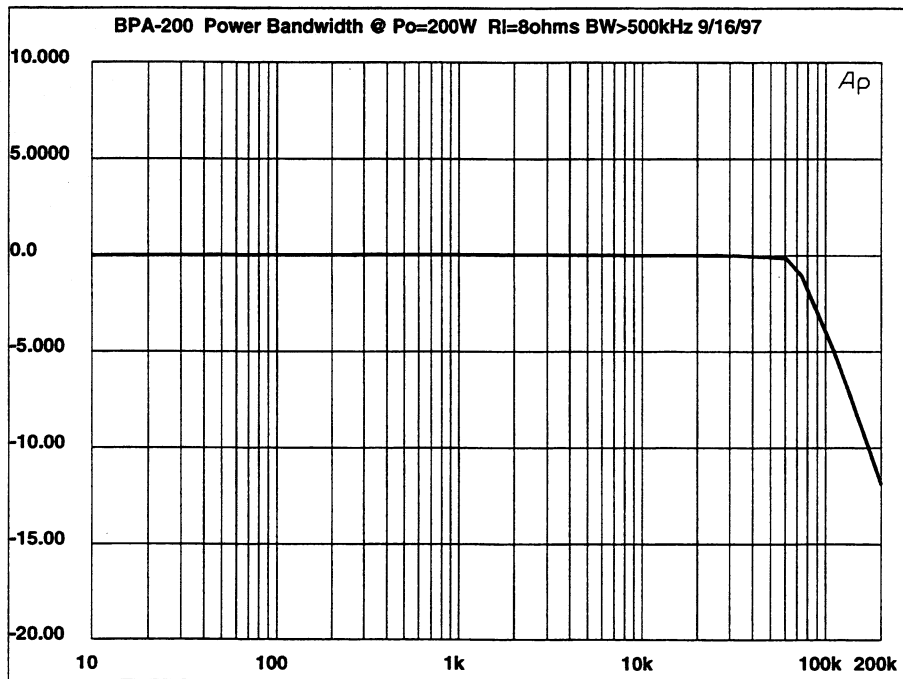


Figure 3. Power Bandwidth

**- Noise Floor Tests**

The following plots exemplify the low-noise aspects of the BPA-200. Figure 4 was obtained using an 8k FFT relative to 1dBV with a measurement bandwidth of 22kHz. Figure 5 is the same measurement as Figure 4, but shown in a logarithmic scale. An FFT analyzer is extremely handy in determining the noise culprit when debugging a new circuit and its layout, as well as evaluating the coupling effects of the 60Hz component and its harmonics. As shown in Figure 6, the noise level is quite low and the influence of the power supply is relatively small. The highest 60Hz components reach -105dBV, while the noise floor sits around -120dBV.

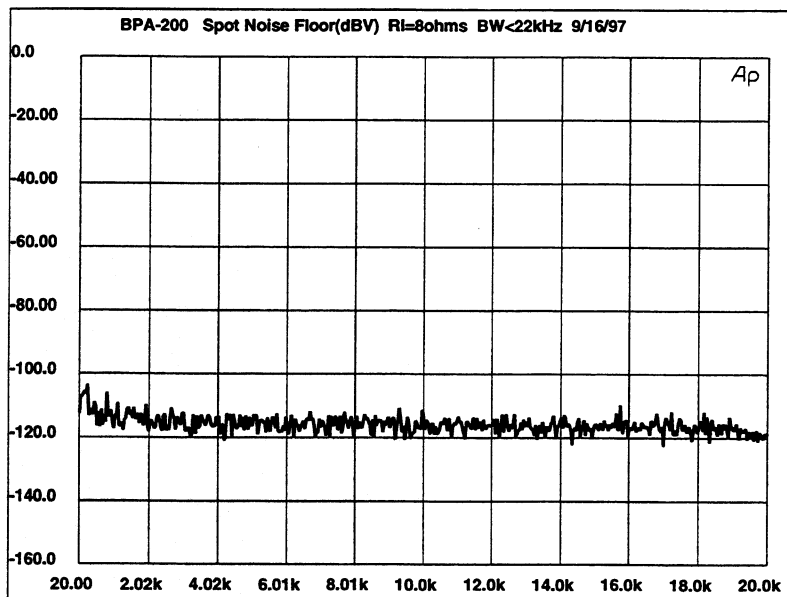


Figure 4. Linear-Scale Noise Floor

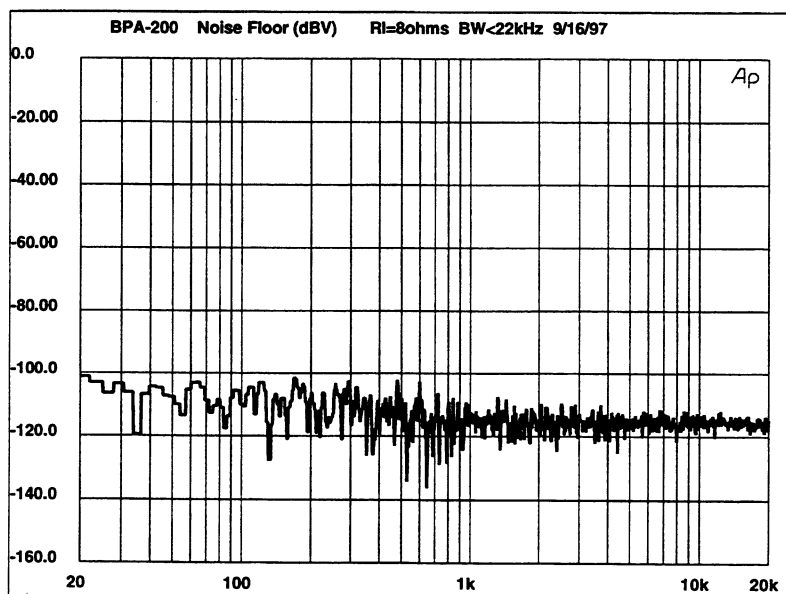


Figure 5. Log-Scale Noise Floor

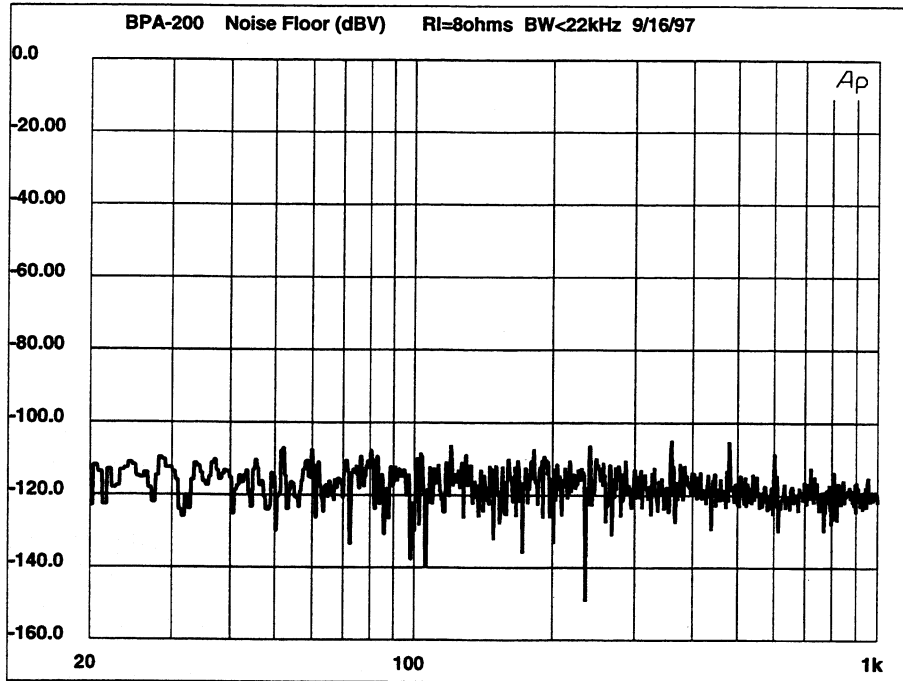


Figure 6. Log-Scale 60Hz Noise Floor

Even with the limited number of graphs shown, the quality of this amplifier from a measurement perspective is quite good. However, with all audio equipment, nothing is really better than doing a test drive with your ears. We recommend that you check this design concept out.

V. Schematics:  
- Basic Bridge/Parallel Amplifier Schematic

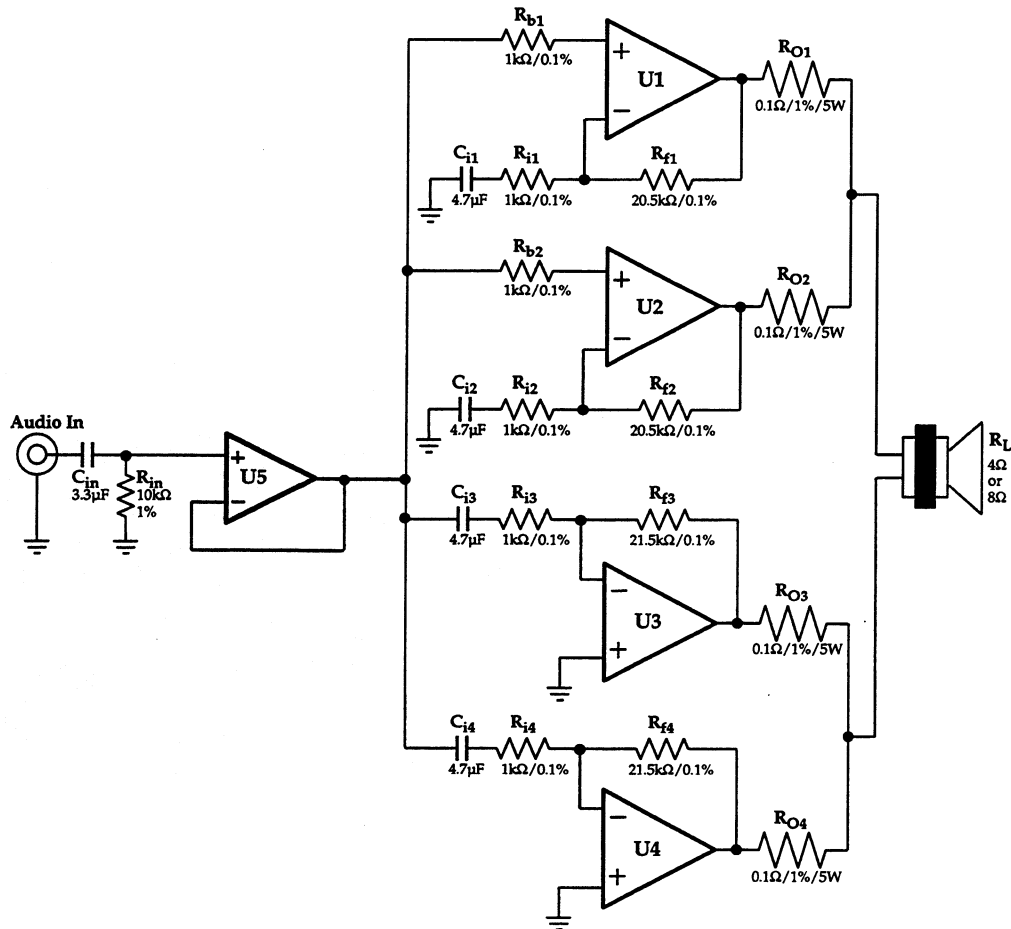


Figure 7. Basic Bridge/Parallel Amplifier Schematic

- Servo Circuits

While output ballast resistors in the basic bridge/parallel circuit work well to keep separately biased IC outputs from fighting each other, the addition of servo circuits will minimize output offset voltages that cause output voltage inequalities. Different output offset voltages cause a constant current to flow between outputs that increases IC power dissipation. By minimizing output offset voltages, all of the ICs will run cooler, expanding the ICs' longterm reliability and output power capability without activating sensitive protection circuits.

Typically, offset voltages are compensated for by using input and output coupling capacitors. Power amplifiers used in a single-supply configuration, utilize large value, large size electrolytic or polypropylene capacitors. This is because the load impedance is 4 or 8Ω and the RC combination creates a highpass filter that can rolloff audio frequencies. Since these output coupling capacitors



have nonlinearities and are quite large, many designers choose to employ split power supplies. While split power supplies don't use these capacitors, a DC blocking capacitor is needed somewhere in the circuit to protect speakers. This capacitor is typically,  $C_{i1}$ ,  $C_{i2}$ ,  $C_{i3}$ , &  $C_{i4}$  as shown in Figure 7. With the application of a servo circuit, this capacitor can also be eliminated as shown in Figures 8 & 9.

Servo circuits are essentially integrator op amp circuits that integrate offset voltage changes from the power op amp's output and feed back the integrated voltage to the opposite input of the power op amp. A servo circuit is required at each IC output of the bridge/parallel circuit to keep currents from flowing between IC outputs. Without each output compensated, one offset voltage will cause current to flow between ICs, increasing power dissipation. If gain setting resistors are 0.1% and closely matched, the servo circuit may be left out, but DC blocking capacitors will be required.

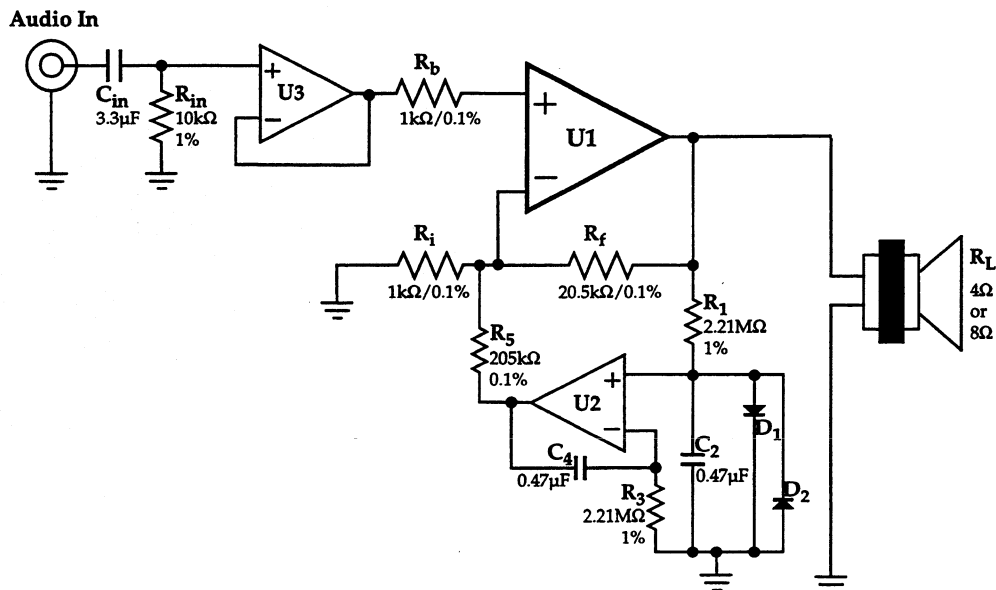


Figure 8. Non-Inverting Servo Amplifier Schematic

The inverting type servo amplifier applied to the inverting amplifier portion of the bridge/parallel circuit is shown in Figure 9. The non-inverting type servo circuit could be applied to the inverting input of U1 to achieve the same result, however, it uses an extra RC network that can be eliminated with the inverting type servo.

If a different power amplifier gain is desired, other component values can be used under the following conditions: In Figure 8, resistor  $R_5$  should be about 10 times the value of  $R_f$ , while  $R_i$  and  $R_b$  should be equal. In Figure 9, resistor  $R_3$  should be about 10 times the value of  $R_f$ , while  $R_4$  and  $R_i$  should be equal. For both the Non-Inverting and Inverting Servo solutions, the input clamping diodes should be low-leakage, with low-leakage film capacitors having a high-quality dielectric such as polypropylene or polystyrene (mylar), and metal-film resistors.

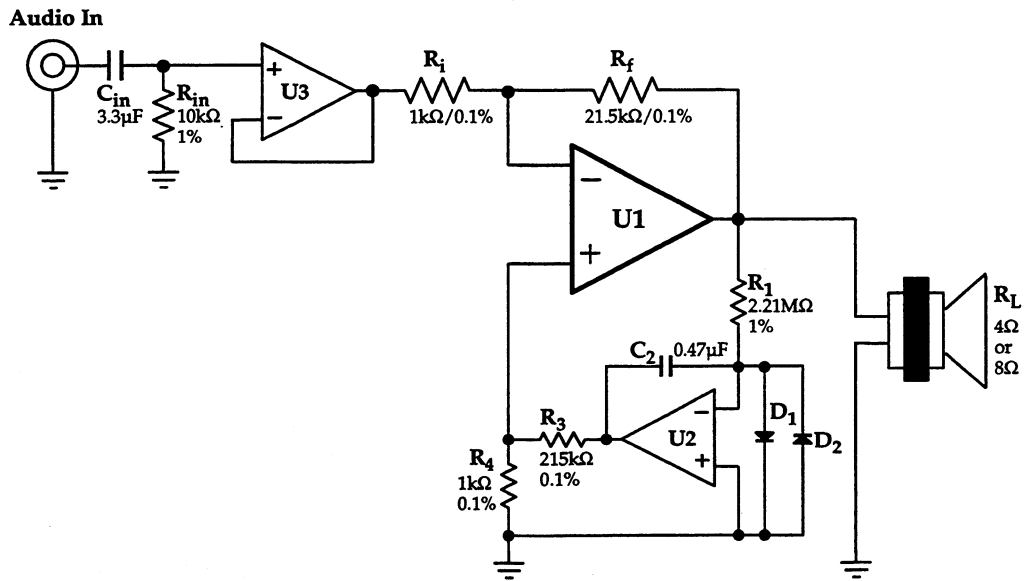


Figure 9. Inverting Servo Amplifier Schematic

**- Power Supply Circuit**

The power supply portion of the amplifier is made up of a typical unregulated bipolar power supply. The supply is comprised of an input AC line filter, surge protecting MOVs, a separate 385VA toroidal transformer for each channel, and 40,000µF of supply reservoir capacitance for each supply voltage rail.

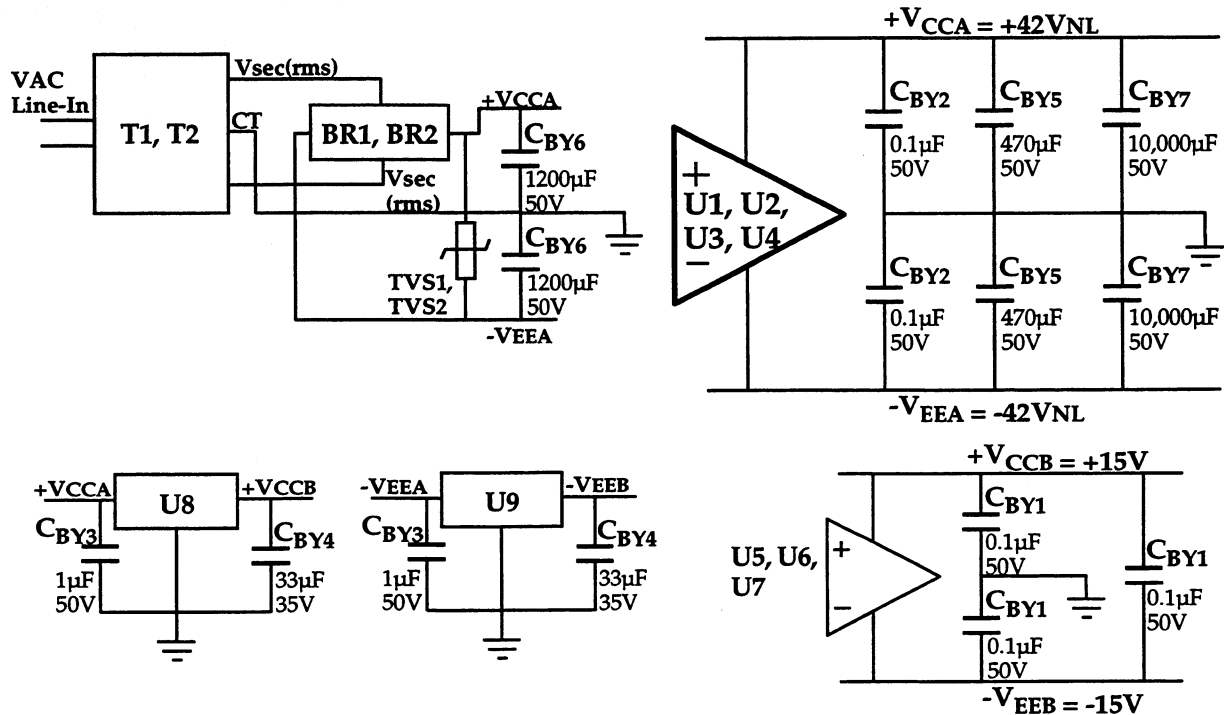


Figure 10. Power Supply Schematic



- Detailed Bridge/Parallel Amplifier Schematic

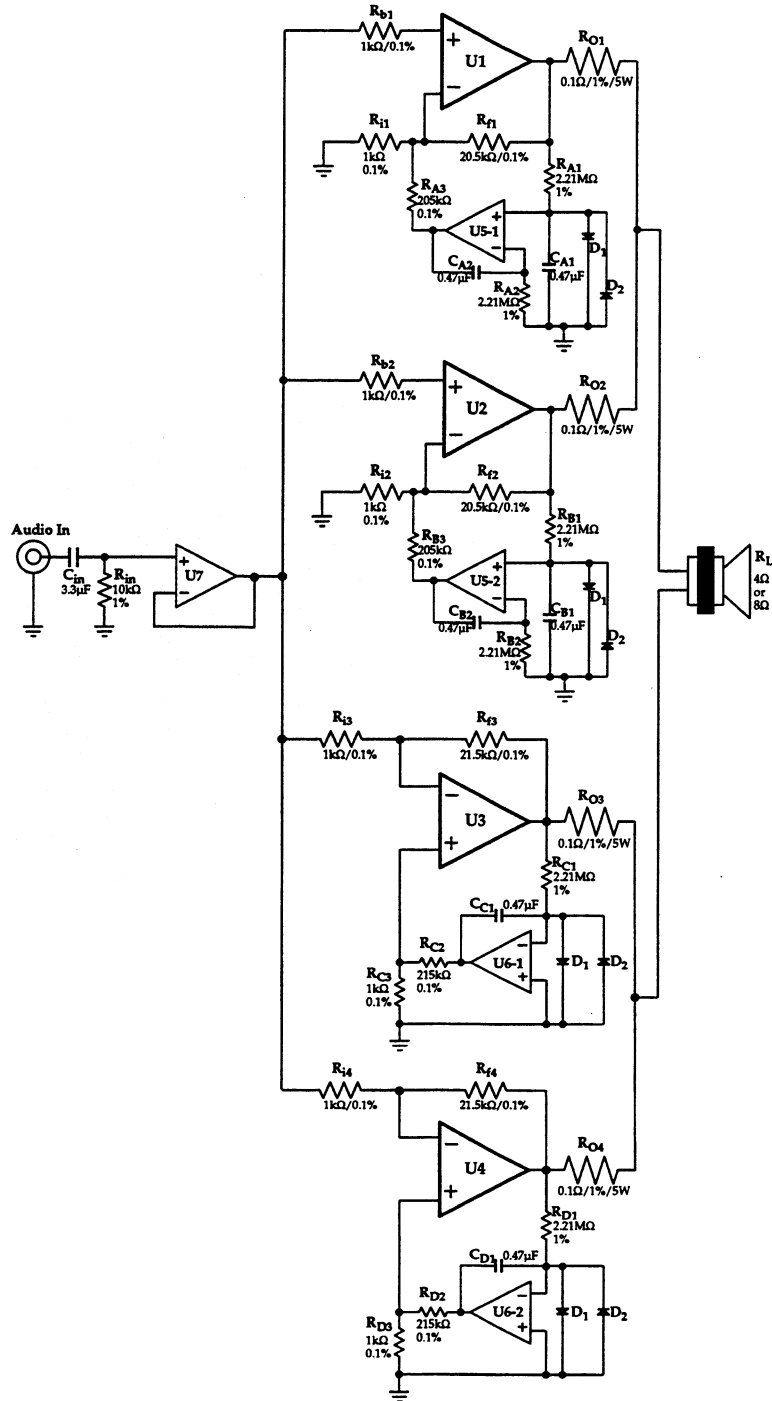


Figure 11. Detailed Bridge/Parallel Amplifier Schematic



VI. Parts List & Vendors:

DESCRIPTION	DESIGNATOR	MANUFACTURER'S PART NUMBER
<b>Passive Components</b>		
0.47 $\mu$ F/100V Mylar Capacitor	CA1, CA2, CB1, CB2, CC1, CD1	Electrocube, 230B-.47 $\mu$ F-100V-JB
3.3 $\mu$ F/250V Polypropylene	Cin	Panasonic, ECW-F2335JB
0.1 $\Omega$ /5W/1% Power Ballast Resistor	RO1, RO2, RO3, RO4	Dale, RS-5-0.1-1%
1k $\Omega$ /0.1% Metal Film Resistor	Rb1, Rb2, Ri1, Ri2, Ri3, Ri4, RC3, RD3	Dale, RN-55D-1000-B
10k $\Omega$ /1% Metal Film Resistor	Rin	Dale, RN-55D-1002-B
20.5k $\Omega$ /0.1% Metal Film Resistor	Rf1, Rf2	Dale, CMF-55-20.5k-.1%-T2
21.5k $\Omega$ /0.1% Metal Film Resistor	Rf3, Rf4	Dale, MF-55-21.5k-.1%-T2
205k $\Omega$ /0.1% Metal Film Resistor	RA3, RB3	Dale, CMF-55-205k-.1%-T2
215k $\Omega$ /0.1% Metal Film Resistor	RC2, RD2	Dale, CMF-55-215k-.1%-T2
2.2M $\Omega$ /1% Metal Film Resistor	RA1, RA2, RB1, RB2, RC1, RD1	Dale, CMF-55-2.21M-.5%-T9
1N456A Low Leakage Diodes	D1, D2	National Semiconductor (NSC) 1N456A
<b>Integrated Components</b>		
LM3886T, 50W Monolithic Power IC	U1, U2, U3, U4	NSC, LM3886T
LF412ACN, Dual JFET Input Op Amp	U5, U6	NSC, LF412ACN
LF411ACN, JFET Input Op Amp	U7	NSC, LF411ACN
LM78L15ACZ, +15V Linear Regulator	U8	NSC, LM78L15ACZ
LM79L15ACZ, -15V Linear Regulator	U9	NSC, LM79L15ACZ
<b>Power Supply Components</b>		
385VA, 60Vrms Sec. Transformer	T1, T2	Toroid Corp. of Maryland, #738.302
Bridge Rectifier	BR1, BR2	General Instrument, KBU8B
100V, 1.5kW Metal Oxide Varistor (Transient Voltage Suppressor)	TVS1, TVS2	Digikey, 1.5KE100CACT-ND
0.1 $\mu$ F/50V Ceramic Capacitor	CBY1	Sprague, 1C25Z5U104M050B
0.1 $\mu$ F/50V Polypropylene	CBY2	Panasonic, ECQ-P1H104GZ
1 $\mu$ F/50V Electrolytic Capacitor	CBY3	
33 $\mu$ F/35V Electrolytic Capacitor	CBY4	
470 $\mu$ F/50V Electrolytic Capacitor	CBY5	Mallory, SKR471M1HJ21V
1200 $\mu$ F/50V Electrolytic Capacitor	CBY6	Mallory, LP122M050A1P3
10,000 $\mu$ F/50V Electrolytic Capacitor	CBY7	Panasonic, ECE-S1HU103U
AC Line Connector		Schurter, 34.3124
Power Switch (Bowden Cable)		Schurter, 886.0101
<b>Miscellaneous Hardware</b>		
IC 11 pin Sockets		Yamaichi, SMT-15420