TOSHIBA

FILE NO. 526-9401

VIDEO WALL PROJECTION UNIT
P4100U

SERVICE TEXT

TOSHIBA CORPORATION

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CONTENTS

SECTION 1.
INTRODUCTION

1-1. DESCRIPTION

P4100U is 41" video wall projection unit. The P4100U consists of two pieces main constructions so called "front box" and "rear box". It can be made small when not in used. So, it is easy to transfer, store, install or maintenanced. So it can be repaired easily. The alignment can be implemented both computer and remote hand set. (Available in option)

This service text explains operations of main circuits of the P4100U.

1-2. FEATURES

Mechanism

Item	Features
Screen Edge	• 2.5mm **– merit –** · less obvious than the other when enlarged picture
Cabinet Structure	• Separate type (2 parts) **– merit –** · Several assemble methods · Easy replaceable electronics · Easy access electronics while servicing
Compact Size Transportation	• Slide-in electronics **– merit –** · less foot-print for warehousing and transportation
Depth	• 1,110mm (43.7") **– merit –** · less projecting cubes from wall
Lifting Method	• Versatile Handles in more locations

Optical

Item	Features
Screen Technology	• Improved Vertical view angle by additional lenticular **– merit –** · Wider observation angle
	• Non linear distribution of diffuser **– merit –** · Improved vertical/horizontal color shift

Electronics

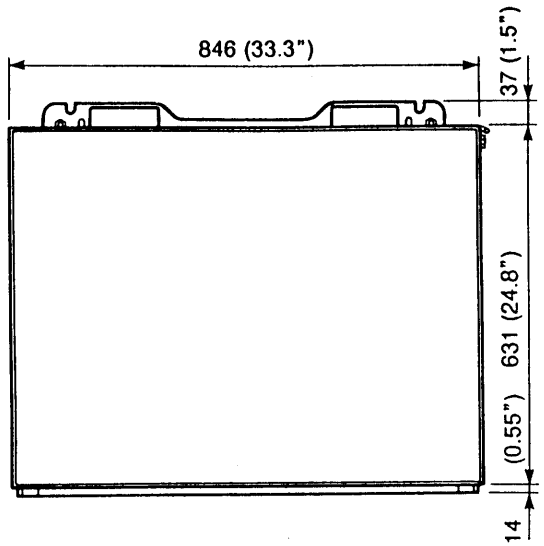
Item	Features
Adjustment	• Remote Control (15m Cable detachable) **– merit –** · possible to adjust at view point · even after wall setup adjustment is easy
RS-232C Adjustment	• All remote control functions are equipped **– merit –** · PC can control all adjustments
Test Pattern	• Single cross and cross hatch **– merit –** · Both static and dynamic convergences adjustment possible

1-3. LIST OF UNITS

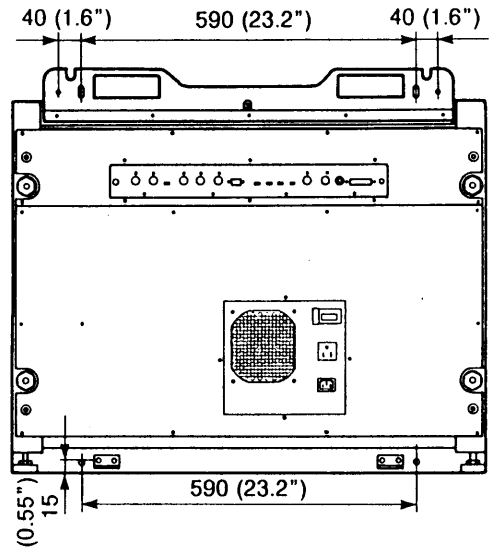
	Unit name	Circuit name	Unit construction	Name of module	Size (mm)
1	PB4478	POWER		TLC137TR/ R8700S	330×249
2	PB4486	DEF		TLC137TR/ R8700S	330×249
3	PB4487	CONV OUT	Two boards of the same	TLC134	330×249
4	PB4492	VIDEO		TLC134	330×249
5	PB4493	CONTROL/ CONV		TLC134	330×249
6	PB4494	CPT-D/ COMB	Four different boards	TLC134	249×249

1-4. NAME AND DIMENSIONS

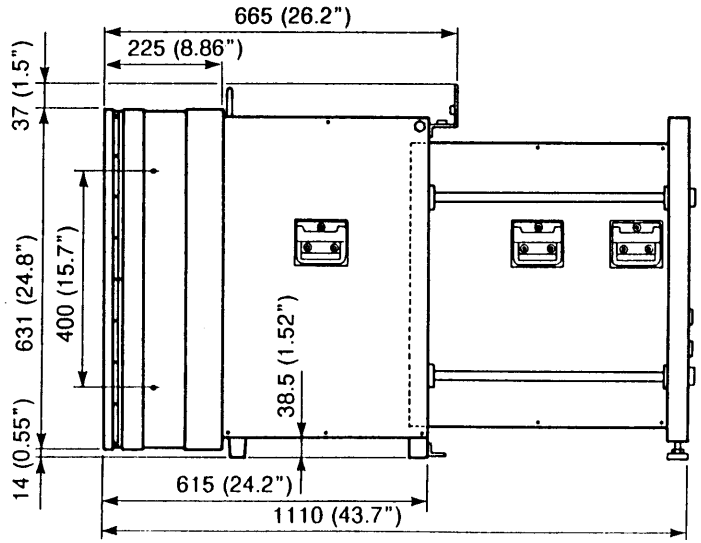
[FRONT]



[REAR]



[SIDE VIEW]



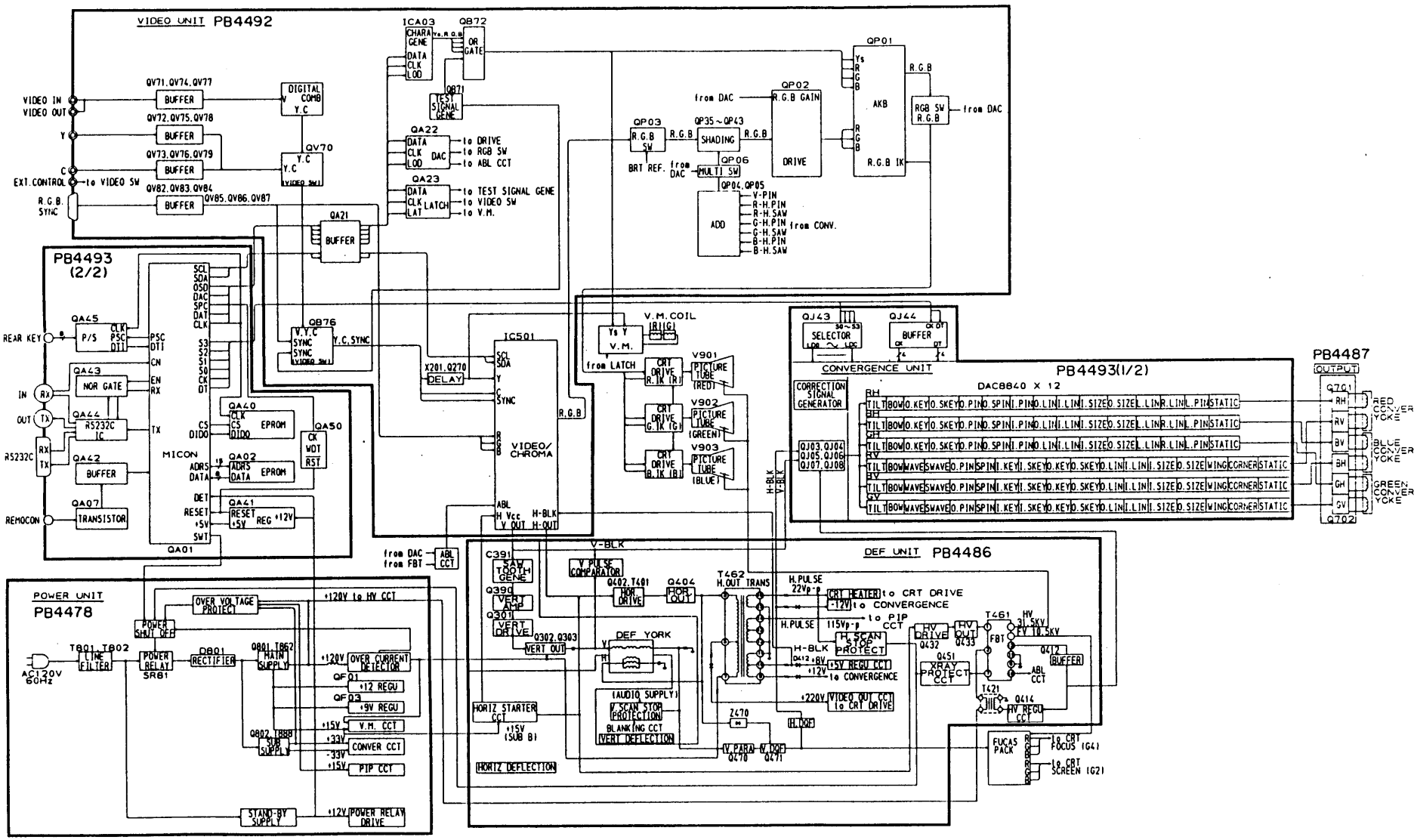
1-5. SPECIFICATIONS

Type		41" Projection Unit	
TV System		NTSC	
Projection tube		7" CRT × 3	
Resolution		800 line or more (Horizontal) 350 line or more (Vertical)	
Usable field of view		150° (Horizontal), 60° (Vertical)	
Usable temperature		5~35°C (41~95°F)	
Input signals			
	Video input	Input terminal Input level	BNC connector × 1 1V(p-p) (75Ω) Standard level
	Video output	Output terminal	BNC connector × 1
	Y/C separate input	Input terminal Input level	Luminance (Y): BNC connector × 1 Chromainance (C): BNC connector × 1 Luminance (Y): 1V(p-p) (75Ω) Chrominance (C): 0.286V(p-p) (75Ω)
	Ext. control signal input	Input terminal Signal input	BNC connector × 1 Open: Video input Short circuit: Y/C separate input
	RGB input	Input terminal Input level	D SUB 9-pin (male) connector × 1 R, G, B signal: 0.7V(p-p) (75Ω) Sync signal: 0.3V(p-p) (75Ω)
	Remote control input	Input terminal Signal input	φ 3.5mm terminal Remote signal, +3V, GND
	RS-232C port	Input terminal Speed Mode	D SUB 25-pin (female) connector × 1 1,200, 2,400, 4,800, 9,600 baud No parity, 8 bit, 1 stop bit
Combination I/O		Input terminal	DIN 5-pin connector × 2
White balance switch		2 mode selectable	
Electrical requirement		AC 120V, 60Hz	
Power consumption		260W (370VA)	
Dimensions		846(W) × 682(H) × 1110(D) mm (33.3"(W)×26.9"(H)×43.7"(D)) (excluding protruding parts)	
Weight		85kg (187 lbs.)	
Accessories		Control cable (DIN 5-pin connector) Power cable	

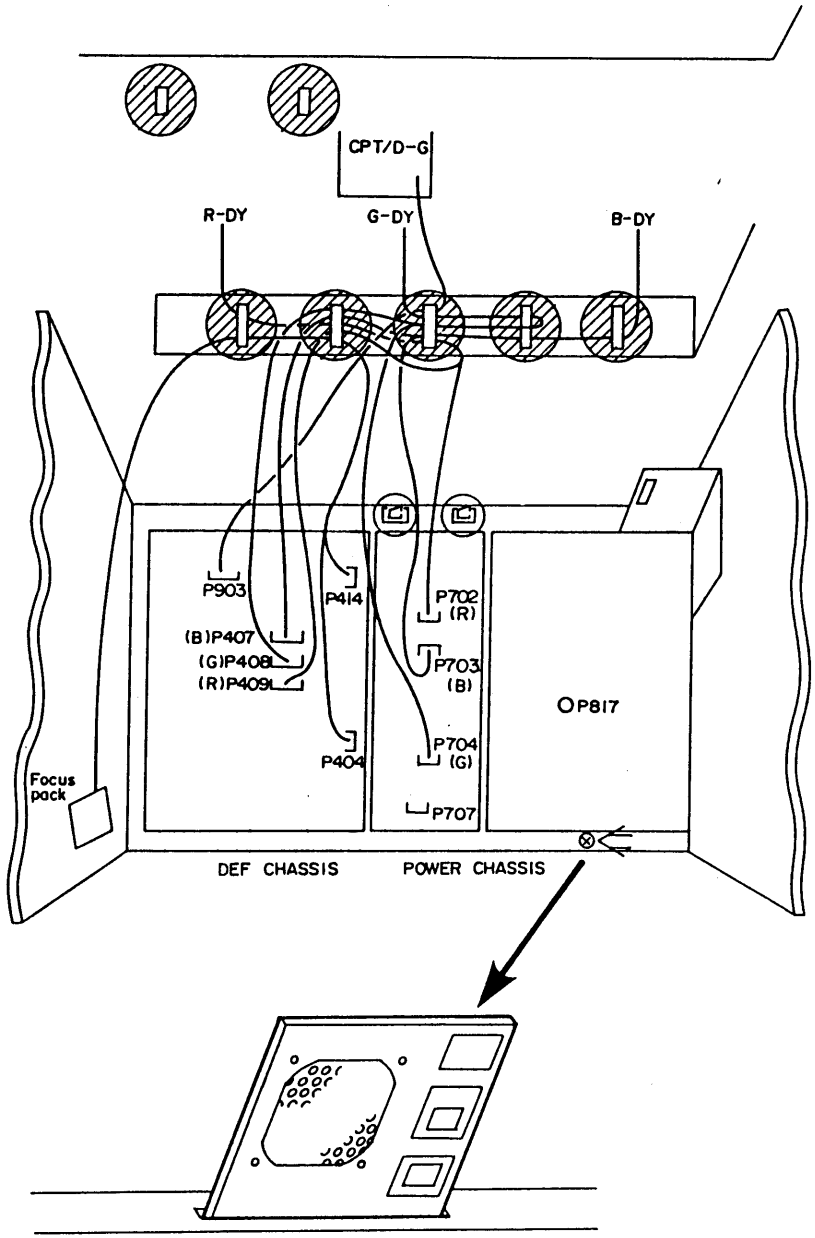
* A control cable is supplied for controlling video will projection unit being used toghther.

* The specifications and design of this product are subject to change without notice due to improvement.

1-6. BLOCK DIAGRAM



1-7. PARTS ARRANGEMENT



SECTION 2.

OPTICAL SYSTEM

2-1. NECK CONSTRUCTION

2-1-1. Main Components of Neck of Projection Tube

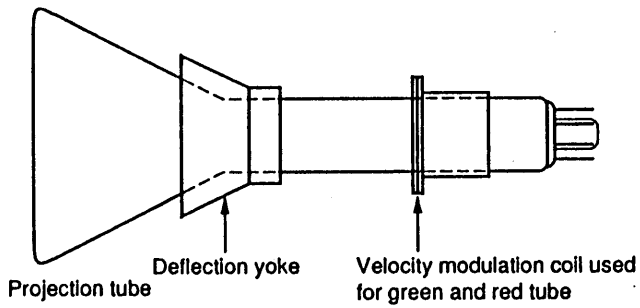


Fig. 1-1

2-1-2. Theory of Operation

As component parts of the neck of the projection tube, there are (1) deflection yoke (consisting of main yoke, sub-yoke, centering magnet) and (2) velocity modulation coil provided.

The main yoke of the deflectin yoke is composed of horizontal and vertical deflection yokes that turn light beam horizontally and vertically respectively.

The sub-yoke is called the convergence yoke, which is composed of horizontal and vertical coils. The sub-yoke functions to adjust distortion and coloring of picture with regulating current supplied from the convergence output circuit.

The centering magnet that is composed of bipolar magnets and installed behind the deflection yoke functions to adjust picture position in the screen.

The velocity modulation coil functions to make the picture clear by modulating deflection velocity.

2-1-3. Projection Tube

The flourescent screen is concavely curved with a radius of 350 mm. This concave gathers light beams in edge portions in the direction of the optical axis for efficient use of the quantity of light of the projection tube.

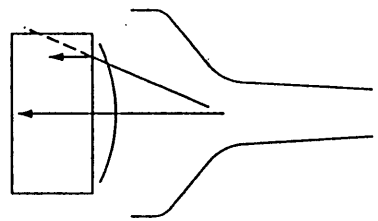


Fig. 1-2

Electrostatic focus

Parabolic waveform voltage applied to the FOCUS terminal in the horizontal and vertical periods gets the picture to be in focus uniformly in the center and edge portions of the screen.

The velocity modulation circuit is additionally installed to make the picture clearer.

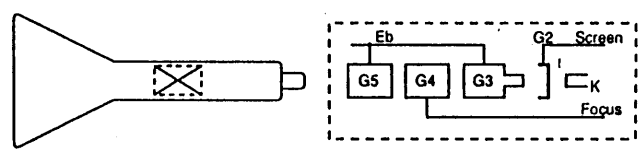


Fig. 1-3

2-2. FUNCTIONS OF MAIN COMPONENTS

2-2-1. Outline

The optical system of the P4100U(J) is mainly composed of the screen, the lens and the projection tube.

The distance between the flourescent screen of the projection tube and the screen is 814.6 mm.

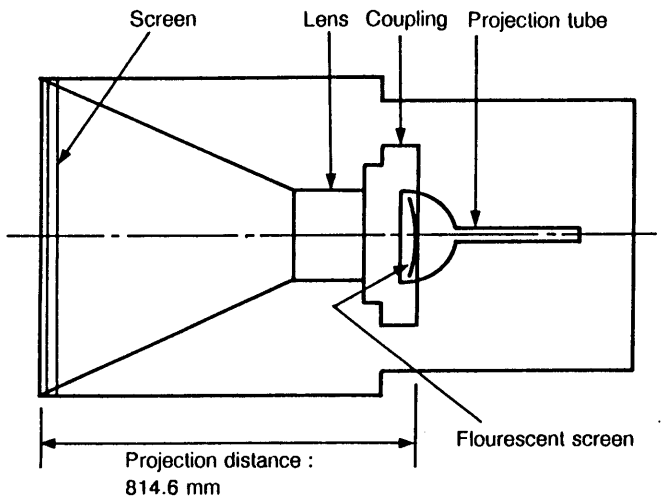


Fig. 2-1

2-2-2. Theory of Operation

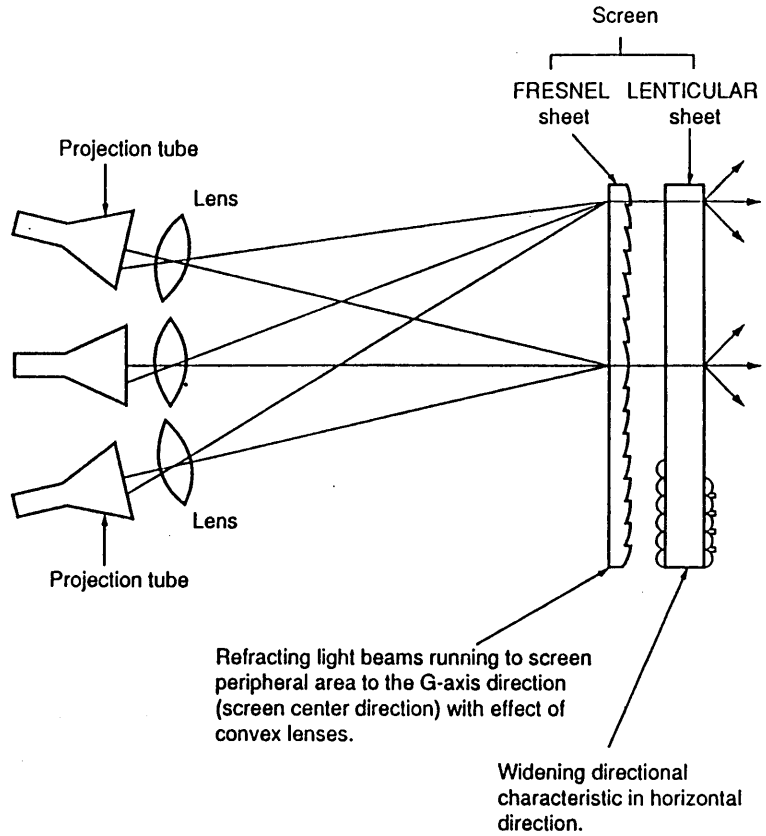


Fig. 2-2

2-3. SCREEN

2-3-1. Effect of Flesnel Sheet

Concaves and convexes that are concentrically arranged on the audience side of the Flesnel sheet have the same effect as convex lenses, and the uneven surface turns refracted rays nearly in parallel with the normal illumination direction to the screen even not only for the center part of the screen but also for the edge portions. This effect results from the focal length of the Flesnel lens so that it is designed to fucus on the emission pupil of the lens.

Moreover, the other side of the Flesnel sheet toward the projection lens has horizontally parallel fine unnevenness called the vertical lenticule, which has an effect on vertical expansion of light beam.

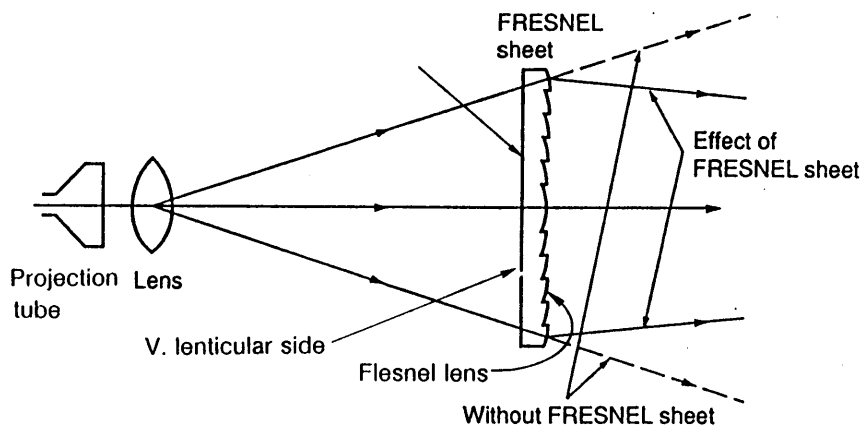


Fig. 2-3

In a video projection system that employs one Flesnel sheet, rays in the edge portions of the screen are generally refracted in the direction of the optical axis. However, this projection system refracts rays to be parallel with the optical axis to remove luminance difference from the neighboring screens for other sets since this system uses multiple Flesnel sheets.

2-3-2. Outward Appearance of Lenticular Sheet

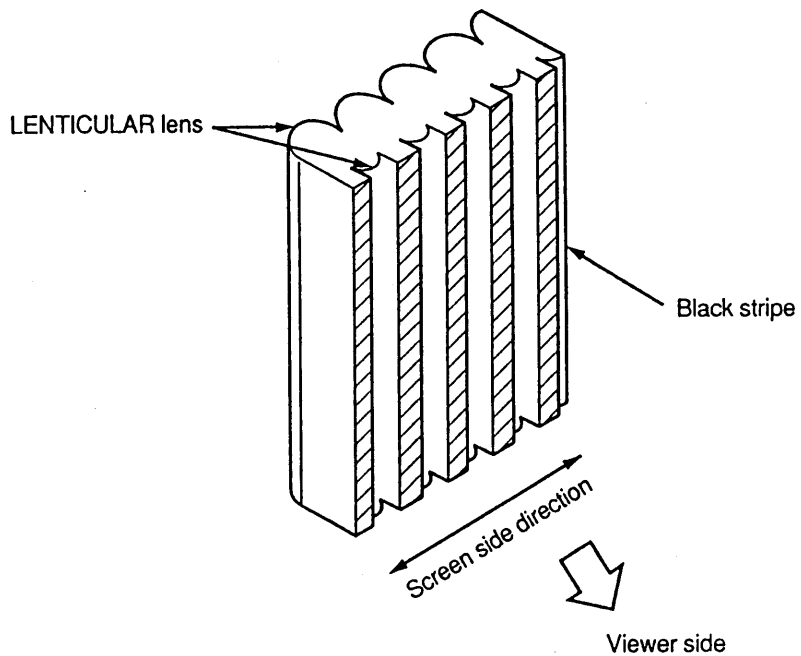


Fig. 2-4

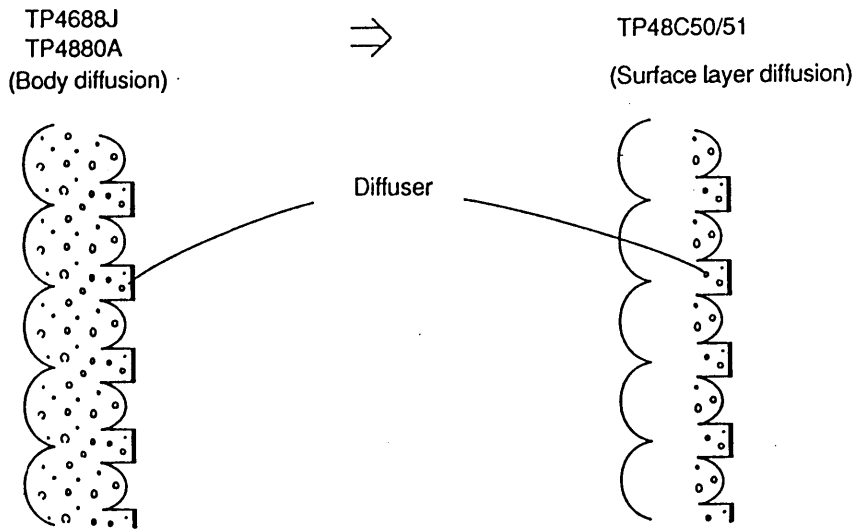


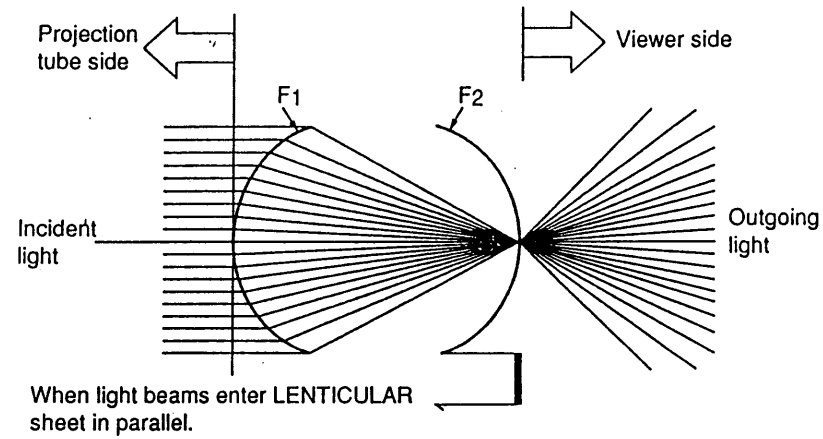
Fig. 2-5

Light beams are gathered in diffusers on the layer surface for efficient illumination, and the luminance is consequently raised by 10 % approximately.

The P4100U(J) employs the lenticular sheet for surface diffusion.

2-3-3. Effect of Lenticular Sheet

The lenticular sheet is effective to diffuse rays that are obliquely applied to the screen similarly to rays irradiated to the screen at a right angle when the screen is viewed from the front.



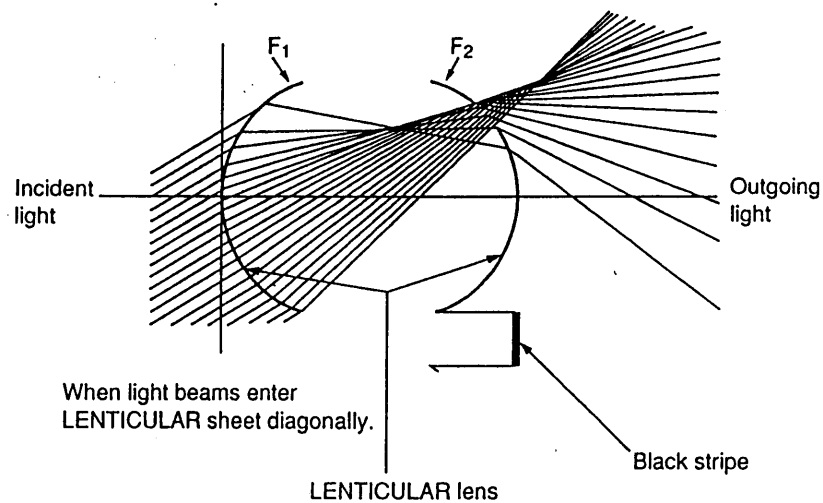


Fig. 2-6

2-4. EFFECT OF OPTICAL COUPLING

If something (liquid) having a refractive index similar to that of glass fills between the projection tube and the lens, it reduces reflection of rays in the boundary and accordingly improves contrast and loss in quantity of light.

Moreover, such a liquid not only raises the power of the projection tube by its cooling effect but also prevents the surfaces of the projection tube and the lens from getting dust.

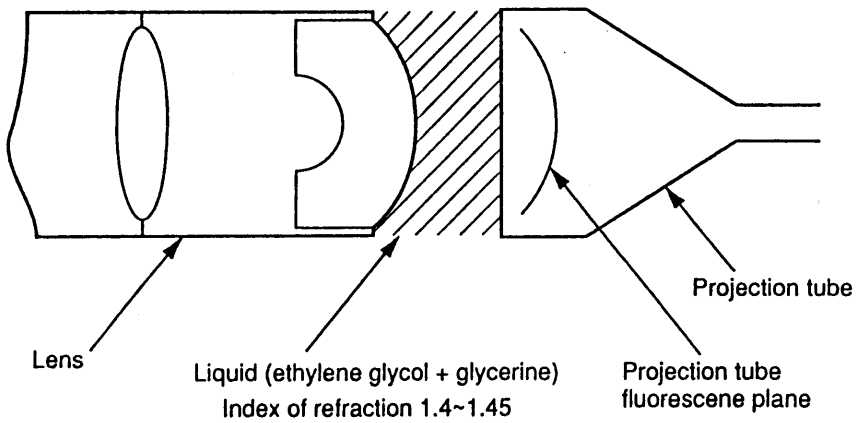


Fig. 2-7

2-5. LENS

The optical system that are mainly composed of the main lens, concave lens, concave fluorescent screen and projection tube realizes the lens system of a short focal length.

Thanks to the short focal length of the the lens system, the projection unit can be designed remarkably thin and compact.

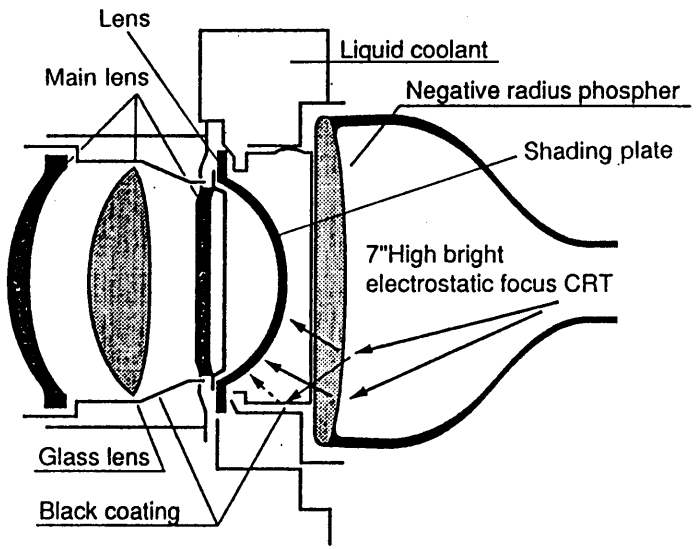


Fig. 2-8

2-5-1. Shading Plate

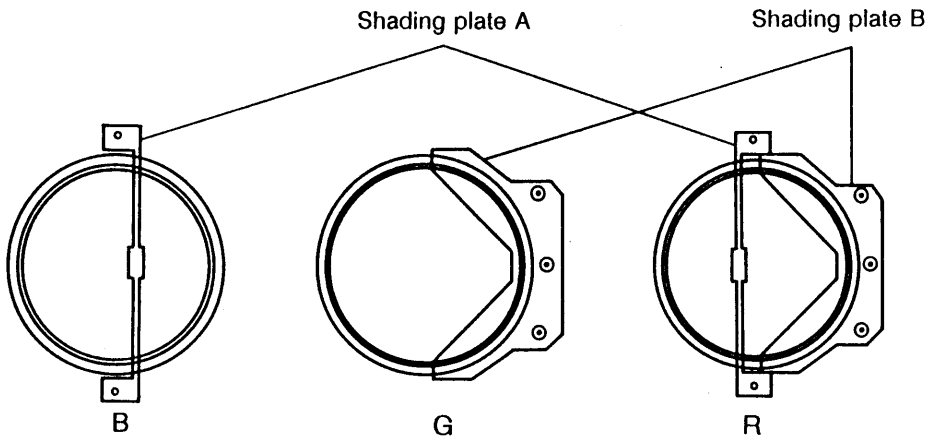


Fig. 2-9 C lens and coupling block as viewed from the screen side (Main lenses are removed.)

Two kinds of shading plates (four shading plates in total) are inserted between the C lens (coupling) and the main lens for preventing picture from irregular coloring. Each shading plate is concaved 2 to 5 mm to the C lens side.

Don't remove any setscrew retaining the shading plate, otherwise coupling liquid leaks out.

2-5-2. Focus Adjustment

Focalization of the lens system can be adjusted according to the following procedure.

Loosen the setscrew and turn the lens slowly clockwise and counterclockwise to get the lens to come into the best focus on the screen. After this adjustment, tighten the setscrew to secure the lens not to go out of focus.

2-6. PRECAUTIONS ON REPLACEMENT OF LENS AND PROJECTION TUBE

When dismounting the main lens, only remove four setscrews (a main lens) retaining it. If any other screw is removed, coupling liquid will leak out.

When mounting the main lens again, loosen the focus adjusting screw and turn the main lens fully counterclockwise as viewed from the screen side beforehand.

The projection tube to be supplied as a service part is an assembly incorporating the C lens and coupling with coupling liquid sealed inside.

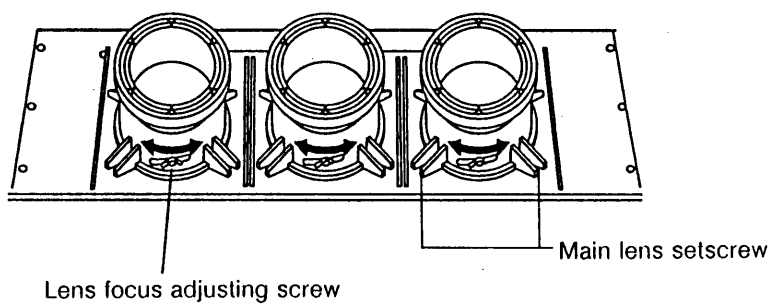


Fig. 2-10

SECTION 3.
MICROPROCESSOR

3-1. OUTLINE OF SYSTEM

The system microprocessor of the video wall projection unit (P4100U) is entirely newly designed under the developing concept of an easy maintenance program such as employment of external program ROM, structured notation, parts modularity, multi-filing system, and so on.

Main functions of the system microprocessor are processing of received remote control data, processing of transmission and reception of RS-232C data, processing of control inputs such as input data of key switches, processing of control outputs such as deflection system control output, video system control output, system control output, etc. besides processing of status holding by readout and write-in various regulating data from/to the nonvolatile memory.

The features of the system microprocessor are remarkable improvement in the precision and drastic time saving in adjustment as a result that the deflection control system can be adjusted by the external method (remote control) with the S/P controlled DAC replacing the conventional internal adjustment method (manual) with variable resistors.

For the P4100U, those adjustments can be performed with external control signals of the RS-232C standard, moreover, respective units can be controlled and adjusted individually or together even when they are connected in a multi-unit system.

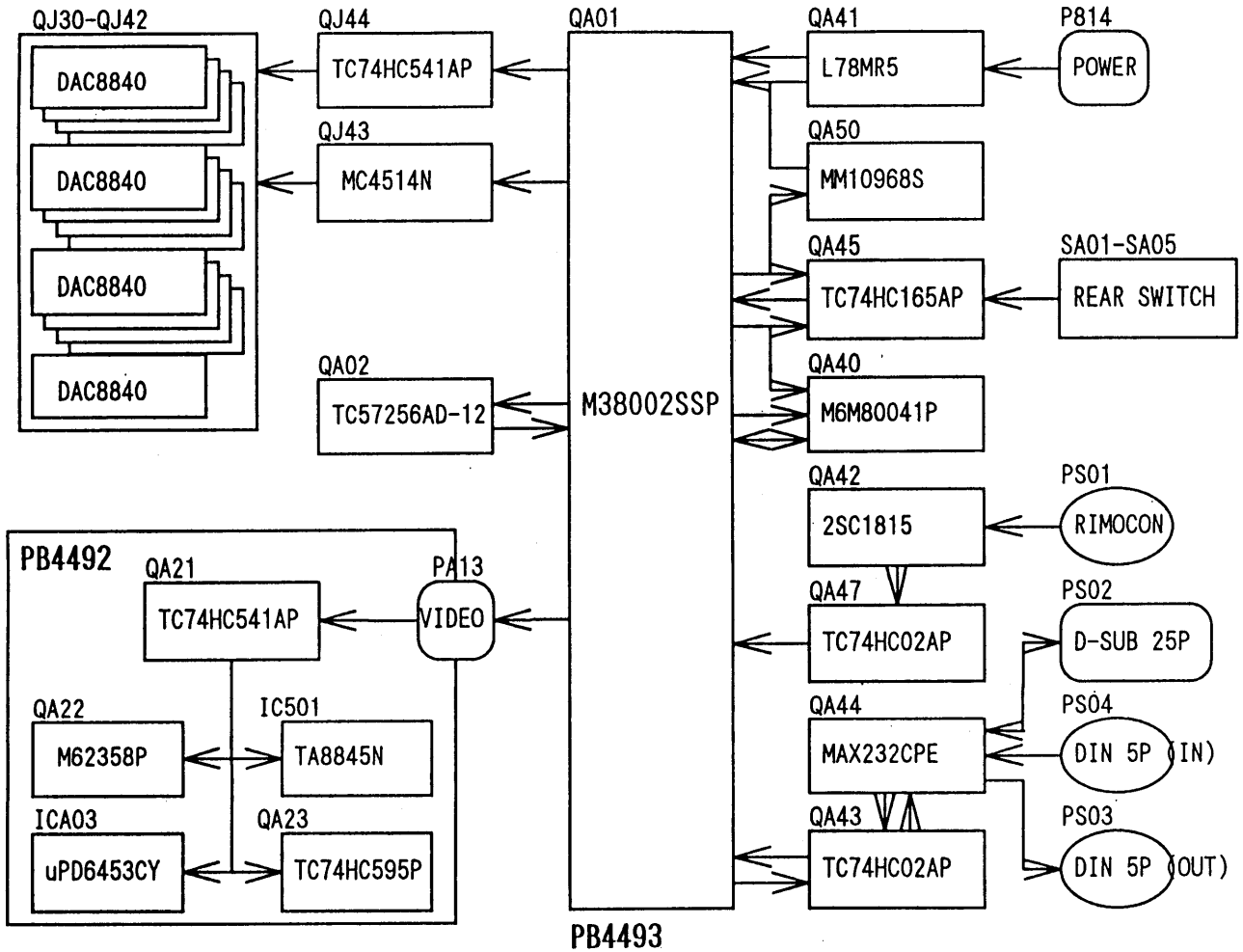


Fig. 3-1-1 System block diagram

3-2. SYSTEM MICROPROCESSOR

A Mitsubishi's 8-bit microcontroller (M38002SSP) is employed as the system microprocessor, QA01, which does not use the internal programming area but uses QA02 (Toshiba's EPROM, TC57256AD-12) as an external program ROM. As a result, change of the specifications of the system microprocessor and maintenance such as repair of bug are very easy.

As shown in Fig. 3-2-1 'Pin assignment of microprocessor' and Fig. 3-2-2 'Table of pin functions', the system microprocessor manages all inputs and outputs of control signals such as processings of remote control inputs, RS-232C inputs, adjustment data inputs and outputs, deflection system control signals, video system control signals, OSD display control signals, etc.

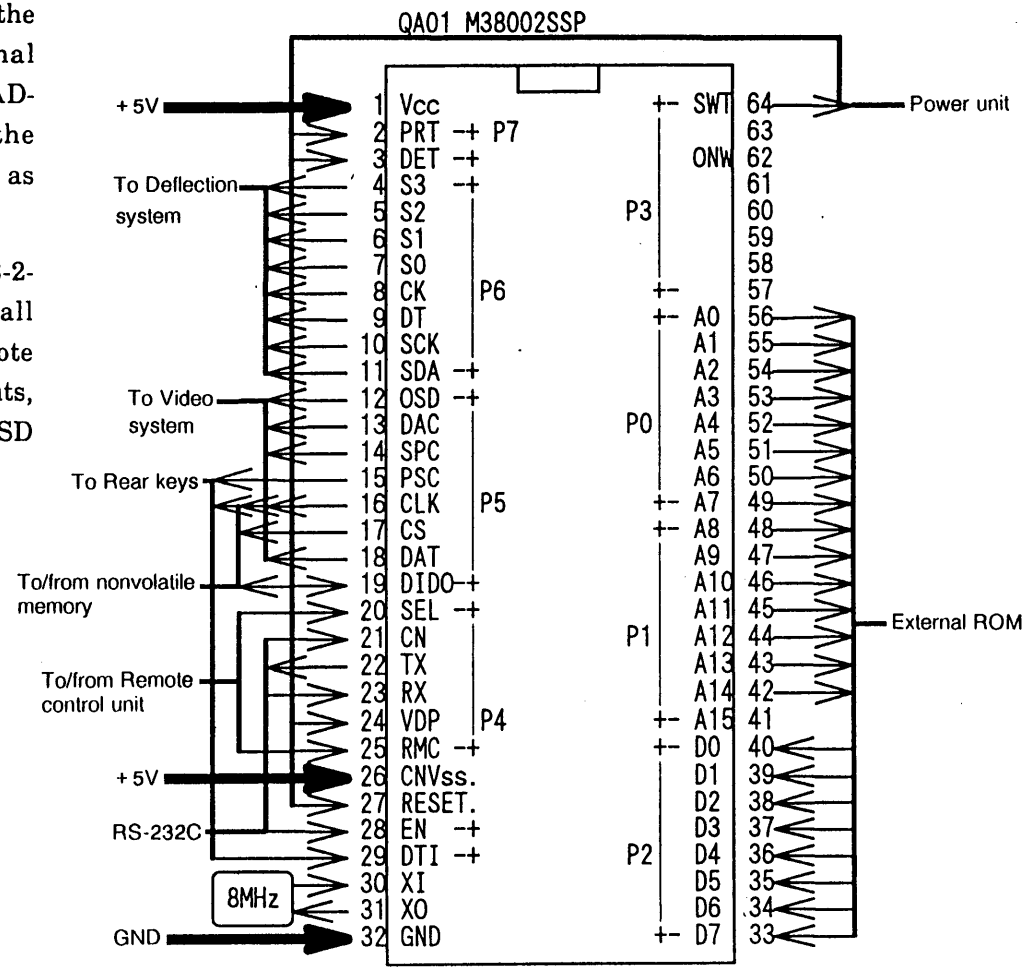


Fig. 3-2-1 Pin assignment of system microprocessor

Pin No.	Pin Name	Function	Input/ Output	Logic/Detail	Remark
1	Vcc	Power supply	Input	+5V	
2	PRT	Protect monitor input	Input	Detection at low level	Not connected
3	DET	Low voltage detection input	Input	Detection at low level	
4	S3	DAC8840 selection 3	Output	For deflection system	
5	S2	DAC8840 selection 2	Output	For deflection system	
6	S1	DAC8840 selection 1	Output	For deflection system	
7	SO	DAC8840 selection 0	Output	For deflection system	
8	CK	Clock for DAC8840	Output	For deflection system	
9	DT	Data for DAC8840	Output	For deflection system	
10	SCK	I2C clock for TA8845N	Output	For video adjustment	To video circuit
11	SDA	I2C data for TA8845N	Output	For video adjustment	To video circuit
12	OSD	uPD6453CY load	Output	For OSD	To video circuit
13	DAC	M62358P load	Output	For video adjustment	To video circuit
14	SPC	TC74HC595AP latch	Output	For video adjustment	To video circuit
15	PSC	TC74HC165AP load	Output	For fetch of rear key	
16	CLK	Common clock for devices	Output	Common clock	To video circuit

Pin No.	Pin Name	Function	Input/ Output	Logic/Detail	Remark
17	CS	M6M80041P chip selection	Output	For nonvolatile memory	
18	DAT	Common data for devices	Output	Common data	To video circuit
19	DIDO	Data for M6M80041P	Input/ Output	For nonvolatile memory	
20	SEL	Remote control selection	Input	For check of remote control insertion	Not connected
21	CN	RS-232C combination	Input	For check of system bus connection	
22	TX	RS-232C transmission data	Output	Data output for RS-232C	
23	RX	RS-232C reception data	Input	Data input for RS-232C	
24	VDP	VD pulse	Input	Vertical blanking pulse	Not connected
25	RMC	Reception data from remote controller	Input	Reception data for remote control	
26	CNVss	Operation mode setting	Input	External ROM operation with +5 V	
27	RESET	External reset	Input	Reset operation at low level	
28	EN	RS-232C enable	Output	Enable operation at low level	
29	DTI	Data for TC74HC165AP	Input	Data to fetch rear key	
30	XI	Oscillating input	Input		
31	XO	Oscillating output	Output	Generally connected with X'tal (8 MHz)	
32	GND	Ground	Input	+0V	

Fig. 3-2-2 Table of pin functions (1/2)

Pin No.	Pin Name	Function	Input/ Output	Logic/Detail	Remark
33	D7	Data for external ROM (MSB)	Input	Program data input	
34	D6	Data for external ROM	Input	Program data input	
35	D5	Data for external ROM	Input	Program data input	
36	D4	Data for external ROM	Input	Program data input	
37	D3	Data for external ROM	Input	Program data input	
38	D2	Data for external ROM	Input	Program data input	
39	D1	Data for external ROM	Input	Program data input	
40	D0	Data for external ROM (LSB)	Input	Program data input	
41	A15	Address for external ROM (MSB)	Output	Program data output	Not connected
42	A14	Address for external ROM	Output	Program data output	
43	A13	Address for external ROM	Output	Program data output	
44	A12	Address for external ROM	Output	Program data output	
45	D11	Address for external ROM	Output	Program data output	
46	A10	Address for external ROM	Output	Program data output	
47	A9	Address for external ROM	Output	Program data output	
48	A8	Address for external ROM	Output	Program data output	

Pin No.	Pin Name	Function	Input/ Output	Logic/Detail	Remark
49	A7	Address for external ROM	Output	Program data output	
50	A6	Address for external ROM	Output	Program data output	
51	A5	Address for external ROM	Output	Program data output	
52	A4	Address for external ROM	Output	Program data output	
53	A3	Address for external ROM	Output	Program data output	
54	A2	Address for external ROM	Output	Program data output	
55	A1	Address for external ROM	Output	Program data output	
56	A0	Address for external ROM (LSB)	Output	Program data output	
57		N. C	Output		Not connected
58		N. C	Output		Not connected
59		N. C	Output		Not connected
60		N. C	Output		Not connected
61		N. C	Output		Not connected
62	ONW	External waiting	Input	No waiting with +5 V	
63		N. C	Output		Not connected
64	SWT	Power switch	Output	Power on with +5 V	

Fig. 3-2-2 Table of pin functions (2/2)

3-3. POWER RESET BLOCK

As shown in Fig. 3-3-1 the power reset block employs a three-terminal regulator (L78MR5) with power reset function as the power IC, QA41, and a watchdog timer (MM10968S) as the reset IC, QA50.

The power IC QA41, which inputs +12 V DC power of standby power supply while outputs +5 V DC power, supplies reset signal to the system microprocessor QA01 on the timing shown in Fig. 3-3-2 "L78MR5 reset signal timing chart" when the power is on.

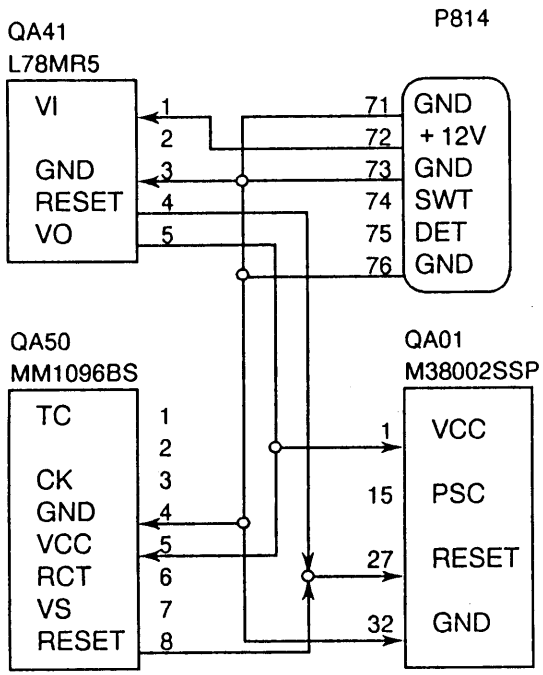


Fig. 3-3-1 Power reset block

The reset IC QA50 inputs load signal to fetch rear key (to be mentioned later) and, if there is no input of the load signal for about one second, it judges the system microprocessor QA01 is running away and supplies reset signal to the system microprocessor QA01 on the timing shown in Fig. 3-3-3 "MM1096BS reset signal timing chart".

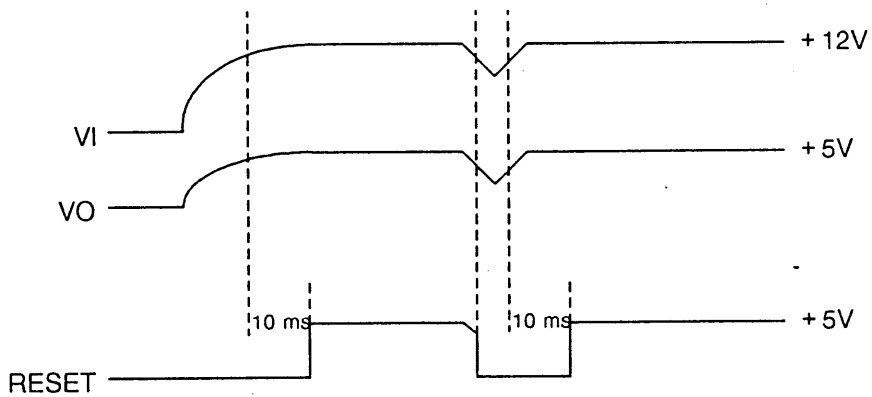


Fig. 3-3-2 L78MR5 reset signal timing chart

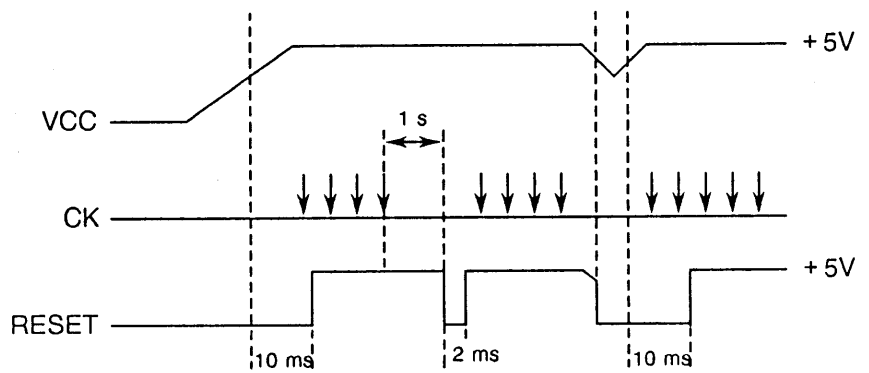


Fig. 3-3-3 MM1096BS reset signal timing chart

3-4. REMOTE CONTROL RECEIVER BLOCK

In the remote control receiver block the transistor QA42 (2SC1815) converts remote control signal of 3 V level supplied from the remote control unit (accessory, CT-) that is connected with the remote terminal as shown in Fig. 3-4-1 into 5 V level signal. This signal is supplied through the noise elimination filter to the buffer QA47 (TC74HC02AP) for shaping waveform, and then supplied to the system microprocessor QA01 on the timing shown in Fig. 3-4-2 "Timing chart of reception signal from remote control unit".

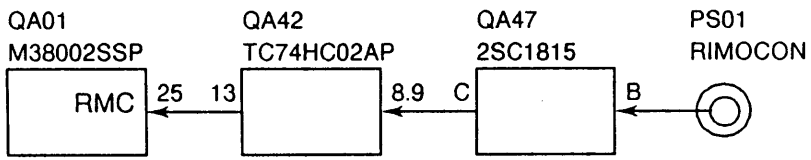


Fig. 3-4-1 Remote control receiver block

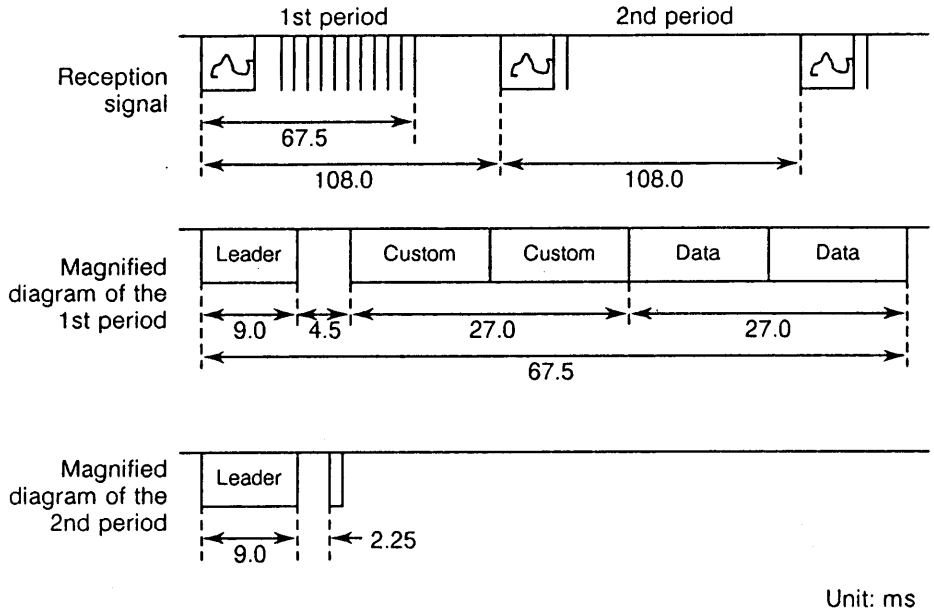


Fig. 3-4-2 Timing chart of reception signal from remote control unit

3-5. RS-232C SIGNAL TRANSMITTER/ RECEIVER BLOCK

In the RS-232C signal transmitter/receiver block, RS-232C signal that is input through the RS-232C connector (D-SUB 25-pin) PS02 or input through the system bus input connector (DIN 5-pin) PS04 on the timing shown in Fig. 3-5-2 (see Fig. 3-5-1, too) is selected by passing either input signal through QA44 of the DC/DC converter for RS-232C (MAX232CPE) and QA43 of the deta selector (TC74HC02AP), and the selected signal is supplied to the system microprocessor QA01.

This RS-232C signal is controlled by QA01 and then supplied to the system bus output connector PS03 (DIN 5-pin).

For identify management of respective systems, enable signal is controlled to output or not to output RS-232C signal input, in other words, if the signal has the identity number (to be described later), it will be output as it is; or, if it has no identity number, it will not be output.

Fig. 3-5-2 is just an example of communication conditions in which signaling speed is 9600 bps, bit pulse length is 8 bits, and stop bit is 1, without parity bit.

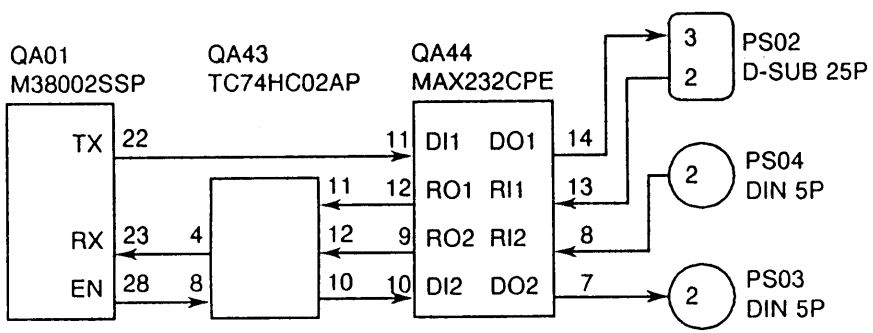
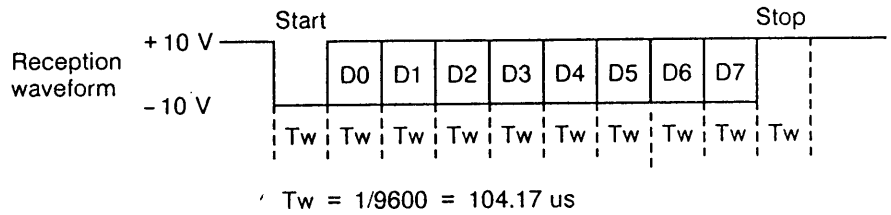


Fig. 3-5-1 RS-232C signal receiver block



Communication conditions:
9600 bps, 8 bits pulse length, 1 stop bit, without parity

Fig. 3-5-2 RS-232C signal timing chart

3-6. REAR KEY FETCH BLOCK

As shown in Fig. 3-6-1 "Rear key fetch block", the P/S of QA45 (TC74HC165AP) of the rear key fetch block holds the operation status of respective rear keys with input data from SA01 to SA05 as well as that of the power switch with input data from PA12 of the video unit. The system microprocessor QA01 fetches those status holding data on the timing shown in Fig. 3-6-2 "TC74HC165AP timing chart". In concrete, data fetch is performed at a certain interval (every 10 ms) in the steady state besides at the initialization by turning on the AC power supply. Therefore, the power can be turned on or off with the power switch instantly (1 sec later in actual operation).

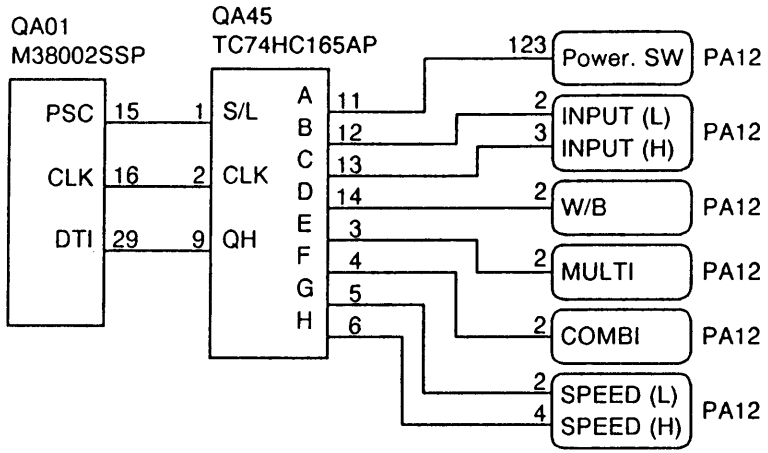


Fig. 3-6-1 Rear key fetch block

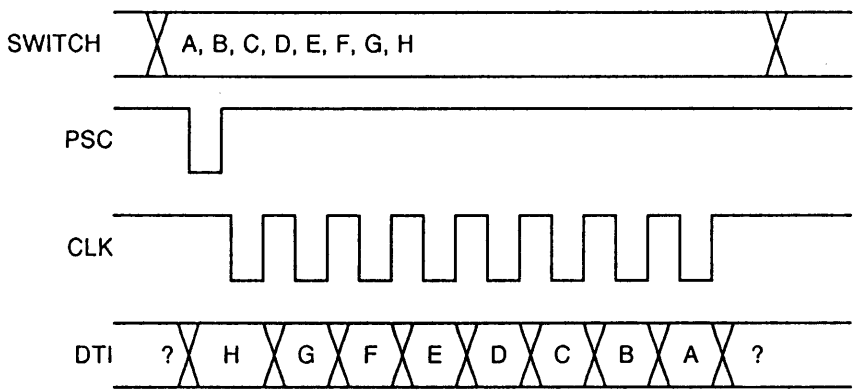


Fig. 3-6-2 TC74HC165AP timing chart

3-7. NONVOLATILE MEMORY BLOCK

In the nonvolatile memory block employs the nonvolatile memory QA40 (M6M80041P) to store various regulating data as shown in Fig. 3-7-1.

When power is on (AC on), the system microprocessor QA01 reads all regulating data out of the memory on the timing shown in Fig. 3-7-2(A) "Read timing chart" to hold the previously regulated status. When writing regulating data in the memory, the system microprocessor QA01 writes all regulating data on the timing shown in Fig. 3-7-2(B) "Write timing chart" to store all current data for holding the present regulating status.

However, if something faulty (momentary power failure, etc.) occurs in writing regulating data, there is possibility to write data erroneously. To avoid such error in writing data, the initial data stored in the system microprocessor QA01 are read out and written in the memory when any error in data writing is detected.

Fig. 3-7-3 illustrates the nonvolatile memory map used for the system microprocessor.

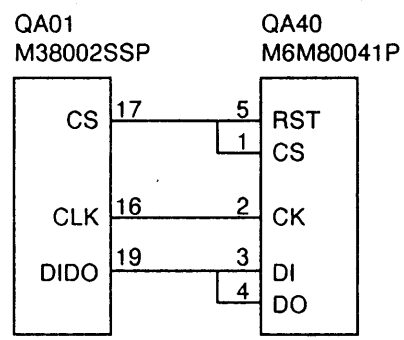
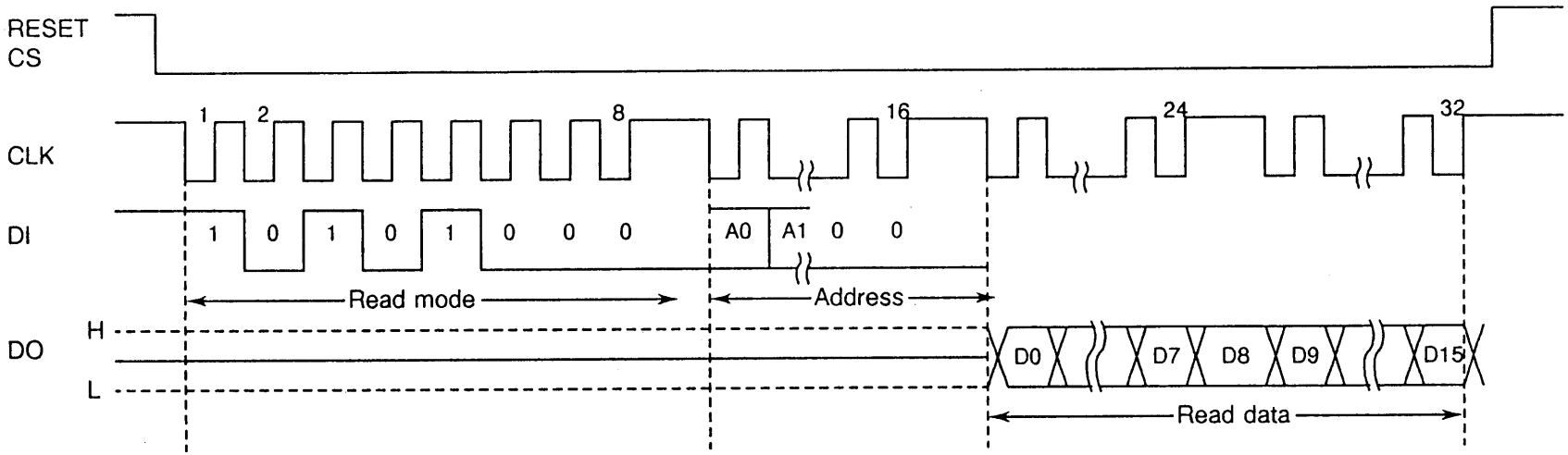
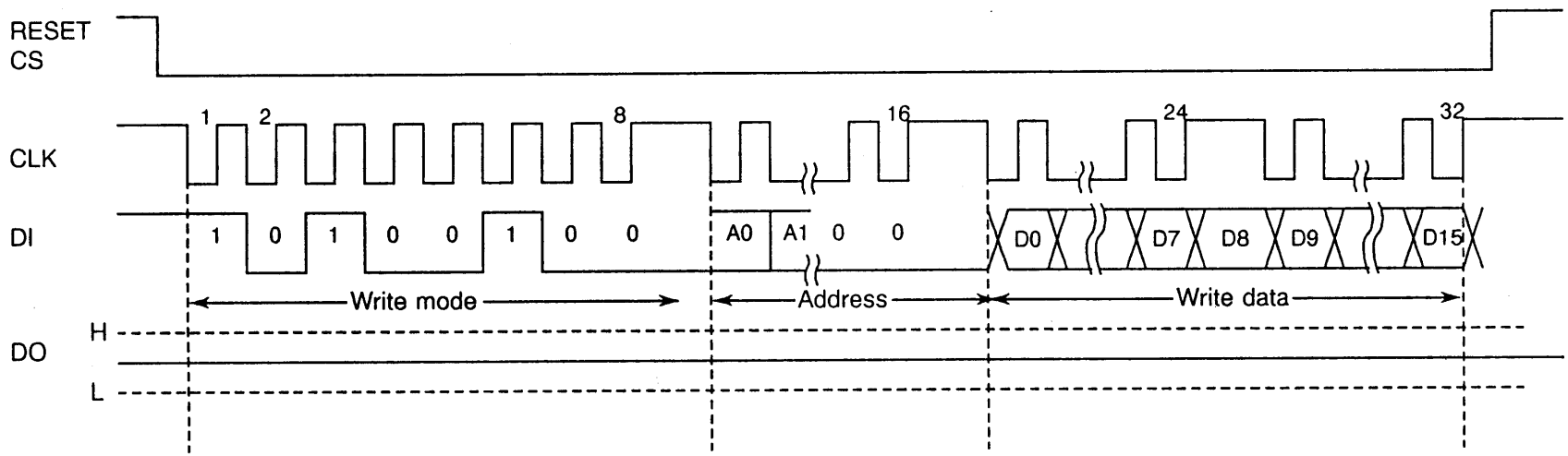


Fig. 3-7-1 Nonvolatile memory block



(A) Read timing chart



(B) Write timing chart

Fig. 3-7-2 Write/read timing chart of nonvolatile memory

Address	LSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	MSB 15
00	Video (TA8845N)										Drive (1/2)			Cut off (1/2)		
10	Video (M62358P)								ID							
20	R-H deflection (DAC8840)								R-V deflection (DAC8840)							
30	B-H deflection (DAC8840)								B-V deflection (DAC8840)							
40	G-H deflection (DAC8840)								G-V deflection (DAC8840)							
50	Video (DAC8840)															
60																
70																

Fig. 3-7-3 Nonvolatile memory map

3-8. DEFLECTION SYSTEM CONTROL BLOCK

In the deflection system control block, the line decoder QJ43 (MC4514N) outputs load signals while the buffer QJ44 (TC74HC541AP) outputs clock and data signals to control respective deflection system control DACs QJ30 to QJ42 (DAC8840) as shown in Fig. 3-8-1.

Those signals are used to hold the previous status in reading all regulating data as the power is on, while they are used to recover abnormal data if there occurs something faulty such as noise in output signal in the refresh processing (regular data output processing).

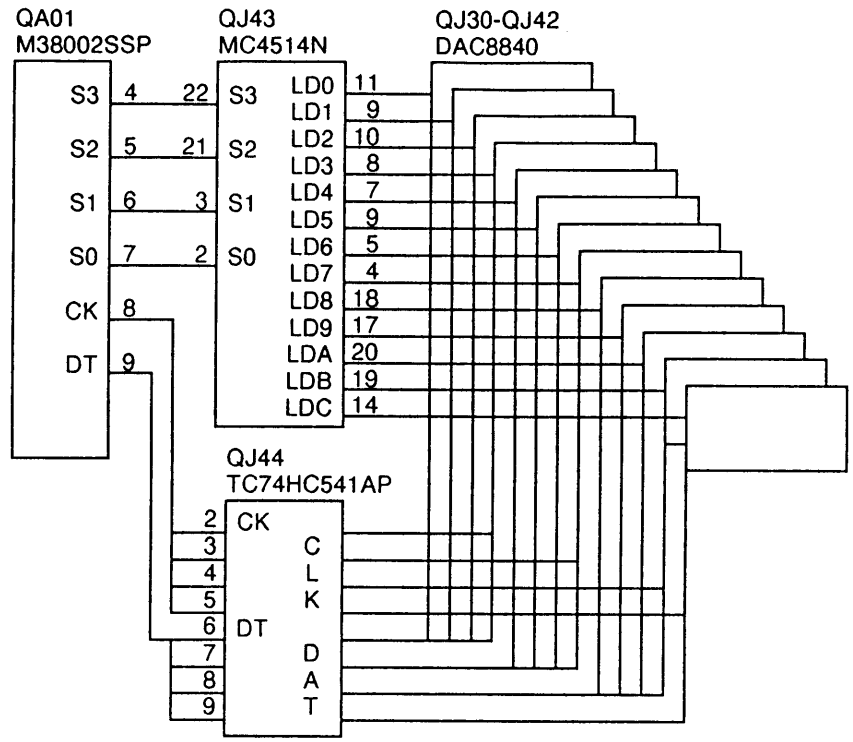


Fig. 3-8-1 Deflection system control block

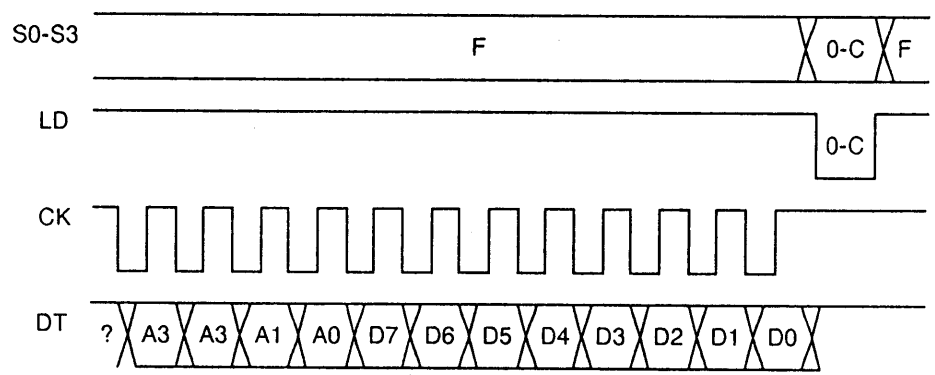


Fig. 3-8-2 DAC8840 timing chart

3-9. VIDEO SYSTEM CONTROL BLOCK

In the video system control block, various control signals are supplied through the buffer QA21 (TC74HC541AP) to the following control ICs as shown in Fig. 3-9-1 "Video system control diagram".

(1) QA23 (TC74HC595AP), an S/P for the selector, generates signals to switch input signals and test signals on the timing shown in Fig. 3-9-2 "TC74HC595AP timing chart".

(2) QA22 (M62358P) of a serial control DAC generates mode switching signal and regulating signal for the video system on the timing shown in Fig. 3-9-3 "M62358P timing chart".

(3) ICA03 (μPD6453CY-514) of the OSD display IC, which is supplied with control signal on the timing shown in Fig. 3-9-2 "μPD6453CY timing chart", generates on-screen character display signal on the timing determined by a free-running frequency according to a V. or H. pulse that is also supplied to QA22.

(4) IC501 (TA8845N) of the video control LSI generates various video regulating signals on the timing shown in Fig. 3-9-4 "TA8845N timing chart".

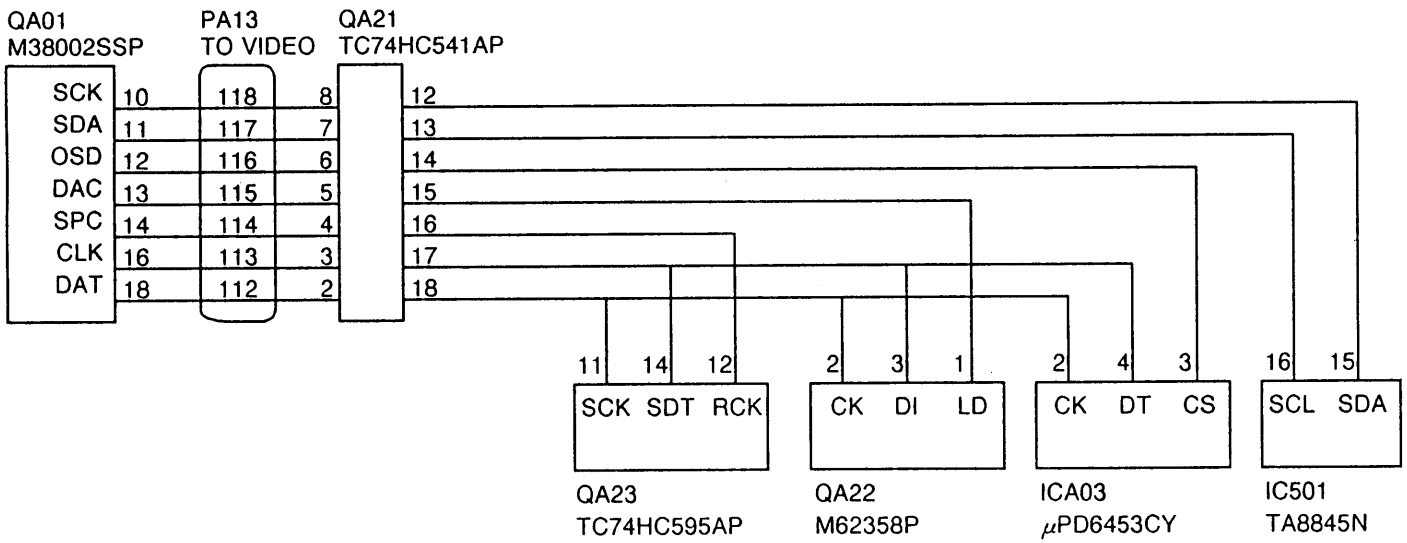


Fig. 3-9-1 Video system control diagram

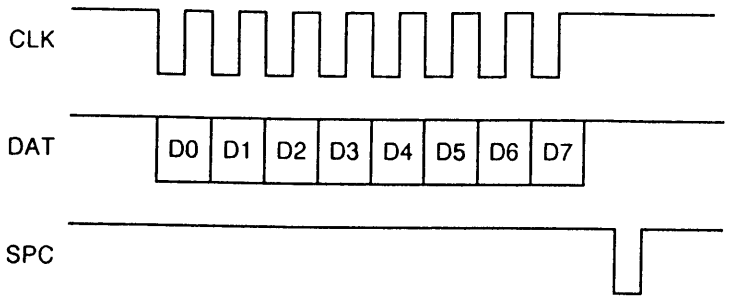


Fig. 3-9-2 TC74HC595P timing chart

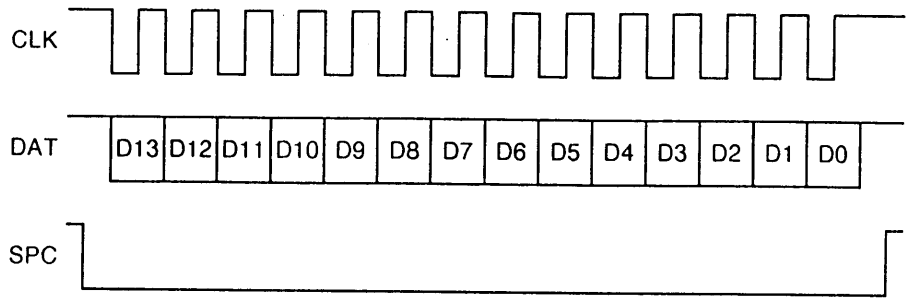


Fig. 3-9-3 M62358P timing chart

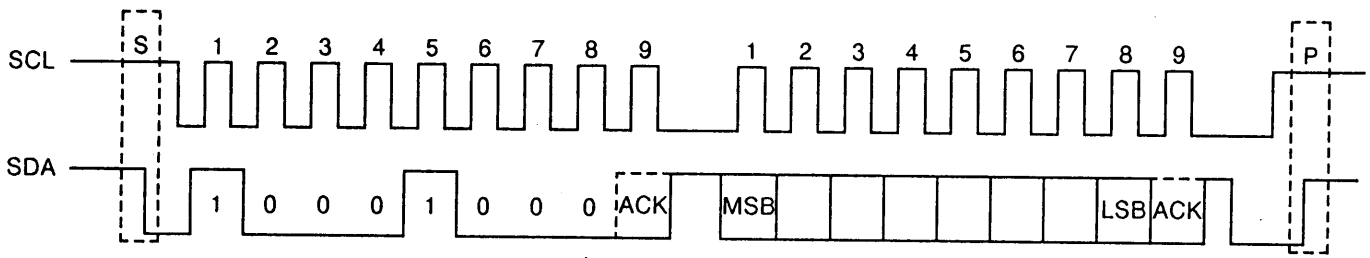


Fig. 3-9-4 TA8845N timing chart

3-10. POWER SOURCE INTERLOCKING MODE

The power source interlocking mode means the status that the power to be supplied to this system is turned on or off interlocking with power on/off operation of the system at the previous stage when multiple systems are connected in daisy chain.

For effectuating the power source interlocking mode in such a multi-system connection as shown in Fig. 3-10-1, only the system at the front of the multi-system connection must be turned on with its power switch on the rear panel set to the "on" position (depressed status), and the other systems following in the connection must be set in the standby mode (power switch is not depressed). In this interlocking setup, the systems following the first system are turned on/off 1 second behind on/off operation of the first system.

When the following systems are set in the standby mode, keep it in mind that they cannot be turned on or off externally by the remote control unit or the RS-232C interface, because the standby mode is provided only for the power source interlocking mode in which the following systems are turned on/off only by the power source interlocking signal.

Moreover, if respective systems need individual operation, set their power switch to the on position, since all the systems are operated as same as the first system in the power source interlocking on mode.

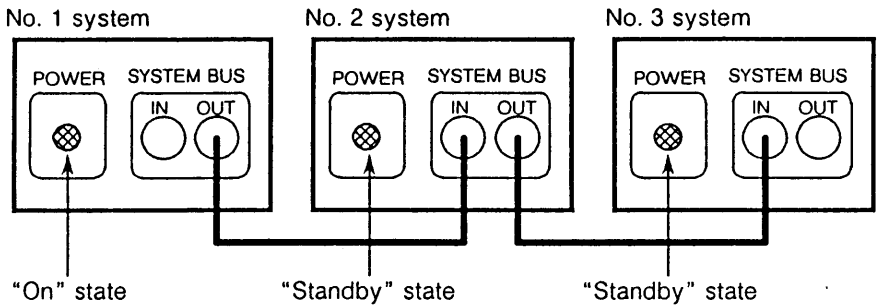


Fig. 3-10-1 Multi-system connection

3-11. SYSTEM CONTROL MODES

There are some system control modes prepared for operation of this system.

As shown in Fig. 3-11-1, the state transition of the system control modes starts with the "initialization mode" just after the AC power on, and then transfers to the "normal mode". After the normal mode, the state transfers to the "adjustment (ADJUST) mode" that is classified into the "auxiliary (AUX) mode" and the "special mode".

In the initialization mode, the stored data of the rear keys status are read out of the nonvolatile memory besides the last regulating data, and the systems are set in the same operation status as previously done according to the readout data. At the same time, when the power switches are switched on, the systems are set in the "on" state of the normal mode, or, when the power switches are set to standby mode, the systems are set in the "off" state of the normal mode.

In the "off" state of the normal mode, the systems accept the power-on operation only to be ready to transfer to the "on" state of the normal mode. From the "on" state of the normal mode, the systems can be transferred to the "off" state of the normal mode or to the adjustment mode by making choice of the adjustment mode. When the systems are transferred to the adjustment mode, the AUX mode or the special mode is directly selectable besides the general adjustment mode.

Fig. 3-11-2 is a table of control items operable in relating control modes, while Fig. 3-11-3 shows an outward appearance of the optional remote control unit (CT-9720).

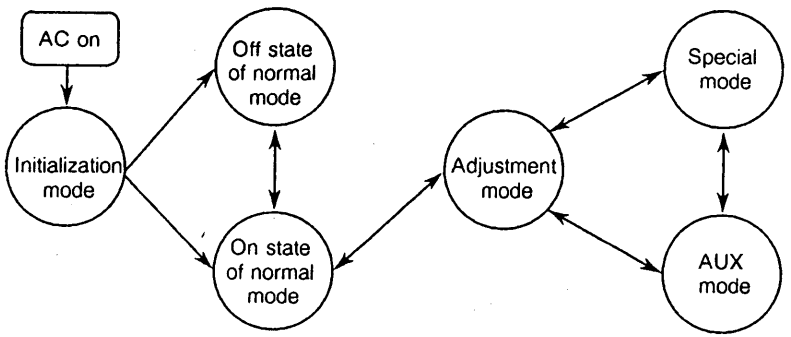


Fig. 3-11-1 Control mode transition diagram

Control			Mode				Command			
Item	Sort	Detail	Normal	Adjust	AUX	Special	Remote control	unit	RS-232C	
POWER	MODE	Power on/off	○				$40	PON	POF	
CALL	MODE	Display mode on/off	○				$41	DON	DOF	
ADJUST	MODE	Adjustment mode on/off	○				$42	AJY	AJN	
VIDEO	MODE	Video input selection	○				$43	IN1		
Y/C	MODE	Y/C input selection	○				$44	IN2		
RGB	MODE	R/G/B input selection	○				$45	IN3		
COMBI	MODE	Combination on/off	○				$46	CBY	CBN	
MULTI	MODE	Multi-mode on/off	○				$47	MMY	MMN	
W/B	MODE	White balance 1/2	○				$48	WB1	WB2	
UP	ADJUST	Vertical increment of adjustment value		○			$18	VLP		
DOWN	ADJUST	Vertical decrement of adjustment value		○			$19	VDW		
LEFT	ADJUST	Horizontal decrement of adjustment value		○			$1A	VLF		
RIGHT	ADJUST	Horizontal increment of adjustment value		○			$1B	VRG		
SPEED	ADJUST	Adjustment value increment-decrement rate switching		○			$1C	VSP		
STANDARD	ADJUST	Not connected		○			$1D	VST		
WRITING	ADJUST	Adjustment value write selection		○			$1E	VWR		
CONTRAST	VIDEO	Contrast selection		○			$50	CNT		
BRIGHT	VIDEO	Brightness selection		○			$51	BRT		
COLOR	VIDEO	Color selection		○			$52	COL		
TINT	VIDEO	Tint selection		○			$53	TIN		
SHARP	VIDEO	Sharpness selection		○			$54	SHP		
ABL	VIDEO	ABL selection		○			$55	ABL		
CUTOFF	VIDEO	Cutoff selection		○			$57	LOW		
DRIVE	VIDEO	Drive selection		○			$58	HIG		
TEST	VIDEO	Test signal selection (OFF/1/2)		○			$56	TOF	TS1	TS2

Fig. 3-11-2 Control items by mode (1/3)

Control			Mode				Command			
Item	Sort	Detail	Normal	Adjust	AUX	Special	Remote control unit	RS-232C		
R-ON/OFF	ON/OFF	Raster R on/off		○			$15	RON	ROF	
G-ON/OFF	ON/OFF	Raster G on/off		○			$16	GON	GOF	
B-ON/OFF	ON/OFF	Raster B on/off		○			$17	BON	BOF	
R-SEL	SELECT	Raster R selection		○			$12	SLR		
G-SEL	SELECT	Raster G selection		○			$13	SLG		
B-SEL	SELECT	Raster B selection		○			$14	SLB		
L SIZ	H&V	For detail, refer to description of deflection system adjustment.		○			$80	ISZ		
Q SIZ	H&V	For detail, refer to description of deflection system adjustment.		○			$81	OSZ		
L LIN	H&V	For detail, refer to description of deflection system adjustment.		○			$82	ILN		
Q LIN	H&V	For detail, refer to description of deflection system adjustment.		○			$83	OLN		
Q PIN	H&V	For detail, refer to description of deflection system adjustment.		○			$84	OPN		
Q SPIN	H&V	For detail, refer to description of deflection system adjustment.		○			$85	OSP		
Q KEY	H&V	For detail, refer to description of deflection system adjustment.		○			$86	OKY		
Q SKEY	H&V	For detail, refer to description of deflection system adjustment.		○			$87	OSK		
TILT	H&V	For detail, refer to description of deflection system adjustment.		○			$88	TLT		
BOW	H&V	For detail, refer to description of deflection system adjustment.		○			$89	BOW		
STATIC	H&V	For detail, refer to description of deflection system adjustment.		○			$8A	STC		
L PIN	H	For detail, refer to description of deflection system adjustment.		○			$92	IPN		
L LIN	H	For detail, refer to description of deflection system adjustment.		○			$90	LLN		
R LIN	H	For detail, refer to description of deflection system adjustment.		○			$91	RLN		
L PIN	H	For detail, refer to description of deflection system adjustment.		○			$94	LPN		
CORNER	V	For detail, refer to description of deflection system adjustment.		○			$95	COR		
WING	V	For detail, refer to description of deflection system adjustment.		○			$96	WNG		
L KEY	V	For detail, refer to description of deflection system adjustment.		○			$98	IKY		
I SKEY	V	For detail, refer to description of deflection system adjustment.		○			$99	ISK		
WAVE	V	For detail, refer to description of deflection system adjustment.		○			$9A	WAV		
S WAVE	V	For detail, refer to description of deflection system adjustment.		○			$9B	SWV		

Fig. 3-11-2 Control items by mode (2/3)

Control			Mode				Command			
Item	Sort	Detail	Normal	Adjust	AUX	Special	Remote control unit	RS-232C		
AUX14	ADJUST	AUX mode on/off		○			$97	AUX		
SPECIAL	ADJUST	Special mode on/off		○			$93	–		
ID. CLR	DATA	Identity erasure (In case of remote control: "..")		○			$10	IDC		
ID. SET	DATA	Identity setting (In case of remote control: "99")		○			$11	IDS		
0	DATA	Effective in "Special mode"				○	$00	–		
1	DATA	Effective in "AUX mode" or "Special mode"			○	○	$01	SHV		
2	DATA	Effective in "AUX mode" or "Special mode"			○	○	$02	SHA		
3	DATA	Effective in "AUX mode" or "Special mode"			○	○	$03	SHB		
4	DATA	Effective in "AUX mode" or "Special mode"			○	○	$04	OSD		
5	DATA	Effective in "AUX mode" or "Special mode"			○	○	$05	MNT		
6	DATA	Effective in "Special mode"				○	$06	–		
7	DATA	Effective in "Special mode"				○	$07	–		
8	DATA	Effective in "Special mode"				○	$08	–		
9	DATA	Effective in "Special mode"				○	$09	–		
A	DATA	Not connected					$0A	–		
B	DATA	Not connected					$0B	–		
C	DATA	Not connected					$0C	–		
D	DATA	Not connected					$0D	–		
E	DATA	Not connected					$0E	–		
F	DATA	Not connected					$0F	–		

Fig. 3-11-2 Control items by mode (3/3)

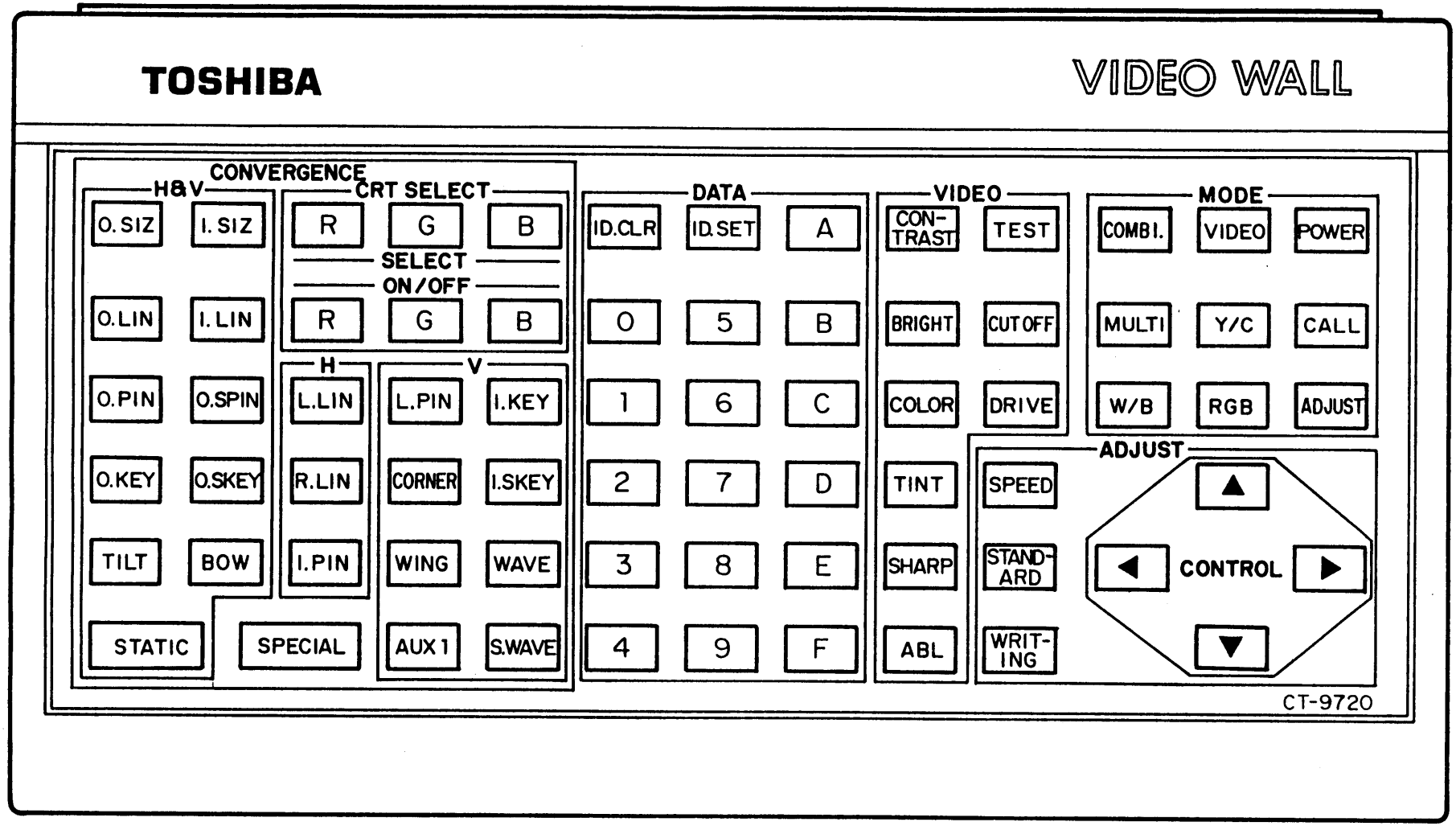


Fig. 3-11-3 Outward appearance of remote control unit

3-12. SYSTEM CONTROL BY RS-232C INTERFACE

The following explains the external control method by RS-232C interface.

The signal connection is a straight-line coding through PS02 of the RS-232C connector as shown in Fig. 3-12-1.

Pin No.	Signal name	Detail of signal	Input/Output
1	F. G	Frame ground	Input
2	RX	Reception data	Input
3	TX	Transmission data	Output
7	S. G	Signal ground	Input

Fig. 3-12-1 RS-232C connection conditions

Communication conditions should be set as shown in Fig. 3-12-2. For transmission rate, set the speed selector switch on the rear panel of the main unit to "0", "1", "2" or "3" as required; namely, setting to "0" for 1200 baud, "1" for 2400 baud, "2" for 4800 baud and "3" for 9600 baud.

Communication condition	Detail of condition
Communication method	Transmission rate: 1200, 2400, 4800, 9600 baud Parity bit: None, Data bit: 8 bits, Stop bit: 1 bit
Communication format	7-bytes of "STX (1 byte) + IDT (2 bytes) + CMD (3 bytes) + EXT (1 byte)" is regarded as a signal block. In the above description, STX is 02 h, ETX is 03 h, IDT is Arabic numerals (0 to 9) and asterisk (*), and CMD is RS-232C command characters listed in Fig. 3-11-2. For inputting CMD, do in capital letters.

Fig. 3-12-2 RS-232C communication conditions

Identity numbers that identify respective systems hooked up in the multi-system connection enable the operator to operate the systems individually or together with at the same time.

Identification can be done with couples of two numerals (0 to 9), and it is theoretically possible to register 100 identity numbers from 00 to 99. However, it is advised not to use "00" as an identity number.

For convenience of multi-system operation, it is recommended to use the asterisk (*) key for a numeral key, since the asterisk represents all numerals in the same place as it is input; for example, if "*2" is input for identification, the identity numbers of "02", "12", ..., "92" are subject to operation, or, if "3*" is input, the identity numbers of "30", "31", ..., "39" are subject to operation.

When transmitting commands, make sure to take an interval of 100 ms at least between two commands. If interval between two commands is too short, it may result in failure in operation owing to misrecognition of the commands.

SECTION 4.
VIDEO CIRCUIT

4-1. OUTLINE OF VIDEO CIRCUIT

The video circuit operates in switching of input signals, Y/C separation and video chroma processing. Moreover, it performs shading correction (luminance adjustment and irregular color correction), AKB processing and ABL interlocking. Fig. 4-1-1 shows a block diagram of the video circuit.

Composite video signal input to the video circuit is separated into Y (luminance) signal and C (chrominance) signal by the digital comb filter. The Y/C separated video signals are supplied to the V/C/D IC through the signal switcher which switches between the Y/C-separated video signals and externally input Y and C signals. RGB signals are directly input to the V/C/D IC which switches between them and other RGB signals converted from the Y/C-separated signals.

The V/C/D IC controls contrast, brightness, color and tint signals by bus control.

RGB signals whose irregularities in luminance and color are corrected for the multi-screen system by the V/C/D IC are supplied to the drive IC that adjusts gain for white balancing. After that, the RGB signals are input to the AKB IC to compensate age changing of cathode current of the CRT, and further supplied to the CRT after they are amplified by the CRT drive circuit.

The ABL circuit adjusts ABL voltage of respective projection units interlocking the ABL voltage of all projection units so as to follow the lowest voltage.

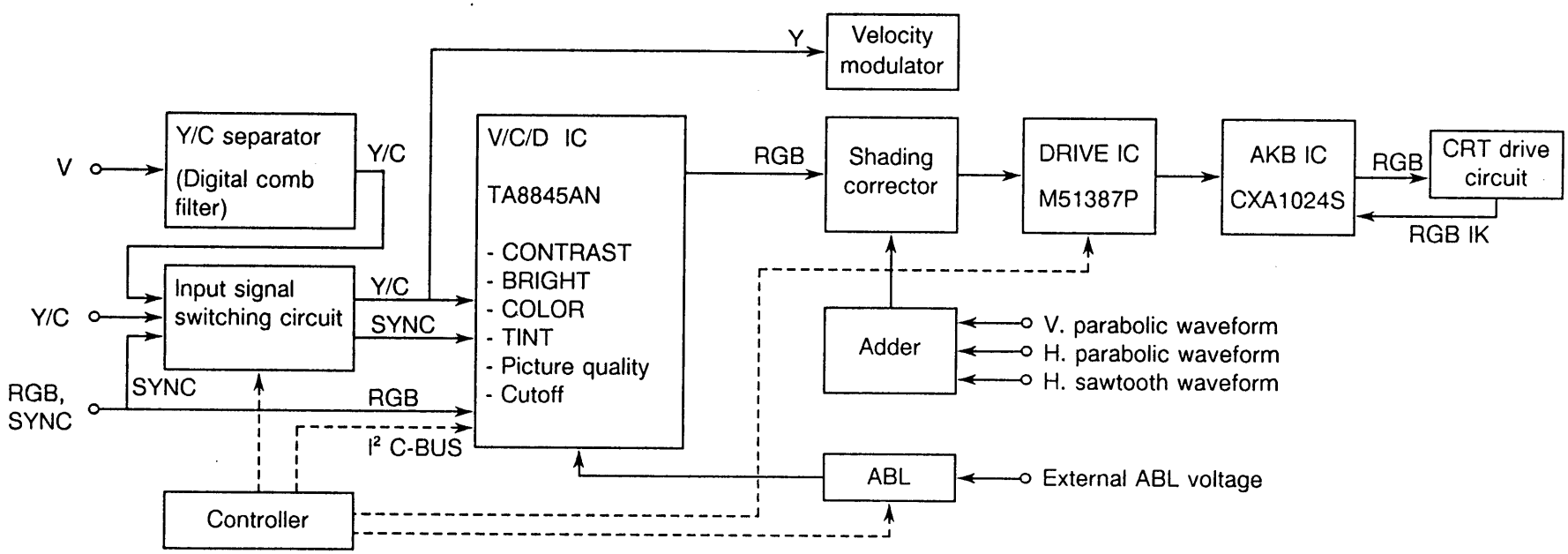


Fig. 4-1-1 Video circuit block diagram

4-2. INPUT SIGNAL SWITCHING CIRCUIT

The input signal switching circuit not only switches between composite video signal input and Y & C signal input but also changes over synchronizing signals according to the input mode of RGB signals or internal test signal. A block diagram of the input signal switching circuit is shown in Fig. 4-2-1.

Composite video signal input through the video input terminal is separated into Y and C signals, and then supplied to the signal switcher QV70 of the input signal switching circuit. Since QV70 is supplied with other Y and C signals from the Y/C input terminal, the Y/C-separated signals are switched on/off by the YC control signal in QV70, and they are input to the synchronize changer QB76 if QV70 switches them on. QB76 switches between two synchronizing signals, one is of the Y signal and supplied from the RGB terminals and the other is supplied from QB71 of the test signal generator IC, with the control signals of "RGB" and "TEST1", and QB76 supplies a synchronizing signal to the Y input terminal or the SYNC input terminal of the V/C/D IC, IC501 (TA8845AN).

Table 4-2-1 shows the logic of the input switching. When video input is selected (the level of the control signal "YC" is low), the video input and Y/C input can be switched over by the EXT. CONTROL terminal as shown in Table 4-2-2.

Input signal/Control signal	YC	RGB	TEST 1	TEST 2
VIDEO	L	L	H	H
Y/C	H	L	H	H
RGB	L or H	H	H	H
TEST1 (cross pattern)	L or H	L	L	L
TEST2 (mesh pattern)	L or H	L	L	H

Table 4-2-1 Logic of input switching

EXT. CONTROL terminal	Input signal
Shortcircuit	Y/C
Open circuit	VIDEO

Table 4-2-2 Specifications of EXT. CONTROL terminal

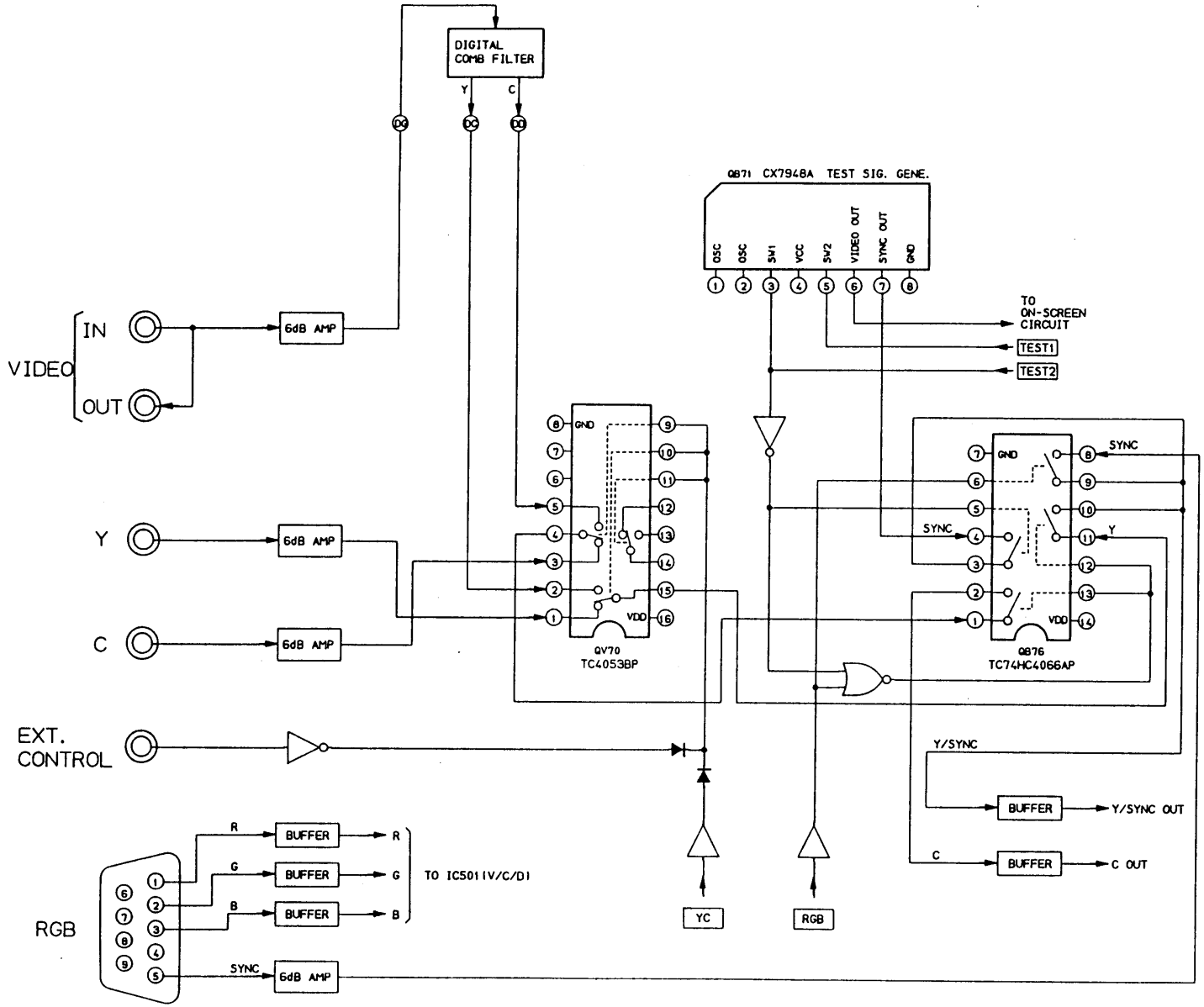


Fig. 4-2-1 Block diagram of input signal switching circuit

4-3. CONTROL SIGNAL GENERATOR CIRCUIT

In the control signal generator circuit, the 8-bit serial-in parallel-out shift register QA23 (TC74HC595AP) controls input signal switching with three-wire serial data from the microprocessor, and the D-A converter QA22 (M62358P) outputs analog control voltage. A block diagram of the circuit is shown in Fig. 4-3-1.

QA23 performs parallel output under control of the DATA, CLK and S/P-LAT lines, while QA22 performs D-A conversion under control of the DATA, CLK and DAC-LOD lines. the DATA and CLK lines are used in common with the on-screen display IC, ICA03 (μPD6453CY-514).

QA23 (TC74HC595AP)

Pin No.	Pin Name	Function	Output level (H = 5 V, L = 0 V)
15	YC	VIDEO/Y,C switching	VIDEO = L, YC = H
1	RGB	RGB switching	RGB-H, Normal = L
2	TEST 1	Internal test signal switching	In reception of TEST signal L, Normal = H
3	TEST 2	Internal test signal switching	Cross pattern = L, Mesh pattern = H, Normal = H
4	VMS	Velocity modulation on/off switching	Fixed at L (ON)
5	VMG	Velocity modulation gain switching	Fixed at H (Gain: Max.)
6	QG	Not connected (open)	
7	QH	Not connected (open)	

Names, functions and output levels of output terminals of QA23 and QA22 are respectively shown in Table 4-3-1.

QA22 (M62358P)

Pin No.	Pin Name	Function	Output level
14	DRIVE R	R drive regulation	0 ~ 9 V
15	DRIVE G	G drive regulation	0 ~ 9 V
16	DRIVE B	B drive regulation	0 ~ 9 V
17	RASTER R	R raster switch	ON = 0 V, OFF = 5 V
18	RASTER G	G raster switch	ON = 0 V, OFF = 5 V
19	RASTER B	B raster switch	ON = 0 V, OFF = 5 V
4	ABL LEVEL	ABL voltage regulation	0 ~ 9V
5	COMBI	ABL interlocking switching	ON = 0 V, OFF = 5 V
6	MULTI	Shading correction switching	ON = 0 V, OFF = 5 V
7	MUTE	Video muting	MUTE ON = 5 V, MUTE OFF = 0 V
8	OSD LEVEL	On-screen brightness switching	LEVEL 1 = 4.5 V, LEVEL 2 = 2.25 V
9	A12	Not connected (open)	

Table 4-3-1

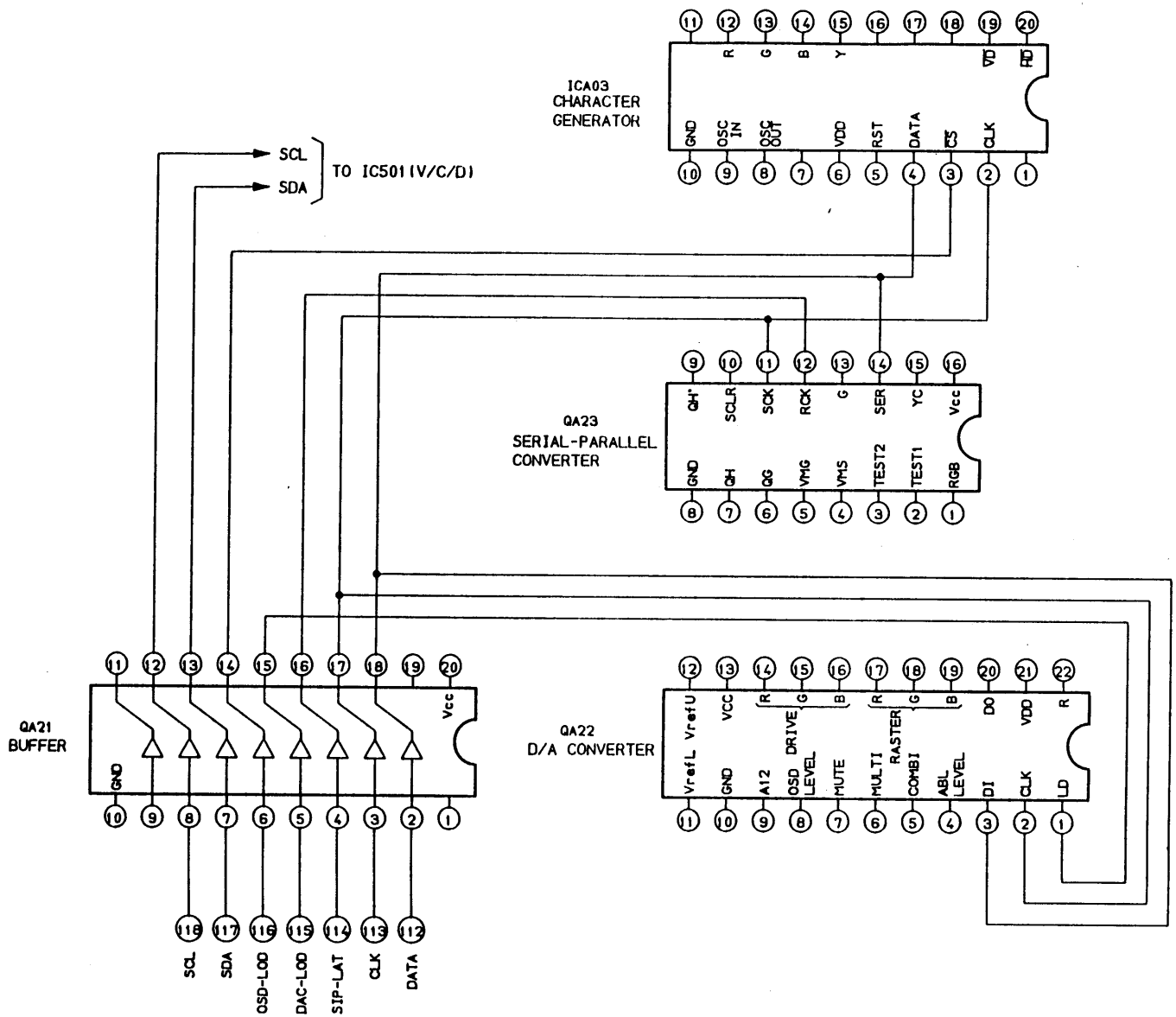


Fig. 4-3-1 Block diagram of control signal generator circuit

4-4. DIGITAL COMB FILTER

1) Outline

The digital comb filter separates input video signal into Y and C signals with the 2H memory.

As compared with previously used analog 2-CCD comb filters, this digital comb filter is designed to be simplified in adjustment.

	Digital comb filter	2-CCD comb filter
Adjusting points	Adjustment-free	8 points

Table 4-4-1 Comparison between digital comb filter and 2-CCD comb filter

2) Signal flow

Fig. 4-4-1 shows signal amplitude and DC voltage at main points besides signal flow as a whole.

3) ICs used in the circuit

(1) QZ01 (TC9063N)

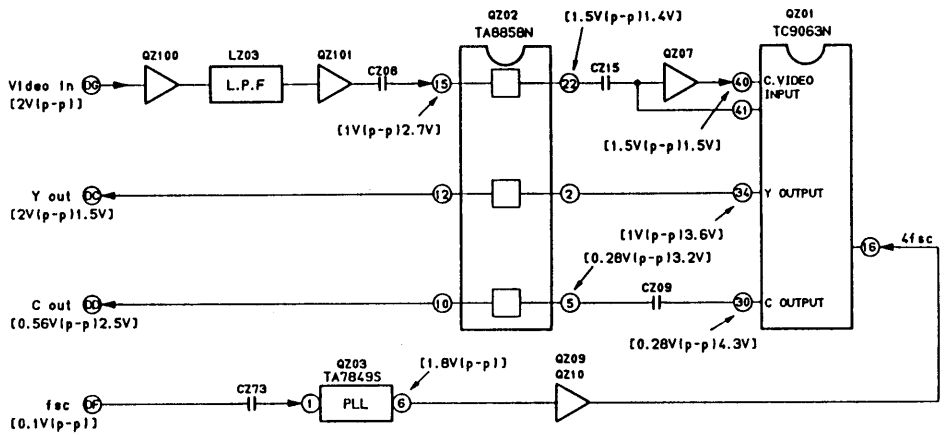
This IC, which incorporates an A-D converter, D-A converters and 2H line memory, functions as the Y/C separator with the 2H memory. Its system block diagram is shown in Fig. 4-4-2.

(2) QZ02 (TA8858N)

This IC which has built-in filters, amplifiers, switches, etc. is used in combination with QZ01 (TC9063N). Its system block diagram is shown in Fig. 4-4-3.

(3) QZ03 (TA8749S)

This IC functions as the PLL oscillator, which inputs 1 fsc (3.58 MHz) signal oscillated in the chroma system of the video circuit and outputs 4 fsc (14.3 MHz) signal to QZ01 (TC9063N).



Note: All DC voltages are shown in pedestal level.

Fig. 4-4-1 Digital comb filter circuit

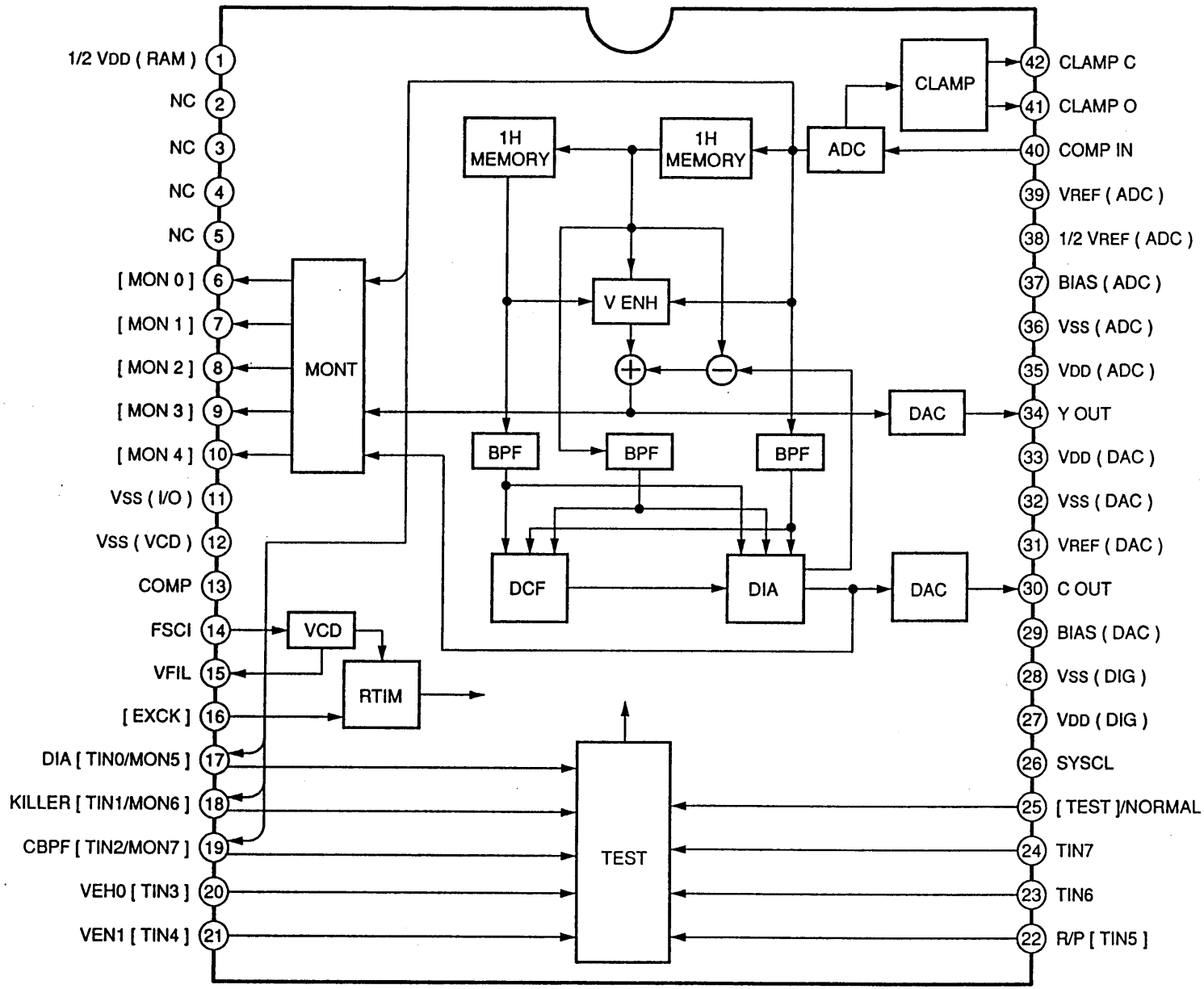


Fig. 4-4-2 TC9063N system block diagram

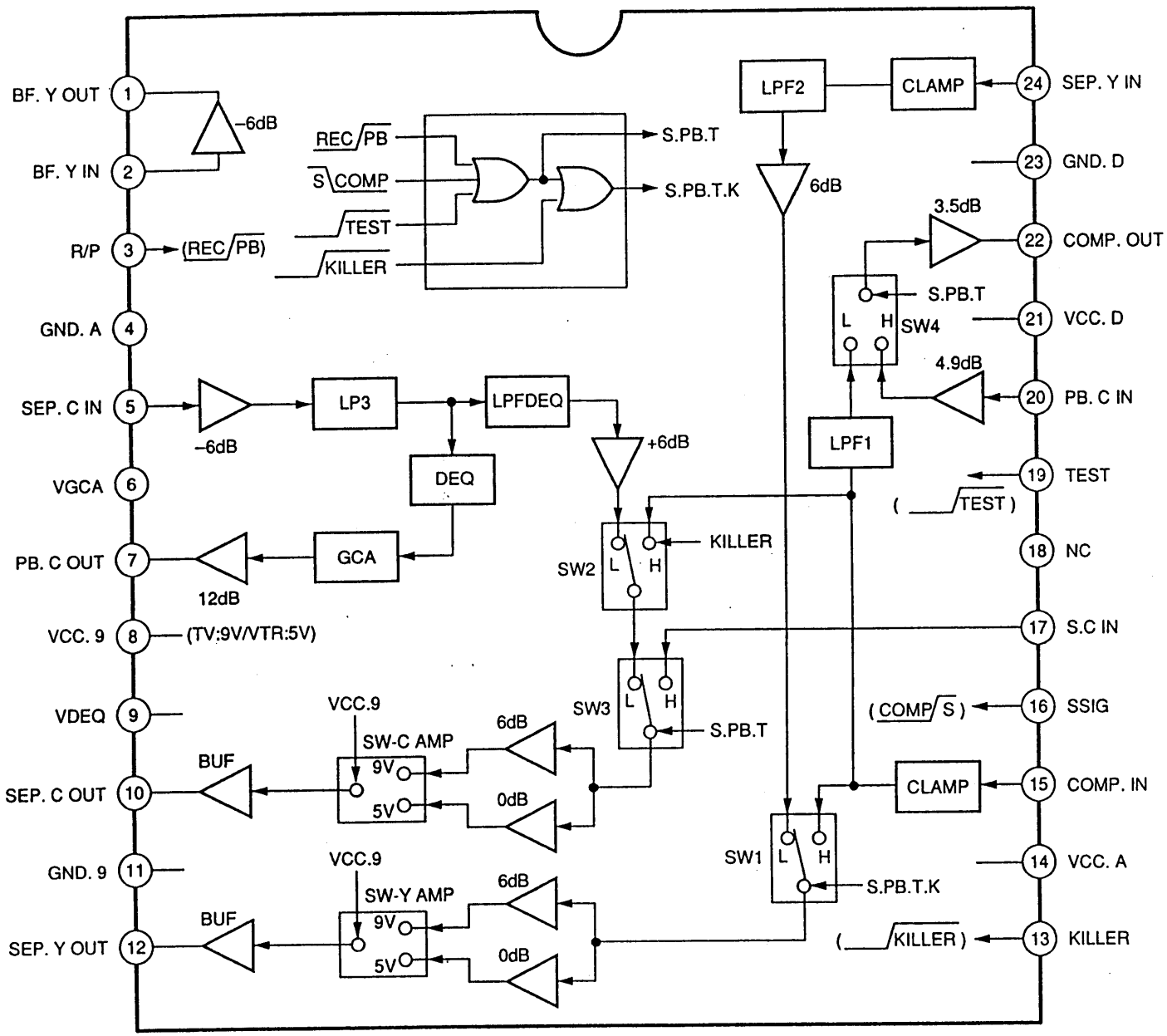


Fig. 4-4-3 TA8858N system block diagram

4-5. CHROMA SYSTEM OF VIDEO CIRCUIT

4-5-1. Outline of V/C/D IC (TA8845AN)

The chroma system of the video circuit employs the V/C/D IC, TA8845N, which is a multi-functional IC for realizing high-quality picture projection, namely, it internally incorporates R/G/B switching circuit, D-A converter for video control by the microprocessor, super-real transient circuit and other functions besides the bus control for white balance adjustment and for manufacture adjustment items.

1) Features of respective blocks

(1) Video signal processing circuit (Video block)
Besides the basic signal processing circuits such as adjustment circuits for brightness, contrast and quality of picture, DC playback circuit, etc., this block is featured by the following circuits.

① Super-real transient circuit
② Color detail emphasis circuit
③ Active noise reduction circuit
④ Black expansion circuit
⑤ High bright color circuit
⑥ White balance control circuit
⑦ Cut-off control circuit
⑧ Analog RGB circuit
⑨ On-screen display circuit

(2) Chrominance signal processing circuit (Chroma block)
This block which is mainly composed of such basic signal processing circuits as ACC (automatic color control circuit), color synchronizing circuit, color demodulation circuit, various tint regulating circuits has the following features.

① Adjustment-free 3.58 MHz oscillator thanks to the new circuitry which is hardly influenced by irregularity of IC elements.
② I.Q. filter built in the IC.
③ New fresh color circuit
④ Color limiter circuit
⑤ Color gamma correction circuit

(3) Deflection processing circuit (Deflection block)
This block which is mainly composed of such basic signal processing circuits as horizontal and vertical synchronizing separator circuits, deflection processing circuit, etc., has the following features.

① Stability of synchronization is improved by employment of automatic slice type synchronizing separator circuit.
② Both horizontal jitter and picture distortion are improved by the newly employed double AFC circuit.
③ Peripheral parts of the 32 fH (503 kHz) oscillator are reduced in number by realizing the 1-pin oscillator.
④ Adjustment-free circuit realized by horizontal and vertical countdown system.
⑤ Internally incorporated horizontal and vertical picture phase adjustment circuits (bus controlled).

2) IC specifications

(1) Circuit functions: Video, Chroma, Deflection, OSD, RGB, and other processings

(2) Type: 64 pins, DIP shrink type

(3) Number of elements: 5185 linear elements + 2137 gate elements; 972 PF in total

(4) Operation voltage: Vcc to pins 21, 48: 12 V
Vcc to pin 7: 9 V
Vcc to pin 6: 2.2 V

(5) Power consumption: 1140 mW

3) Circuit block diagram
A basic block diagram is shown in Fig. 4-5-1.

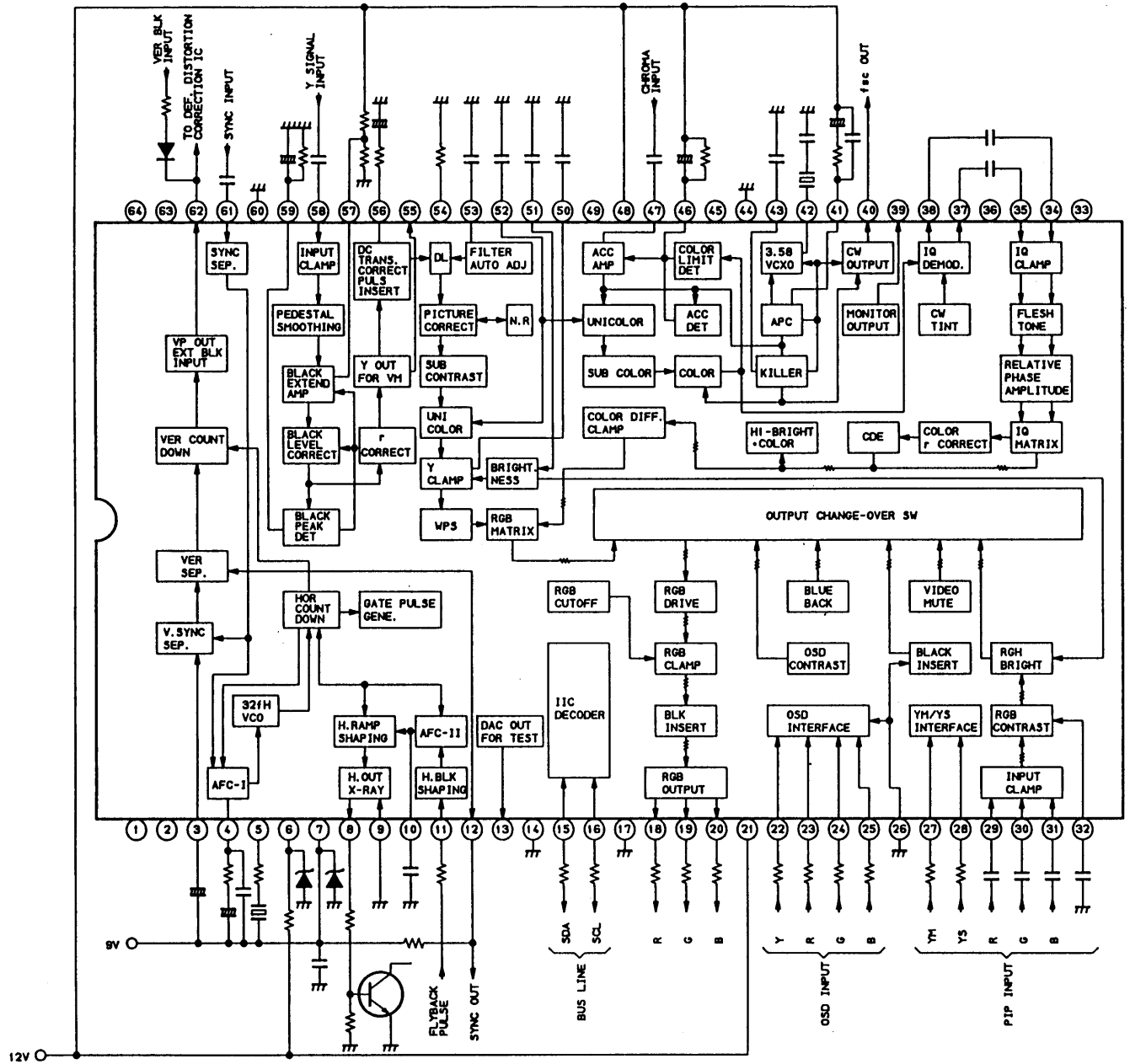


Fig. 4-5-1 TA8845AN block diagram

4-5-2. Video Signal Processing Circuit

1) Outline

This subsection explains about the signal flow of luminance signal that is output from the input signal switching circuit until it enters the shading correction circuit as well as about circuit operation in each part.

2) Operation and flow of luminance signal

Luminance signal flow is shown in Fig. 4-5-2a.

(1) Luminance signal output from the buffer QB80 of the input signal switching circuit is supplied to the delay line X201 to be delayed.

(2) Delayed luminance signal is input to pin 58 of the luminance signal processing IC (TA8845AN) for video processing.

(3) The processed luminance signal is output to the shading correction circuit as RGB outputs.

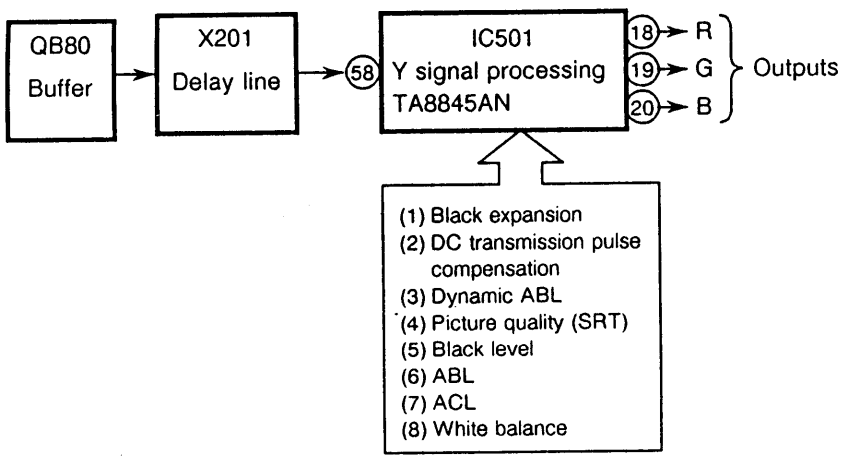


Fig. 4-5-2a

3) Luminance signal processing

The following explains processing of luminance signal that is input to pin 58 of IC501 together with external marginal constants.

(1) Black expansion operation and dynamic ABL

(1)-1 Meaning of black expansion operation

Expansion of signal components near the black portion of a waveform makes a firm picture with well-controlled black.
Fig. 4-5-2b shows relationship between input and output from a viewpoint of black expansion.

(1)-2 Meaning of dynamic ABL

If video signal of high APL (average picture level) is input, it increases high tension current. Therefore, video signal is controlled both in AC and DC to suppress flow of high tension current to a certain limit. Traditional video signal control circuits employ such the AC-DC joint control method.
In the traditional control method, however, the DC control may break black tone if the utmost black level (the deepest black) of the video signal is near the pedestal level. On the other hand, if the DC control is not applied, the black tone is not broken owing to the AC control but the picture having grayish black portion becomes dull and poor in contrast. To solve such problems, the DC control is activated when the utmost black level of the video signal exceeds the pedestal level (picture's black portion looks grayish), while the DC control is suspended when the utmost black level is equal to the pedestal level or under it. The circuit employing this method is called the dynamic ABL (automatic brightness limiter) circuit.

Note: APL : Average Picture Level
AC control: ACL (Automatic Contrast Limiter) circuit
DC control: ABL (Automatic Brightness Limiter) circuit

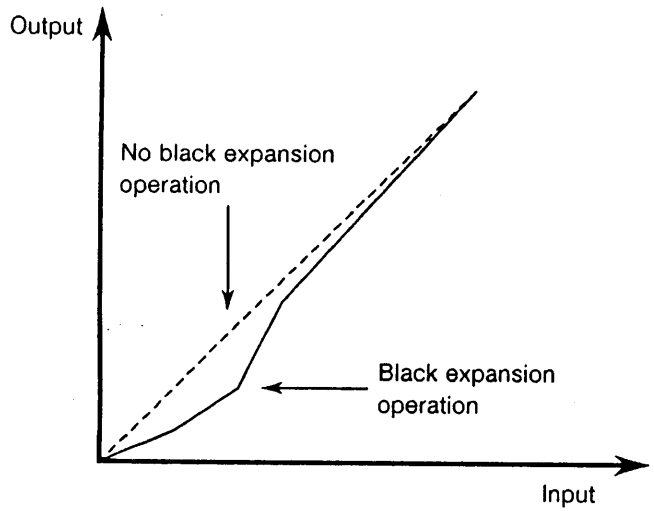


Fig. 4-5-2b

Circuit operation

① Luminance signal is input to pin 58 of IC501.
② Input luminance signal is expanded in the black component, and the average picture level is detected at the same time.

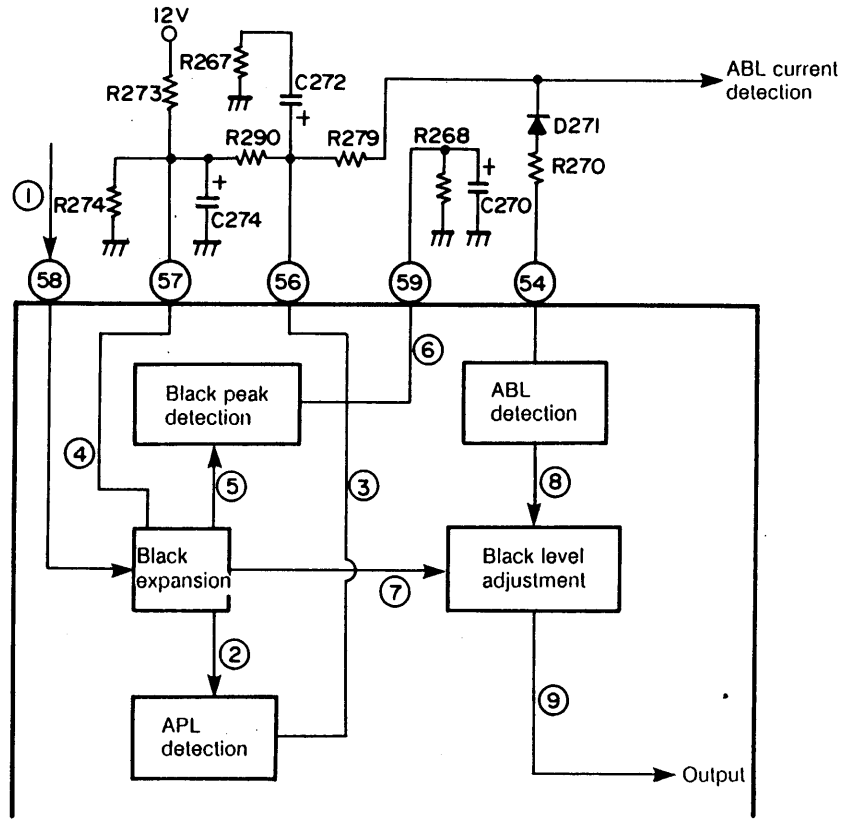


Fig. 4-5-2c

③ The detected APL is output from pin 56 of the IC, and then smoothed by R290 and C274. This voltage is applied to the connection point of R273 and R274, and impressed to pin 57. Accordingly, the value of voltage impressed to pin 57 varies depending on the average modulation of the luminance signal.

④ The voltage impressed to pin 57 is fed back to the black expansion circuit, and this voltage determines the signal level to activate black expansion.

⑤ On the other hand, the luminance signal whose black component is expanded is input to the black peak detection circuit.

⑥ The black peak detection circuit detects the area whose level is less than the pedestal level, and it stops black expansion when the detected area exceeds a certain limit which is determined by R268 between pin 59 and the ground. (The smaller the resistance value of R268 is, the larger the area becomes.)

⑦ The luminance signal whose black component is expanded is supplied to the black level correction circuit.

⑧ As high tension current flows much, voltage at pin 54 drops down and the dynamic ABL circuit is accordingly activated to adjust the black level according to the voltage.

Note: In the multi-screen system, the black expansion circuit is always turned off, because black expansion makes the pictures uneven in the black tone at respective edge portions.

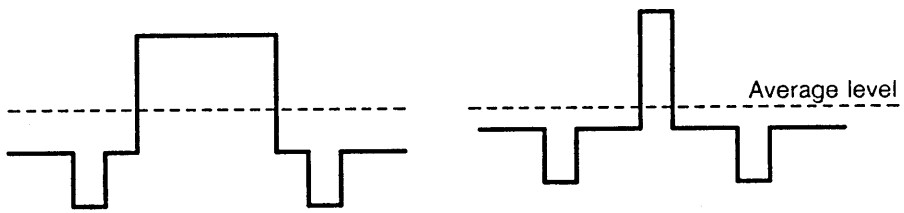
⑨ Finally, the luminance signal that is controlled by the black expansion and dynamic ABL circuit is output.

(2) DC transmission compensation

If luminance signal is amplified step by step by direct-coupled amplifiers, the DC level of the luminance signal will faithfully be reproduced. In practical circuitry, however, it needs to use additional capacitive-coupled amplifiers, which varies the pedestal level depending on average signal level. The DC transmission compensation circuit is provided to solve such the problem.

Fig. 4-5-2d shows examples of 0 % DC transmission and 100 % DC transmission.

<In case of 0 % DC transmission>



<In case of 100 % DC transmission>

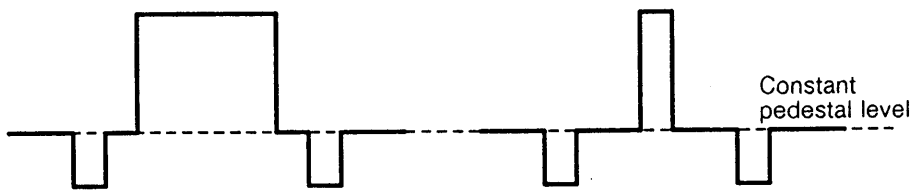


Fig. 4-5-2d

Circuit operation

① Luminance signal that is controlled by the black expansion circuit and the dynamic ABL circuit is input to the DC transmission compensation circuit.

② The rate of DC transmission compensation is determined by R279, R269 and R267 that are connected with pin 56.

Note: In this projection unit, pin 33 is fixed open.

③ The compensation rate is input to the DC transmission compensation circuit according to the average modulation rate.

④ Luminance signal that is compensated by the DC transmission compensation circuit is output.

(3) Picture quality control circuit

Before luminance signal enters the picture quality control circuit, it undergoes edge correction in the super-real transient circuit or the aperture correction circuit as shown in Fig. 4-5-2f. Edge correction is performed by different circuits depending on the amplitude of signal waveform; namely, the aperture circuit is activated for small amplitude while the super-real transient circuit is activated for intermediate and large amplitudes.

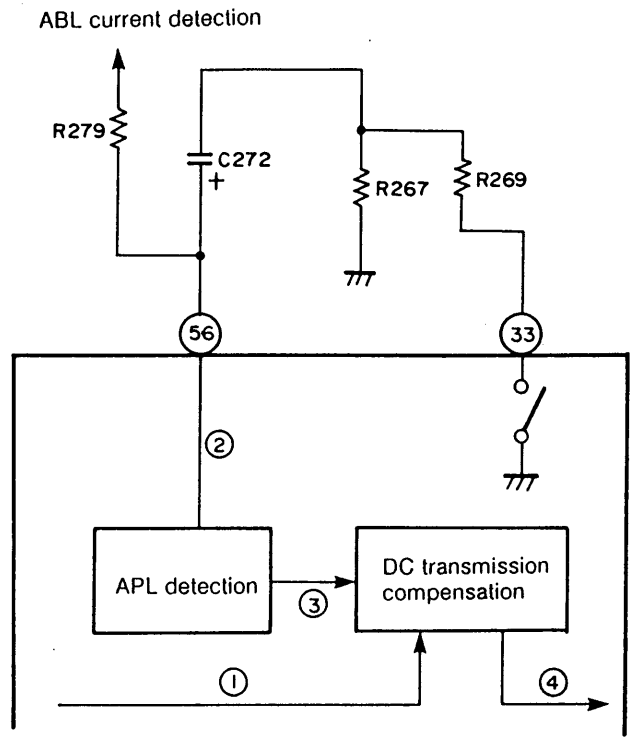


Fig. 4-5-2e

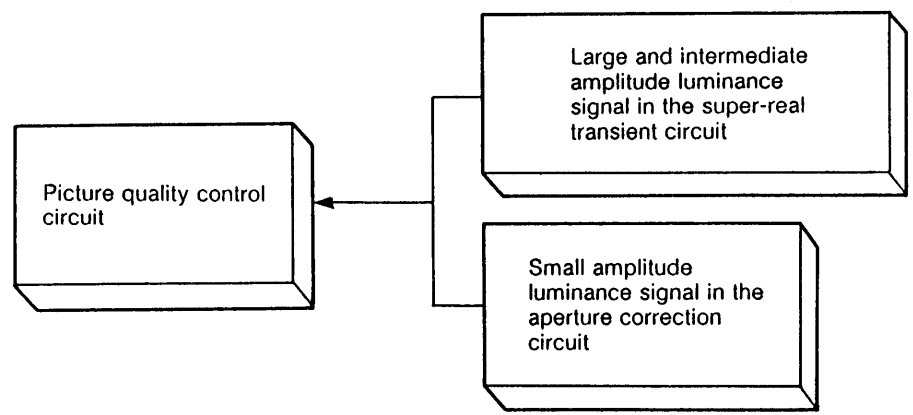


Fig. 4-5-2f

(3)-1 Super-real transient circuit

The super-real transient circuit functions to improve sharpness of large and intermediate amplitude luminance signal in the edge portions with addition of little pre-/over-shooting.
Fig. 4-5-2g shows a block diagram of the super-real transient circuit.

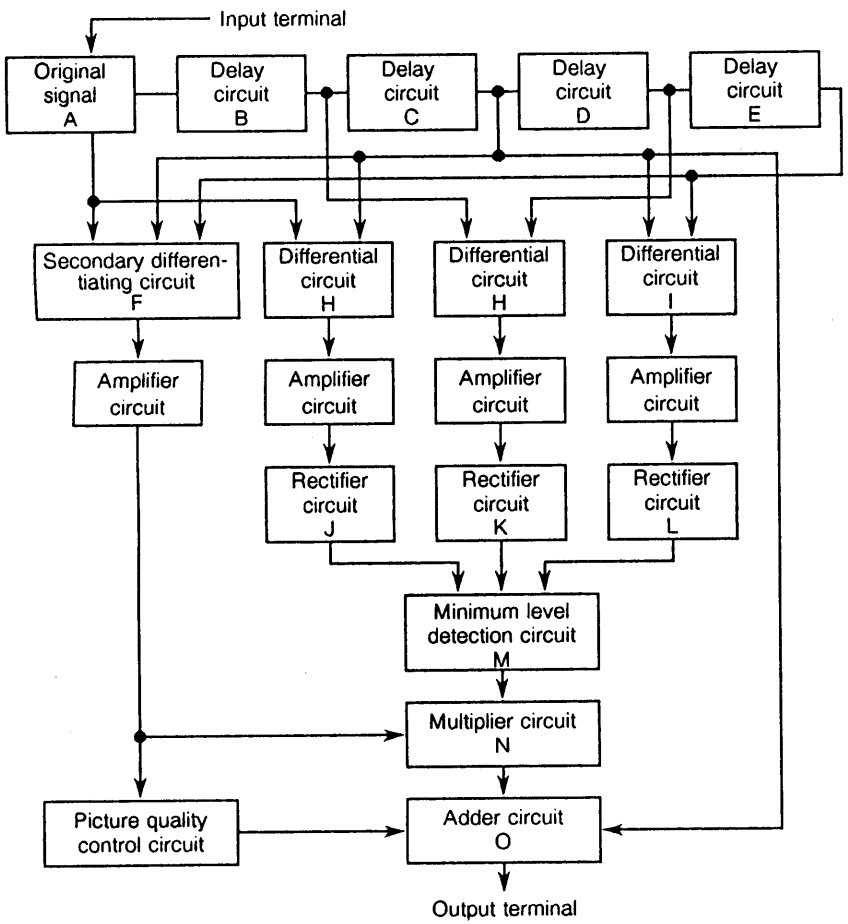


Fig. 4-5-2g

Operation waveforms in respective blocks are shown in Fig. 4-5-2h.

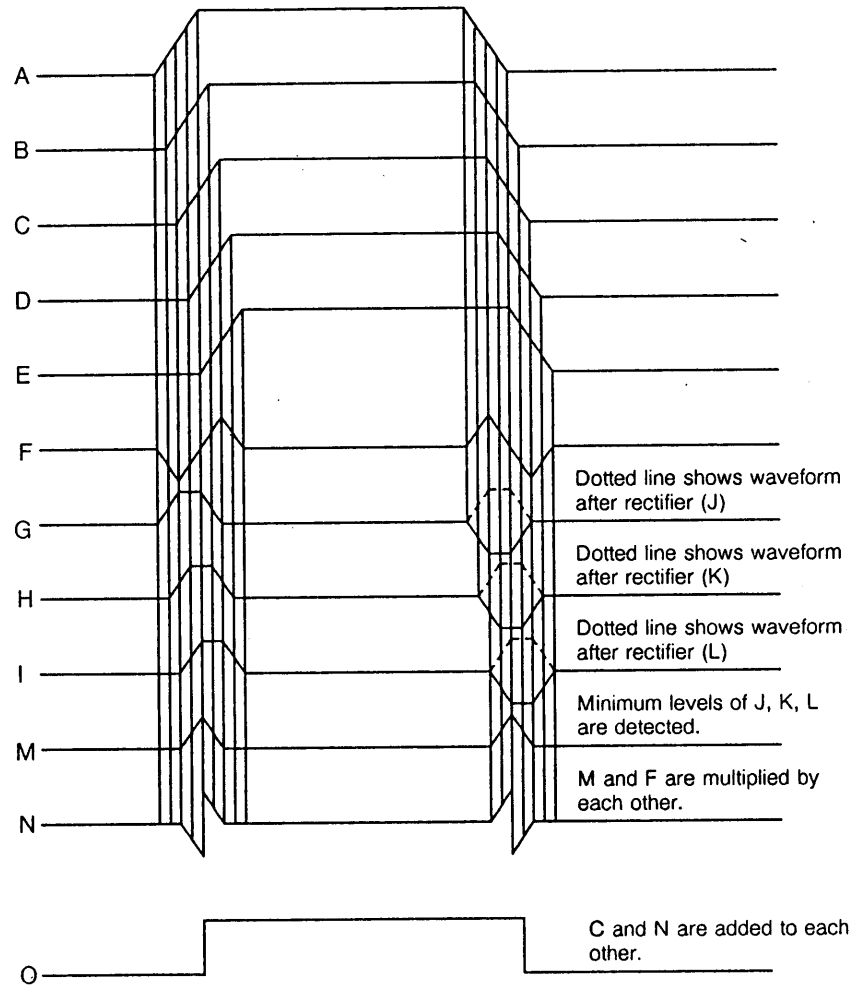


Fig. 4-5-2h SRT circuit output waveforms with input of pedestal waveform

(3)-2 Aperture correction circuit

The aperture correction circuit corrects the edge portions of small amplitude luminance signal by composing its waveform with two delay lines.

Circuit operation

① Luminance signal that is controlled by the black expansion, dynamic ABL and DC transmission compensation circuits is input to the aperture correction circuit, the super-real transient circuit and the delay line respectively. (Luminance signals that are input to the aperture correction circuit and the real-transient circuit are used as the reference signal.)

② Delay time (period of pre-shoot or over-shoot) is determined by connecting C264 to pin 53.

③ The delay time determined in the above step ② is input to the delay line.

④ With the determination of the delay line, the super-real transient circuit starts operation to correct edge portions (of large and intermediate amplitude waveforms).

⑤ Luminance signal that is not corrected in the edge portion by the super-real transient circuit undergoes edge correction in the aperture correction circuit.

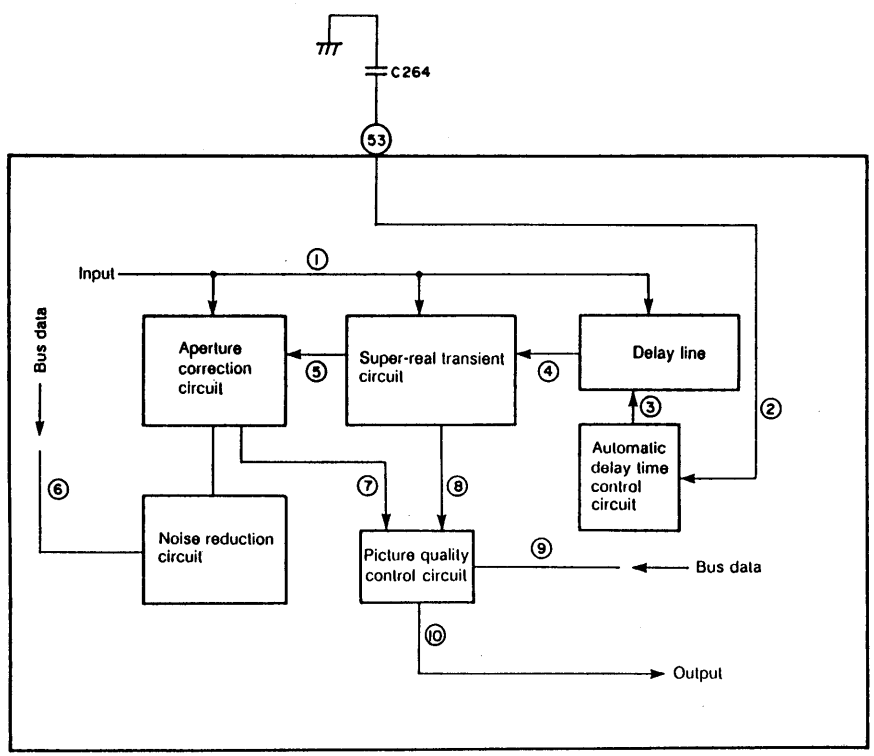


Fig. 4-5-2i

⑥ Luminance signal whose edge portions are corrected by the aperture correction circuit and the super-real transient circuit is input to the picture quality control circuit.

⑦ The picture quality is controlled by bus data in the picture quality control circuit. Accordingly, correction rate of the aperture correction circuit changes depending on the control data.

⑧ The luminance signals corrected by the aperture correction circuit and the super-real transient circuit are added to each other, and the resultant signal is output.

(4) Brightness, unicolor, ABL and ACL circuits

Circuit operations

① Luminance signal that is corrected in the picture quality is input to the contrast circuit.

② Contrast of the signal is controlled by bus data. As high tension current flows much, voltage at the cathode of D287 drops down and D287 is turned on. As a result voltage at pin 52 drops down to turn down the contrast. (ACL circuit)

③ Bus data also controls the brightness of the signal. As high tension current flows much, voltage at the anode of D260 drops down and D260 and D261 are turned on. As a result voltage at pin 51 drops down to turn down the brightness. (ABL circuit)

④ The controls mentioned in the above steps ② and ③ are operated by the DC regenerative circuit.

⑤ IRE value for gamma correction is determined by the white peak detection circuit.

⑥ Gamma correction is applied to the luminance signal that is output from the DC regenerative circuit.

⑦ After the above processes, the signal is output as Y signal from the Y output circuit to the RGB matrix circuit.

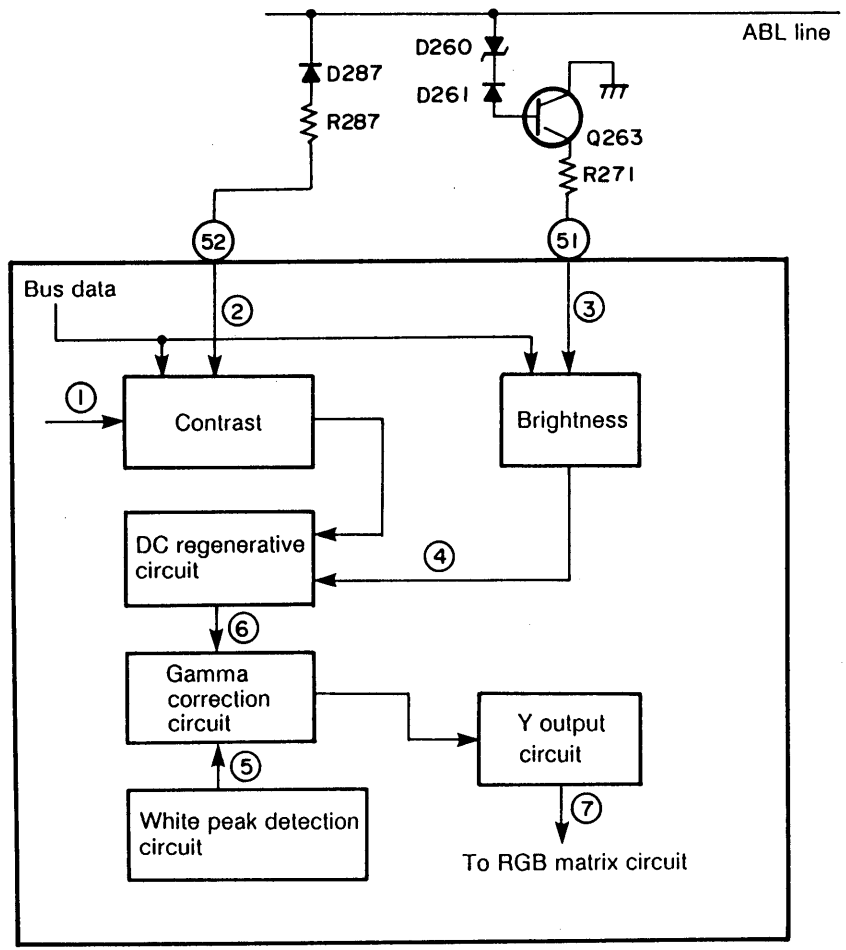


Fig. 4-5-2j

4-5-3. Color Circuit

1) Outline

The chrominance signal circuit regulates 3.58 MHz chrominance signal (color subcarrier + burst signal) contained in composite video signal in the tint, color density as well as operates color demodulation, color killer control (to stop the color circuit in receiving B/W broadcasting), ACC (automatic color control: to hold the level of color subcarrier supplied to the color demodulator circuit regardless of fluctuation in color broadcasting receiving condition).

The color synchronizing circuit, which is mainly composed of the 3.58 MHz oscillator and the APC (automatic phase control) circuit, is an adjustment-free circuit with a newly designed circuitry that is hardly influenced by irregularity of IC devices.

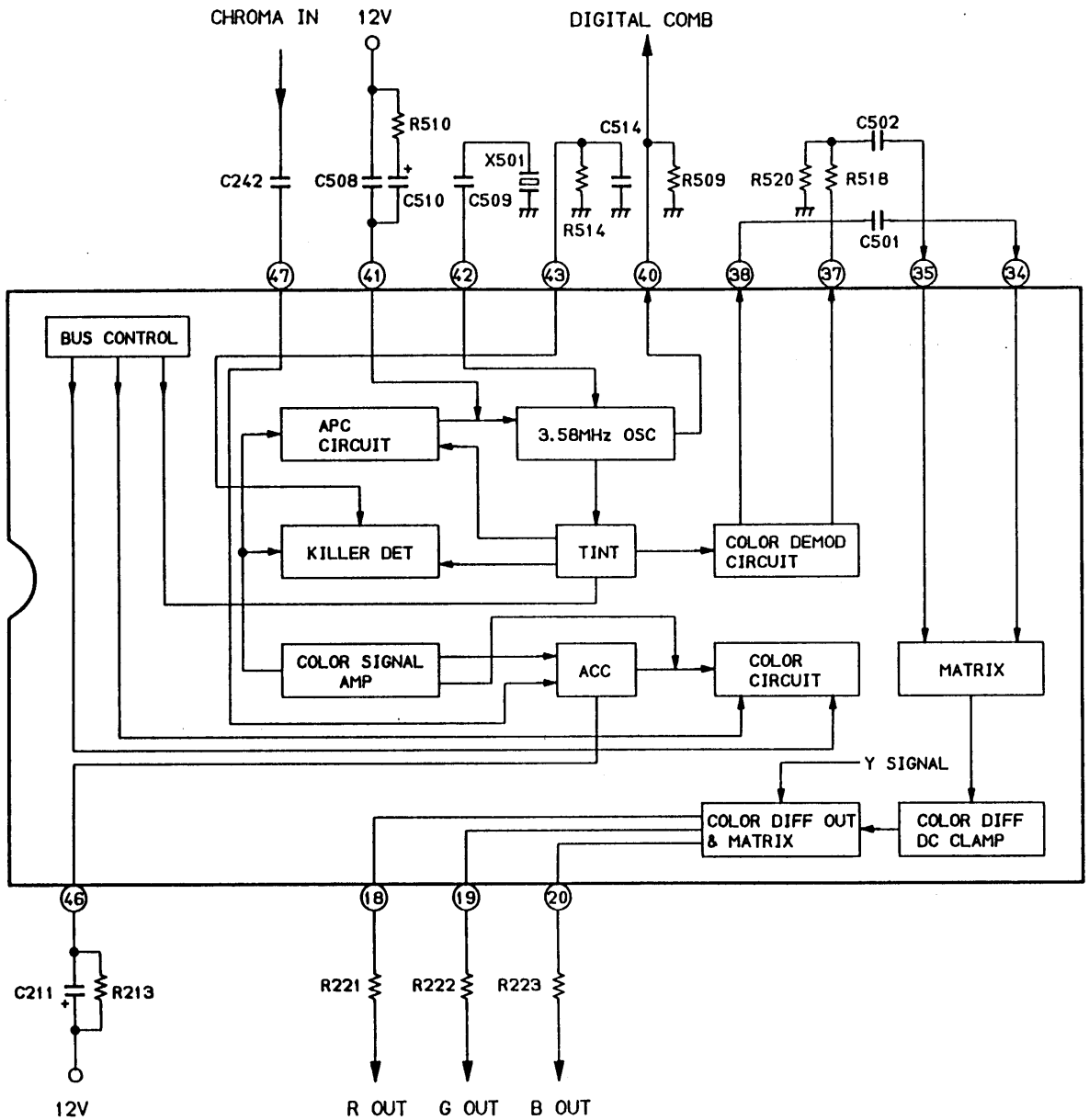

CHROMA IN
12V
DIGITAL COMB
R510
C242
C508
C510
X501
C509
C514
R514
R509
C502
R520
R518
C501
47
41
42
43
40
38
37
35
34
BUS CONTROL
APC CIRCUIT
3.58MHz OSC
KILLER DET
TINT
COLOR DEMOD CIRCUIT
COLOR SIGNAL AMP
ACC
COLOR CIRCUIT
MATRIX
Y SIGNAL
COLOR DIFF OUT & MATRIX
COLOR DIFF DC CLAMP
46
18
19
20
C211
R213
R221
R222
R223
12V
R OUT
G OUT
B OUT

Fig. 4-5-3a

2) Color density adjustment circuit
Color density is adjusted by controlling gain of chrominance signal.

Operation principle

Chrominance signal (burst signal + color subcarrier) that is input through pin 47 of IC501 is supplied to the ACC circuit, which is controlled to keep amplitude of chrominance signal constant automatically regardless of fluctuation of electric field intensity. Chrominance signal having a constant amplitude is supplied to the color circuit, in which color subcarrier is regulated to have an amplitude suitable for bus control, or to have an optimum color density in other words, before it is supplied to the color demodulator circuit.

3) Tint adjustment circuit
Tint is adjusted by controlling the phase of chrominance signal.

Operation principle

In receiving color broadcasting, the 3.58 MHz oscillator oscillates the reference subcarrier whose phase is synchronized with that of burst signal by the APC circuit. The tint adjustment circuit regulates the tint by controlling the phase of the reference subcarrier to be sent to the color demodulator circuit with tint regulating voltage adjusted by users as they like.

4) 3.58 MHz oscillator
The phase of burst signal is synchronized with that of the reference subcarrier that is output from the 3.58 MHz oscillator to oscillate 3.58 MHz signal. This circuit employs a new circuitry that is hardly influenced by irregularity of IC devices.

Operation principle

The phase of burst signal supplied from the color circuit is compared with that of the reference subcarrier oscillated by the 3.58 MHz oscillator by the APC detection circuit, and a control voltage is resultantly output.
Receiving the control voltage, the 3.58 MHz oscillator outputs the reference subcarrier whose phase is synchronized with that of burst signal. In other words, burst signal is synchronized with the reference subcarrier output from the 3.58 MHz oscillator by the loop circuit shown in Fig. 4-5-3c.

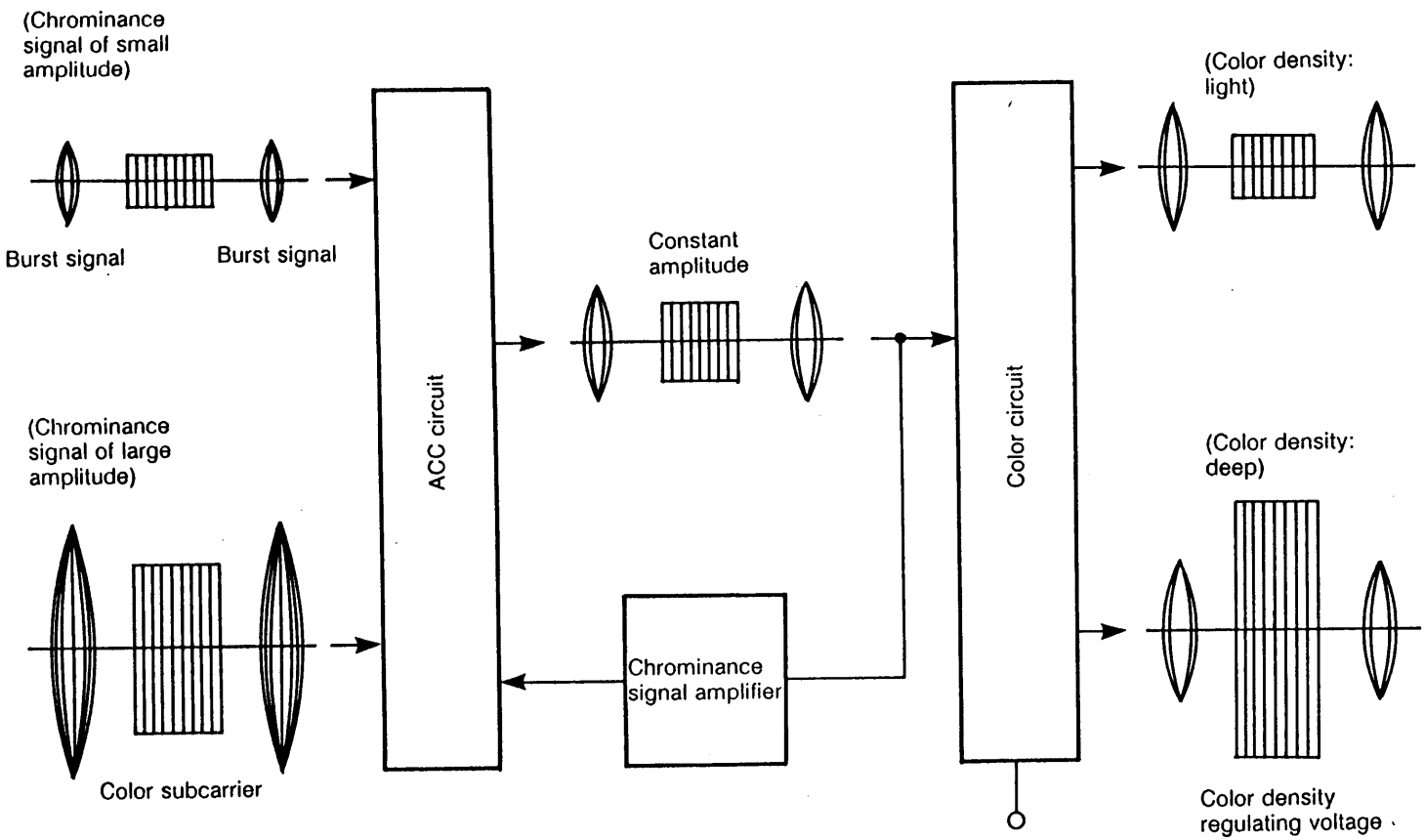

(Chrominance signal of small amplitude)
Burst signal
Burst signal
ACC circuit
Constant amplitude
(Color density: light)
(Chrominance signal of large amplitude)
Color subcarrier
Chrominance signal amplifier
Color circuit
(Color density: deep)
Color density regulating voltage

Fig. 4-5-3b

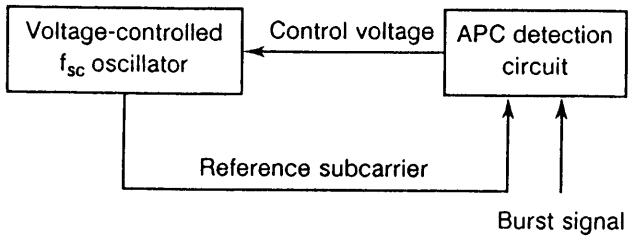


Fig. 4-5-3c APC circuit block diagram

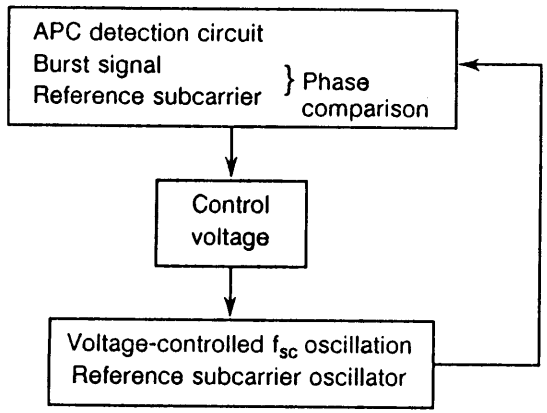


Fig. 4-5-3d APC circuit loop

Table 4-5-3a Killer circuit operation

Reception signal	Chrominance signal input terminal (Pin 47)	Killer filter terminal voltage (Voltage at pin 43)	Killer circuit operation	Color density adjustment circuit operation
Color	Chrominance signal input	9.1 V approx.	OFF	ON
B/W	Color noise	8 V approx.	ON	OFF

5) Killer circuit

The killer circuit functions to prevent color noise from appearing in the picture when B/W broadcasting is received.

Operation principle

(1) In the killer circuit burst signal supplied from the chrominance signal amplifier circuit and the reference subcarrier supplied from the 3.58 MHz oscillator are detected by the killer detector, and the detected signals are converted into DC voltage by the capacitor C514 of pin 43. The resultant DC voltage is used to turn on/off the color density adjustment circuit. (When pin 43 is loaded with DC voltage, the color density adjustment circuit is on.)

(2) Accordingly, burst signal is not supplied to the killer detector in receiving B/W broadcasting, and the level of DC voltage is low. As a result, the color density adjustment circuit stops operation not to output color signal (containing color noise).

6) ACC (Automatic Color Control) circuit

The ACC circuit functions to make the input level of chrominance signal constant avoiding it from fluctuation of electric field intensity, etc.

Operation principle

(1) When electric field intensity is high, burst signal of input chrominance signal is only supplied to the ACC (automatic color control) circuit.

(2) The ACC circuit detects the burst signal input and converts it into DC voltage by the capacitor C211 of pin 46. The resultant DC voltage is used to hold the gain of chrominance signal constant.

When electric field intensity is low and noise components increase, the ACC circuit functions against the noise components to prevent them from appearing in the picture.

(3) Signal (chrominance signal + noise components) that is input through pin 47 generally has input level higher than the level (10 mVp-p) for activating the ACC circuit. Therefore, the gain of the input signal is controlled to be decrement in the ACC circuit.

Table 4-5-3b ACC circuit operation

Electric field intensity	Color signal component	Gain of color amplifier circuit controlled by ACC circuit	Voltage at ACC filter terminal (Voltage at pin 46)
High	Big	Decrement	- Approx. 8.7 V input with chrominance signal input of 100 mVp-p - Decreases with high electric field intensity. - 11.3 V without input signal
Low	Little (much noise components)	Decrement	Decreases with more noise components.

7) Color demodulation circuit

The color demodulation circuit demodulates color difference signal from color subcarrier signal with the reference subcarrier synchronizing with burst signal.

Operation principle

(1) Color subcarrier supplied to the color demodulator circuit is converted into color difference signal (I.Q. signal) by detecting it with the reference subcarrier supplied from the tint adjustment circuit.

(2) The two signals mentioned above are output from pin 38 and pin 37 of IC501, and they are input to pin 34 and pin 35 respectively.

(3) Chrominance signal undergoes DC-clamping at pins 34 and 35 of IC501, and the resultant signal is supplied to the matrix circuit.

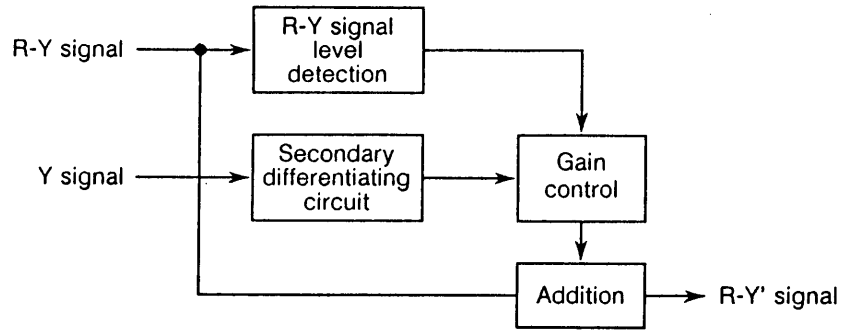
(4) The matrix circuit demodulates I, Q signals to R-Y, G-Y and B-Y signals, and these signals are DC-clamped by the color difference signal DC clamping circuit. Then, these signals are supplied to the matrix circuit to be mixed with Y signal, and are finally output from the RGB output pins 18, 19 and 20.

8) Color detail enhancer circuit

In the current NTSC system, gamma correction in the CRT is operated by the transmitter side. For matrixing R, G, B signals after they have undergone gamma correction, detailed high saturation components (deep color components) are mixed in the I, Q signals.

Since chrominance signal is wider in the band width (1.5 MHz on I axis, 0.5 MHz on Q axis) compared with luminance signal, it loses detailed information in the high saturation components and accordingly deteriorates in resolution.

The color detail enhancer circuit is newly employed for improving the above-mentioned problem.



*High luminance components of high color saturation signal are added to R-Y signal.

Fig. 4-5-3e

4-6. SHADING CORRECTION CIRCUIT

1) Outline

The shading correction circuit compensates and corrects decrease in luminance and irregular coloring which occur in the joint portions of screens in the multi-screen system (or in the edge portions in case of single unit). For this purpose, the shading correction circuit modulates R, G, B signals supplied from the V/C/D IC (TA8845AN) with correction waveforms, and it outputs the modulated R, G, B signals to the drive regulation circuit. The correction waveforms are yielded from V. parabolic waveform, H. parabolic waveform and H. sawtooth waveform generated in the convergence circuit, which waveforms are proper for correction of R, G, B signals respectively.

2) Circuit operation

(1) Processing of R, G, B signals

The switch QP03 functions to add a reference voltage (3 V approx.), which is determined by RP132 and RP133 in the blanking period, to R, G, B signals supplied from the V/C/D IC (TA8845AN). This reference voltage is used as the reference for the black level. The following explains about R signal by way of example.

R signal that passed through QP03 is modulated with R correction waveform by the double balanced differential amplifier composed of dual transistor QP41, QP35 and QP35 (2SC3381BL), and then output through the buffer QP32. The maximum amplification degree of the double balanced differential amplifier is determined by the ratio between RP105 and RP126 and it is approximately 1 time (almost equal), however, actual amplification degree is 1/2 of the maximum amplification degree because QP35 and QP36 have the same base bias potential.

The correction waveform is applied to the common base of pin 7 of QP35 and pin 1 of QP36 for modulating amplification degree of R signal.

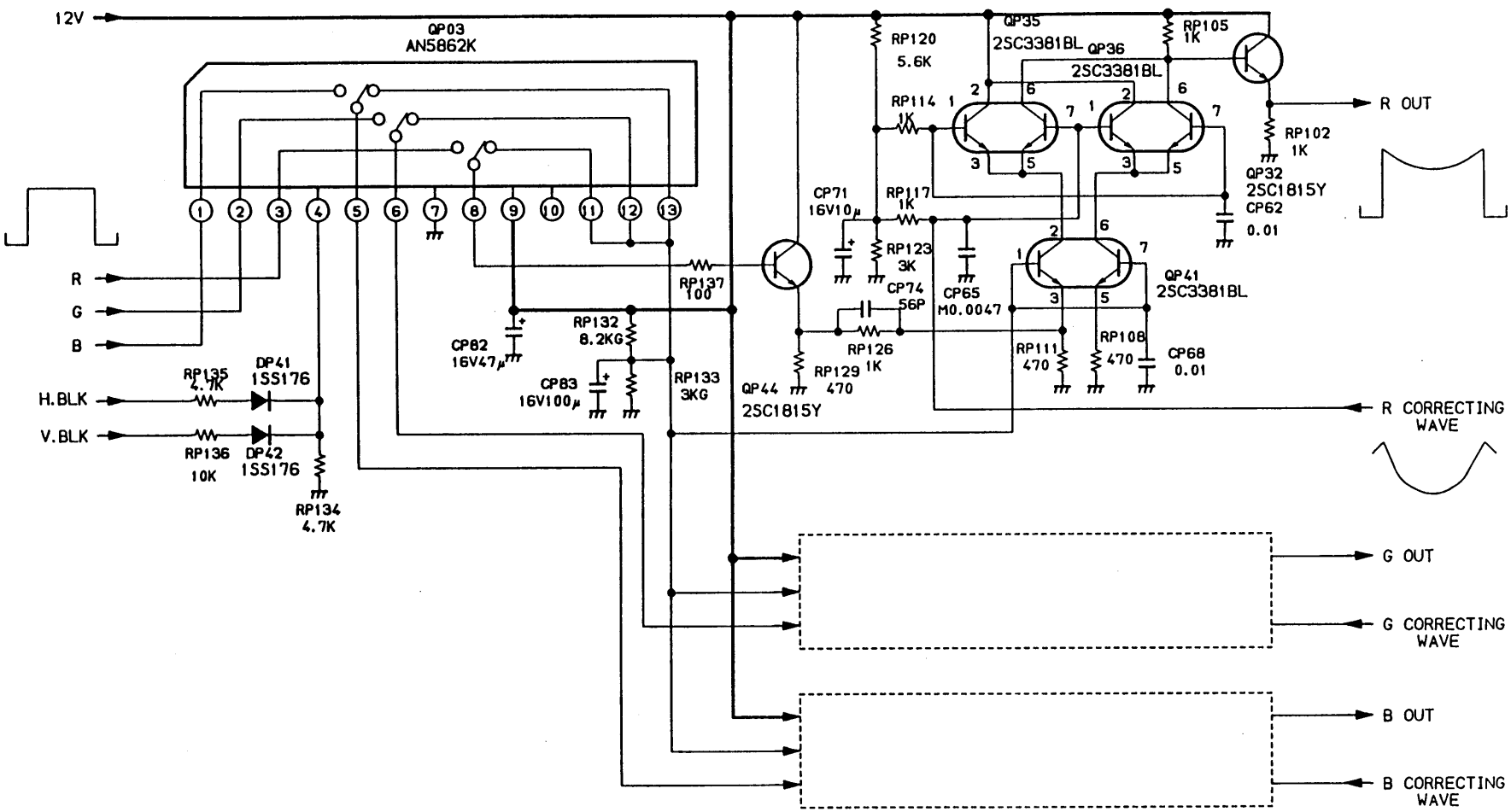

12V
QP03
AN5862K
R
G
B
H.BLK
V.BLK
RP135
4.7K
DP41
1SS176
RP136
10K
DP42
1SS176
RP134
4.7K
RP120
5.6K
QP35
2SC3381BL
QP36
2SC3381BL
RP105
1K
RP114
1K
R OUT
RP102
1K
QP32
2SC1815Y
CP62
0.01
CP71
16V10μ
RP117
1K
RP123
3K
CP74
56P
CP65
M0.0047
QP41
2SC3381BL
RP137
100
CP82
16V47μ
RP132
8.2KG
CP83
16V100μ
RP133
3KG
RP126
1K
RP129
470
QP44
2SC1815Y
RP111
470
RP108
470
CP68
0.01
R CORRECTING
WAVE
G OUT
G CORRECTING
WAVE
B OUT
B CORRECTING
WAVE

Fig. 4-6-1

(2) Correction signal processing

Gains of V. parabolic waveform, H. parabolic waveform and H. sawtooth waveform are controlled by the multiplier QJ42 (DAC8840) for adjustment of correction rate. At that time, H. parabolic waveform and H. sawtooth waveform are controlled in three systems for R, G, B signals.

V. parabolic waveform (V. PIN), respective H. parabolic waveforms for R, G, B signals, H. sawtooth waveform (R-H PIN, R-H SAW, G-H PIN, G-H SAW, B-H PIN, B-H SAW) whose gain is controlled BY QJ04 are respectively added to R, G, B signals, and those signals are amplified before they will be output through the switch QP06.

Correction rate is approximately 115 % in the ratio of signal level in the edges of the picture to that in the center of the picture, and the rate is the same in the vertical and horizontal directions. However, the correction rate in the horizontal direction is unbalanced by gain adjustment of H. sawtooth waveform for the purpose to correct unbalanced luminance in the right and left sides resulting from uneven color adjustment in the optical system. Tints in the right and left sides of the picture are adjusted by controlling the gain of H. sawtooth waveforms for R, B signals.

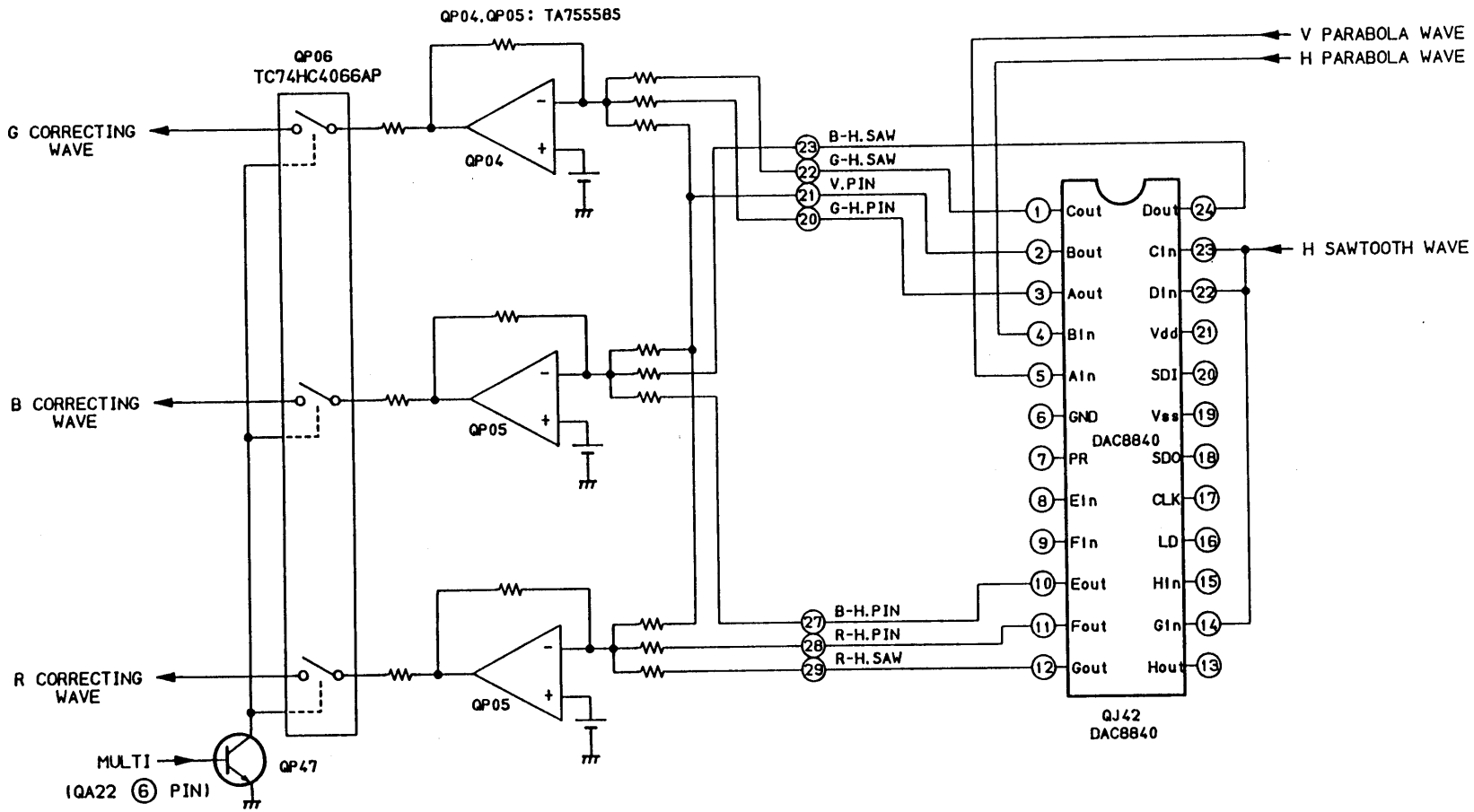


Fig. 4-6-2 Shading correction signal processing block diagram

4-7. DRIVE REGULATING CIRCUIT

The drive regulating circuit amplifies R, G, B signals supplied from the shading correction circuit by the drive IC QP02 (M51387P) besides performing drive regulation in the white balance adjustment mode.

Fig. 4-7-1 is a block diagram of IC M51387P. The control signal is supplied to the subcontrast control terminal from the D-A converter QA22. The cutoff regulation in the white balance adjustment mode is controlled by the V/C/D IC (TA8845AN) through the bus line.

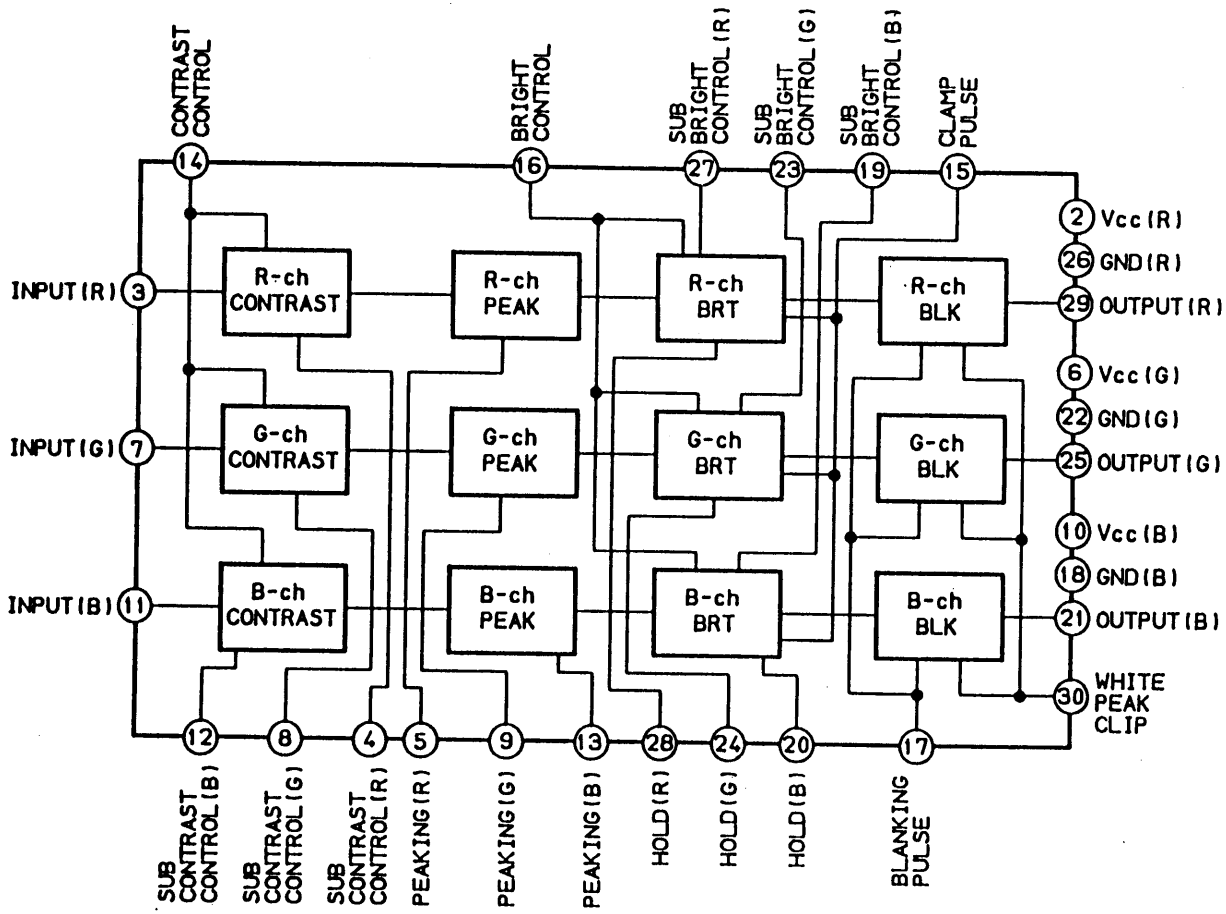


Fig. 4-7-1 M51387P block diagram

4-8. AKB CIRCUIT

1) Outline

The AKB circuit functions to compensate age changing of CRT cathode current. The IC CXA1024S is employed as the AKB IC (QP01) for AKB processing of this circuit.

For AKB processing, AKB reference signal is inserted into video signal. This signal is detected as cathode current by the CRT drive circuit and compared with the reference level so that the cathode current is always constant by the drive and cutoff controls.

2) Circuit operation

Fig. 4-8-1 shows a block diagram of the IC CXA1024S.

R, G, B signals supplied from the drive regulating circuit are input to pins 17, 18 and 19 of QP01, and then clamped by the internal reference voltage Vref1 (pin 1) to be input to the video switch circuits. AKB reference signal which is added to video signal according to the insertion timing determined by the timing control process circuit is output from the video switch to the auto white balance circuits.

The auto white balance circuits performs gain control and level shifting of CRT cathode currents that are respectively input through the IK CUT OFF terminals (pins 33, 39, 44) and the IK DRIVE terminals (pins 35, 40, 45) in order to maintain the CRT cathode current in the same amount.

Fig. 4-8-2 shows a system block diagram of the AKB circuit while Fig. 4-8-3 shows the timing chart.

Before video signal which the AKB reference signal is inserted in is output, its gain is controlled in the drive side while its level is shifted in the cutoff side. Video signal amplified by the video output circuit is detected as cathode current by the current detection transistor. This cathode current is converted into voltage by the detector resistors (RB, RW) and compared with the internal reference voltage Vref2 (pin 2) to be fed back in the form of gain control or level shifting. The feedback system is activated just in the period that the AKB reference signal is being inserted, and in the other period are the gain and level held as they are.

Moreover, the cathode current flows in one of the two lines according to the SW signal, one is I_{KB} (indicated by solid line in Fig. 4-8-2) in the cutoff period and the other is I_{KW} (broken line in the figure) in the drive period.

In this video projection system, the gain of the video output circuit and the detection resistance are determined so that all the R, G, B systems are operated with the center value of the gain of the AKB IC and level shifting operation. The actuating point of the circuit can be adjusted with the screen VR.

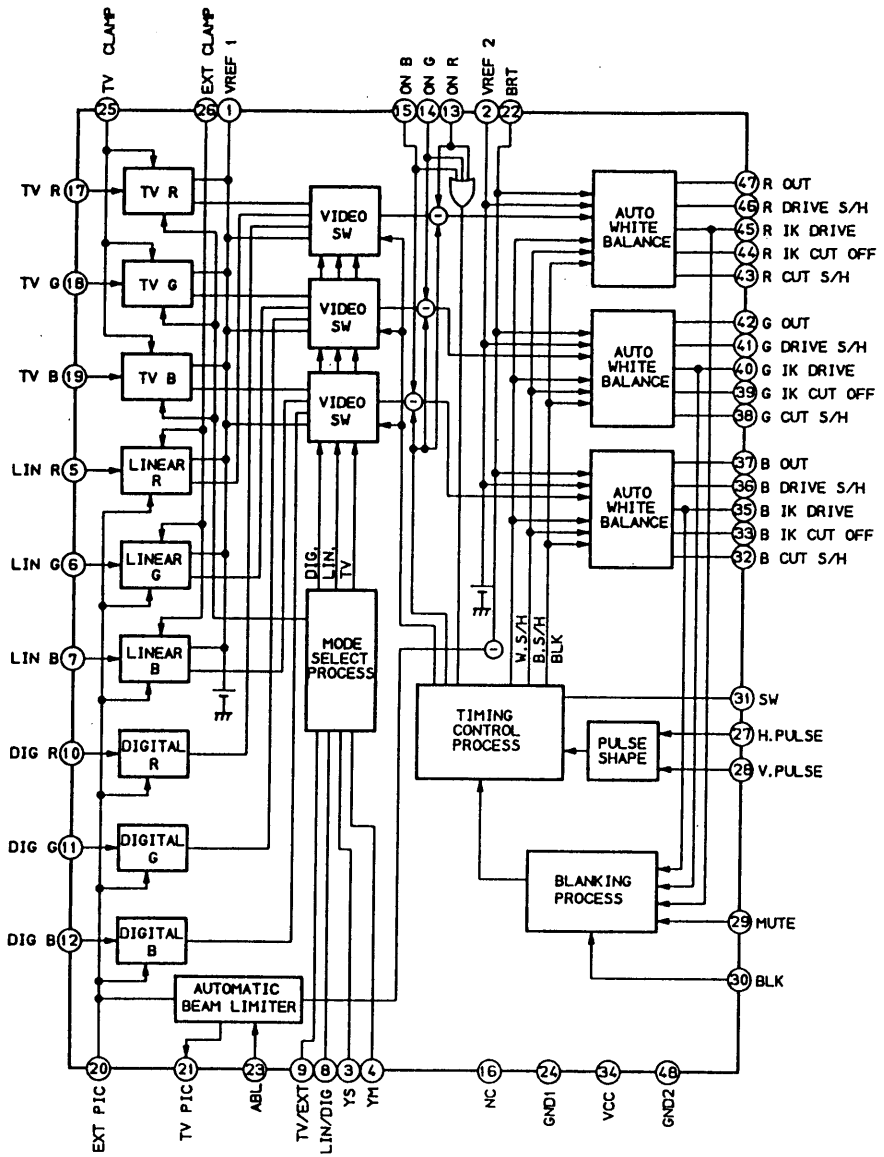


Fig. 4-8-1 CXA1024S block diagram

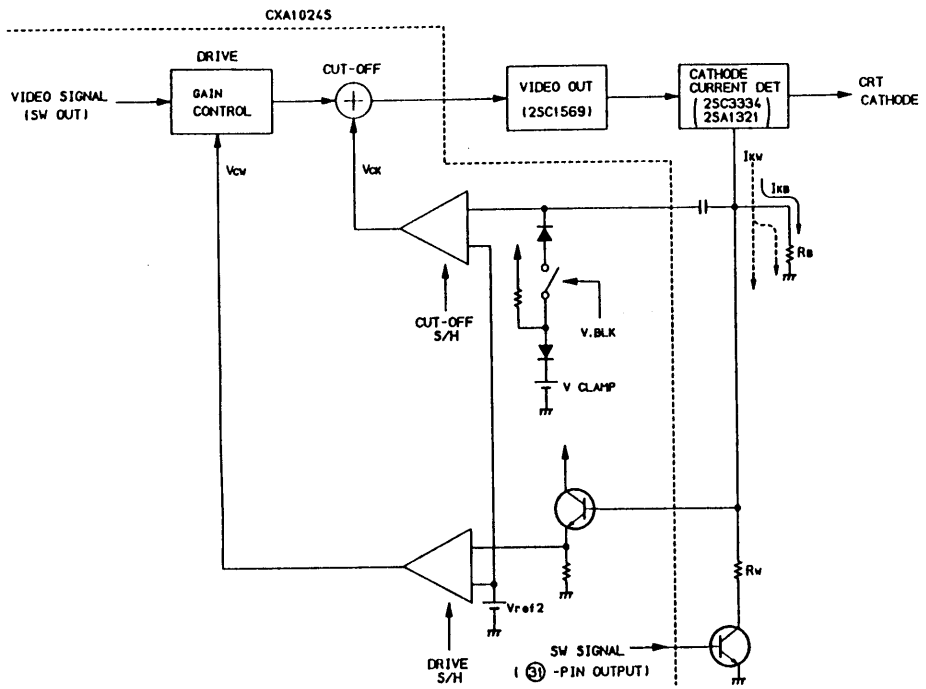


Fig. 4-8-2 AKB system block diagram

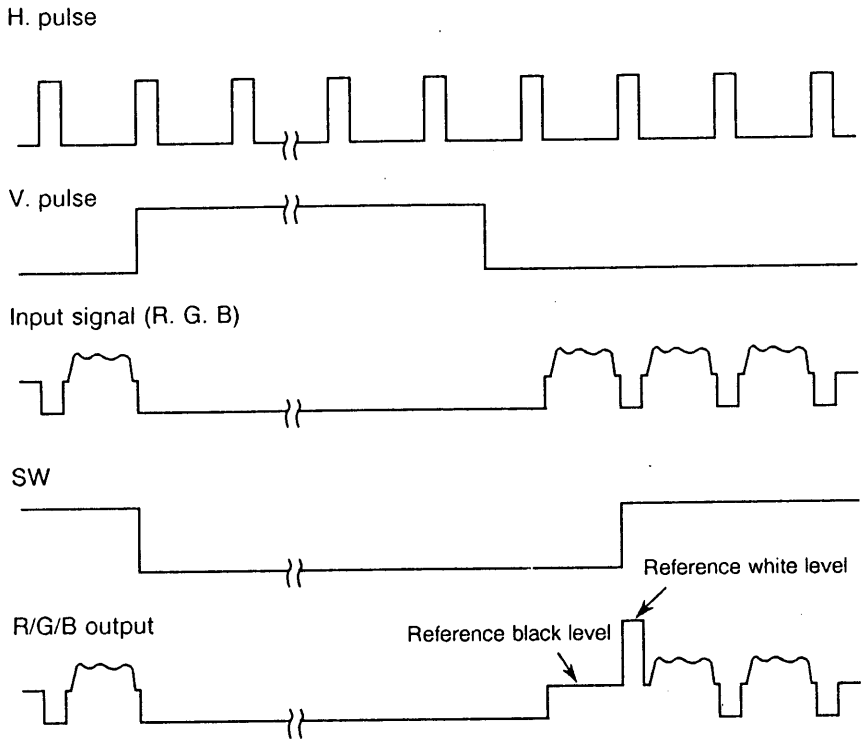


Fig. 4-8-3

4-9. CRT DRIVE CIRCUIT

1) Outline

The CRT drive circuit amplifies R, G, B signals supplied from the AKB circuit up to the amplitude required to drive the CRT while it detects CRT cathode current necessary for AKB processing.

The amplifier circuit which is constructed by general cascade connection has the additionally installed SEEP output buffer circuit for extension of the band width as well as for CRT cathode current.

2) Circuit operation

The CRT drive circuit for the G signal is shown in Fig. 4-9-1 by way of example.

G signal input from the AKB circuit is supplied to the base of Q909. This G signal is inversely amplified by Q909 and Q903 (in cascade connection) and then supplied to Q923 and Q926.

The gain of the CRT drive circuit is roughly expressed by (R906//R909//R974)/(R937//R934).

Q923 and Q926 compose the SEEP output buffer circuit, which supplies the amplified G signal to the CRT cathode while detects Q926's collector current as CRT cathode current. The detected CRT cathode current is converted into voltage by the detection resistors R986 and R992, and then supplied through Q929 to the AKB circuit.

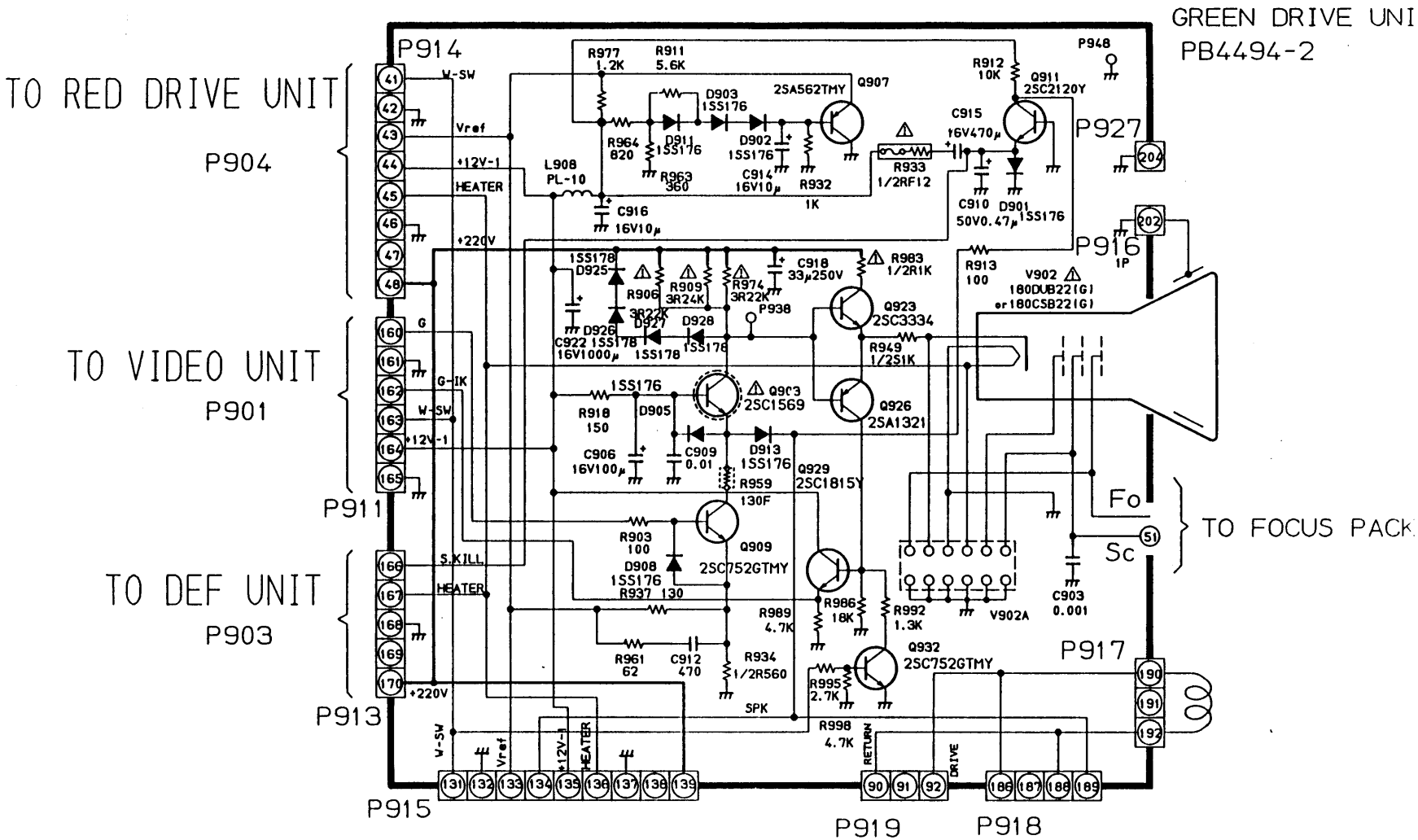

GREEN DRIVE UNI
PB4494-2
TO RED DRIVE UNIT
P904
TO VIDEO UNIT
P901
TO DEF UNIT
P903
TO FOCUS PACK
P914
P911
P913
P915
P919
P918
P917
P916
P927
P948
P938
P902A
W-SW
Vref
+12V-1
HEATER
+220V
G
G-IK
S.KILL
Fo
Sc
R977 1.2K
R911 5.6K
R912 10K
R964 820
R963 360
R932 1K
R933 1/2RF12
R913 100
R903 100
R918 150
R906 3R24K
R909 3R24K
R974 3R22K
R959 130F
R937 130
R961 62
R912 470
R934 1/2R560
R989 4.7K
R986 18K
R992 1.3K
R995 2.7K
R998 4.7K
R949 1/2S1K
R983 1/2R1K
C916 16V10μ
C914 16V10μ
C915 16V470μ
C910 50V0.47μ
C922 16V1000μ
C918 33μ250V
C906 16V100μ
C909 0.01
C903 0.001
D903 1SS176
D911 1SS176
D902 1SS176
D901 1SS176
D925 1SS178
D926 1SS178
D927 1SS178
D928 1SS176
D905 1SS176
D913 1SS176
D908 1SS176
Q907 2SA562TMY
Q911 2SC2120Y
Q923 2SC3334
Q903 2SC1569
Q926 2SA1321
Q929 2SC1815Y
Q909 2SC752GTMY
Q932 2SC752GTMY
L908 PL-10
V902 180DUB221(G) or 180C5B221(G)
RETURN
DRIVE

Fig. 4-9-1

4-10. ABL INTERLOCKING CIRCUIT

1) Outline

If ABL operation is individually performed for every unit in the multi-screen system, it brings about different brightness among the screens even in portions of the same video level. To avoid the system from such the problem, all the screens are controlled to have the same brightness with the lowest ABL voltage that is obtained as a result of comparison of the ABL voltages of all projection units.

Moreover, an adjustable offset voltage is added to all the ABL voltages so that the operation point of every projection unit accords with each other.

2) Circuit operation

(1) ABL interlocking

A block diagram of the ABL interlocking circuit is shown in Fig. 4-10-1. ABL return voltage supplied from the FBT is input through Q211 to the base of Q212, while it is also connected with external ABL voltage (EXT. ABL) via the switch QP06 for comparing the two voltages. When the EXT. ABL voltage is lower, Q211 is cut off and the EXT. ABL voltage passes through Q212, Q214, Q215 to turn down the voltage of the contrast and brightness terminals of the V/C/D IC (TA8845AN). As a result, the brightness is controlled to turn down. On the other hand, when the EXT. ABL voltage is higher, the same operation is performed by the circuit for the external ABL voltage.

(2) ABL voltage regulation

Even when video signal of the same brightness level is input to each projection unit, some units may have different brightness (dark in general) as a result of the ABL interlocking operation with different ABL voltages. Therefore, it is required to adjust the ABL voltage in order to make each unit have the same operation point.

In this projection system, an adjustable offset voltage is added to the ABL voltage of every projection unit as mentioned above, and the ABL voltage is regulated by adjusting the offset voltage. This operation is explained below.

R295, R296 and Q213 are supplied with the offset voltage, while a control voltage is supplied to the base of Q213 from pin 4 (ABL LEVEL) of QA22 of the D-A converter. The dropdown portion of the voltage at R295 can be varied as the offset voltage by the control voltage.

Fig. 4-10-2 shows the control characteristic. With increase of the control voltage, the offset voltage becomes low and the ABL return voltage is accordingly turned down. On the other hand, with decrease of the control voltage, the offset voltage becomes high and the ABL return voltage is accordingly turned up.

The ABL voltage of every projection unit is regulated as mentioned above.

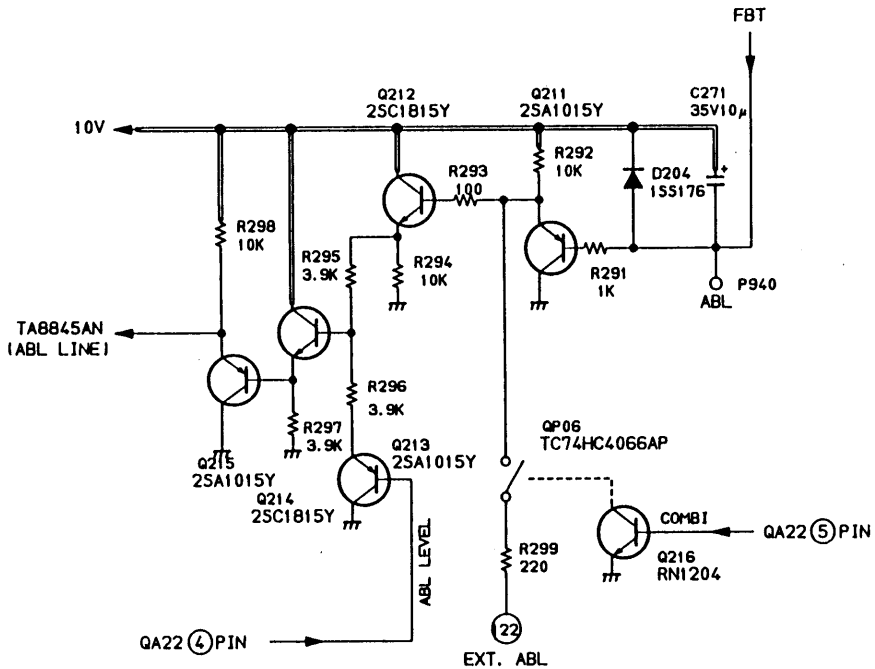


Fig. 4-10-1

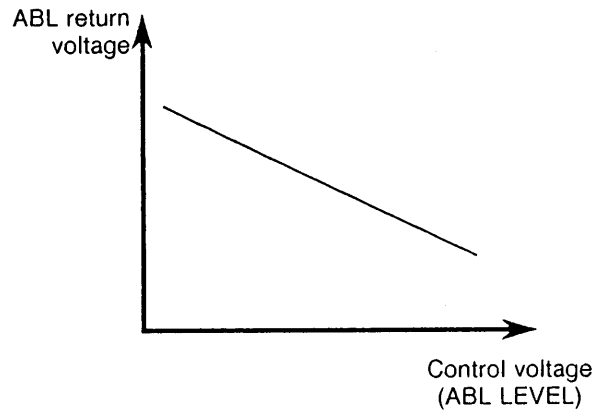


Fig. 4-10-2

SECTION 5.

VERTICAL DEFLECTION CIRCUIT

5-1. OUTLINE OF VERTICAL DEFLECTION CIRCUIT

5-1-1. Comparison Between Model CX32C81

The vertical deflection circuit of the TP48C51 is basically the same as that of N2DB chassis (CX32C81) but differs in following points.

(1) Three deflection yokes are provided because of three projection tubes used.

(2) Protection circuit is provided to prevent fluorescent surfaces from burning when the deflection stops (horizontal one line).

(3) Vertical linearity can be adjusted.

(4) Vertical output circuit is of a discrete type.

The basic circuit consists of Q501 (TA8845AN) containing a sync circuit, Q390 (TA75558S) containing a sawtooth wave generation circuit, differential amplifiers, and general op. amplifiers, Q301 driver transistor, and Q302, Q303 output transistors.

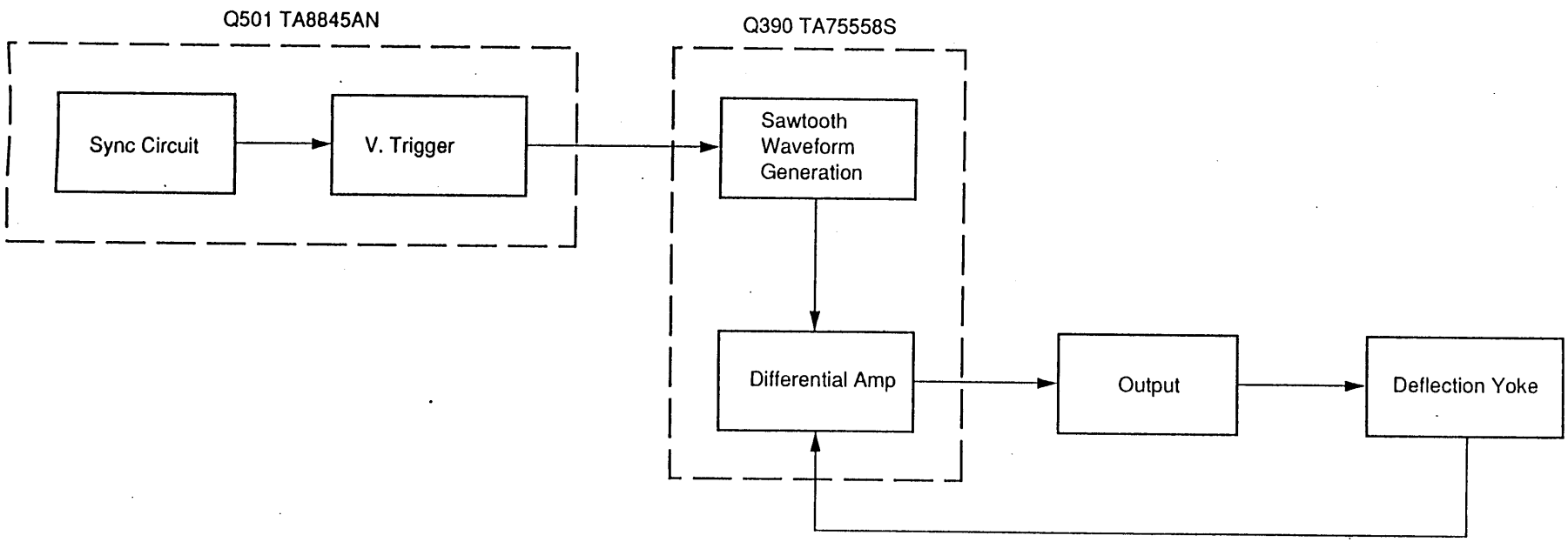


Fig. 5-1

5-2-1. Basic Theory of Operation

The V deflection circuit works to supply a sawtooth wave current with good linearity to the V deflection coil in synchronization with the V period.

In Fig. 5-2, when a sync pulse enters, the switch S turns on and C_1 is charged up to a reference voltage Vp. Next when the switch S turns off, the electrical charges in the capacitor charged up to the reference Vp is discharged at a constant current rate, and a reference sawtooth wave develops at point (a). This voltage is fed to + side (non inverting input side) of the differential amplifier A. At the same time, the current flowing into the deflection yoke is converted into a voltage in passing through a feedback resistor R2 and the voltage is fed back to – side (inverting input terminal) of the amplifier A.

If amplification factor of amplifier A is sufficiently high, V1 = V2 by assuming an imaginary short. That is, when the current of deflection coil is assumed as Iy, the deflection current Iy flows so that V1 = V2 = Iy • R3 is maintained.

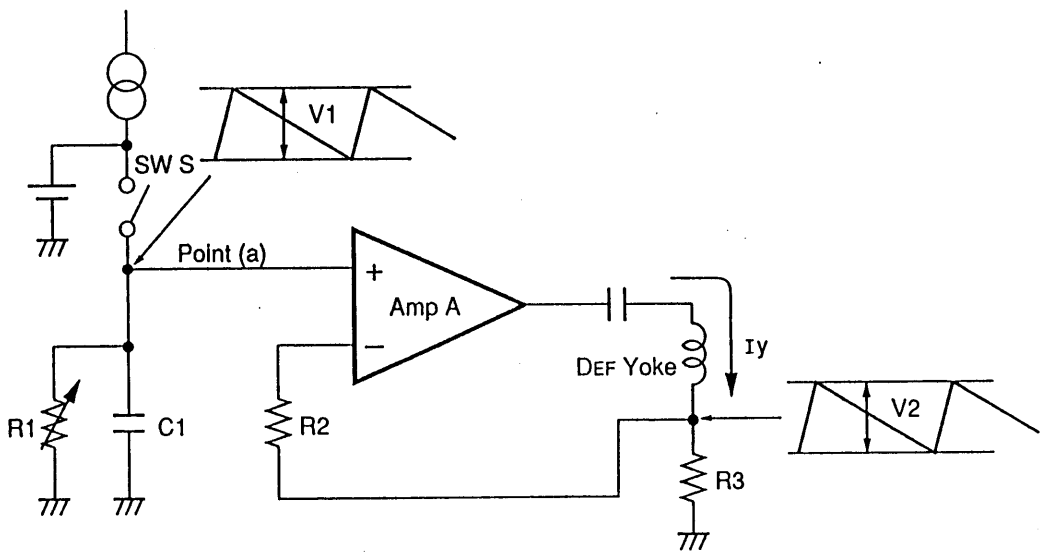


Fig. 5-2

5-2. V DEFLECTION CIRCUIT

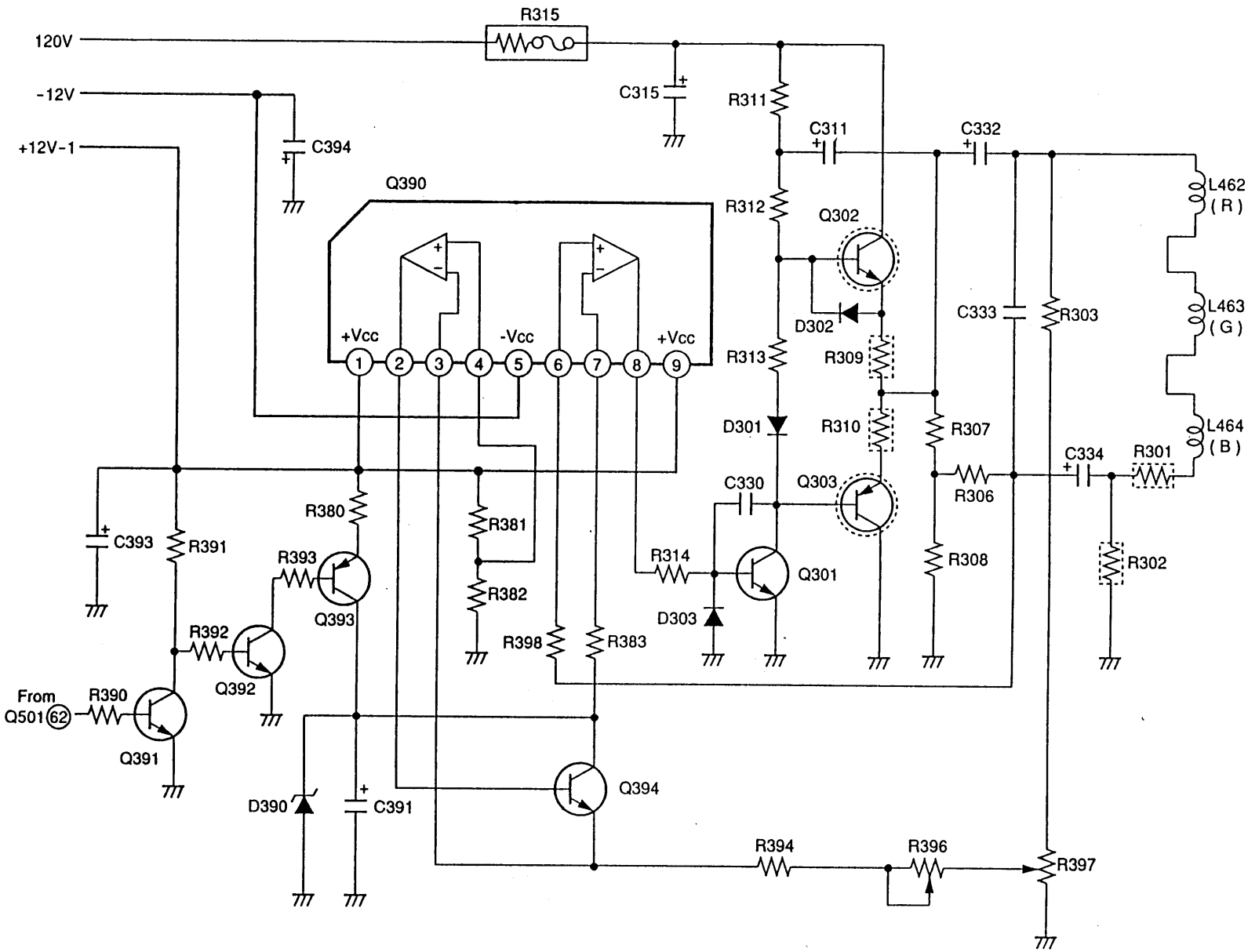


Fig. 5-3

5-2-1. Reference Saw-Tooth Waveform Voltage Generation Circuit

The sawtooth wave generation circuit has a configuration shown in Fig. 5-4.

During the V output pulse period, switch S_1 (Q393) turns on and the capacitor C391 is charged up to the reference voltage, and then when the S_1 opens at end of the V flyback period, the electric charges stored in C391 is discharged as a constant current rate through Q394. As a result, the voltage across C391 proportionally drops with time, thus developing the reference sawtooth wave voltage.

The sawtooth wave voltage obtained in this way is compared and amplified in the op. (differential) amplifier Q390.

In practice, the V height adjustment VR is not grounded, but the sawtooth wave voltage obtained in the output circuit is applied for correction of the linearity. Adjustment of the linearity is carried out by adjusting the amount of correction.

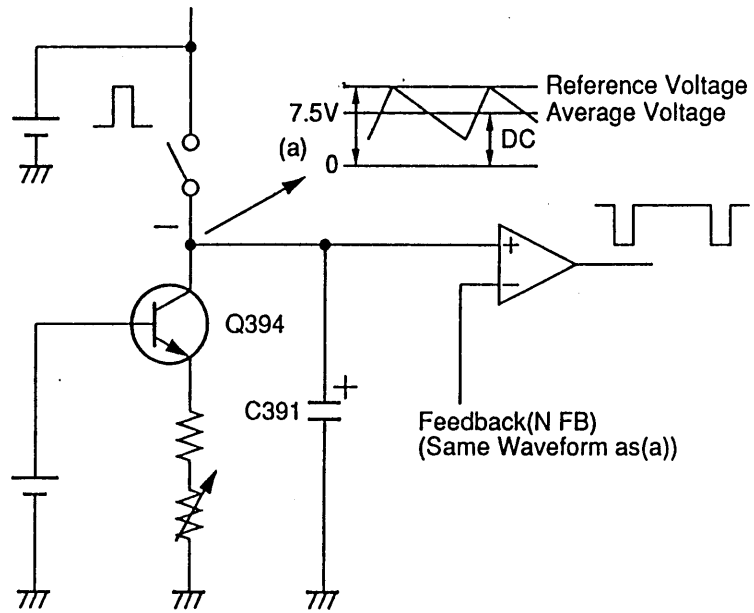


Fig. 5-4

5-2-2. V Output Circuit

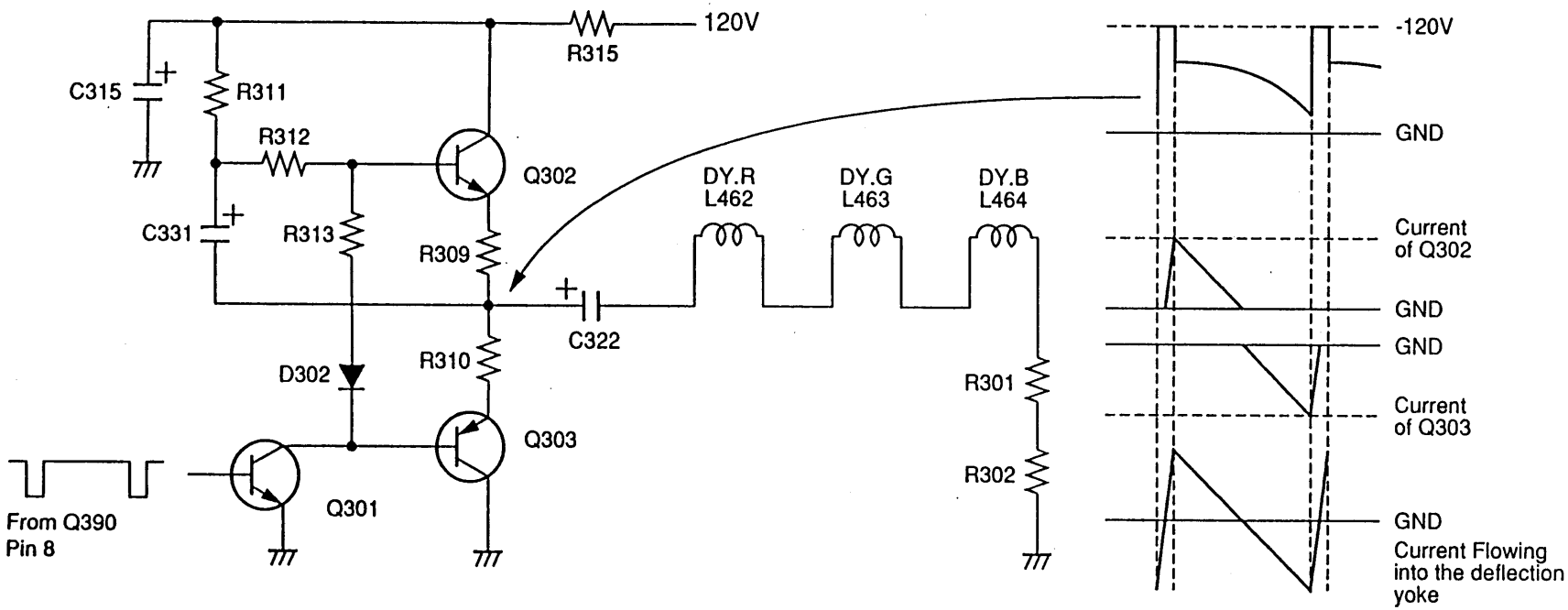


Fig. 5-5

The V output circuit supplies the sawtooth wave current to the V windings of the deflection yokes.

A signal entered through pin 8 of Q390 is amplified by Q301 drive transistor, and then SEPP type output stage consisting of Q302 and Q303 amplifies the sawtooth wave current and the current amplified flows into the deflection yokes L462, L463 and L464.

Q302 performs amplification for a half of the scanning and supplies a positive current to the deflection yokes and Q303 performs amplification for the later half of the scanning and supplies a negative current to the deflection yokes. These operations are shown in Fig. 5-5.

5-2-3. Linearity Correction and Adjustment Circuit

(1) S character correction (expansion at upper and lower ends of the screen)

Since a sawtooth wave current flows into the output capacitor C332, a parabola voltage develops across the capacitor. This voltage is integrated with R307, R308, R306 and C334 to create a S character voltage. The S character voltage is fed back to the non inverting input to make the linearity correction.

(2) When obtaining the S character voltage just stated above, the integration circuit consisting of R307, R308, R306, and C305 also integrates the parabola voltage containing the sawtooth wave voltage across R302, and the resultant parabola voltage is also fed back. Under this condition the screen is compressed at upper side and expanded at lower side. To correct this, a sawtooth wave voltage component obtained across the deflection yoke is divided with R303 and R397 and fed back as an inverted input through R396 and R394. In other word, the sawtooth wave current component caused by the sawtooth wave voltage described here is also contained in the discharge current of C391 (refer to Fig. 5-4) used in the reference sawtooth wave voltage generation, and the parabola component voltage is developed across C391 and this works to cancel the parabola component fed back to the non inverting input, thus correcting the linearity. R397 is a variable resistor and varies amount of the sawtooth wave voltage component applied to the non inverting input terminal, thereby adjusting the linearity balance at upper and lower screen.

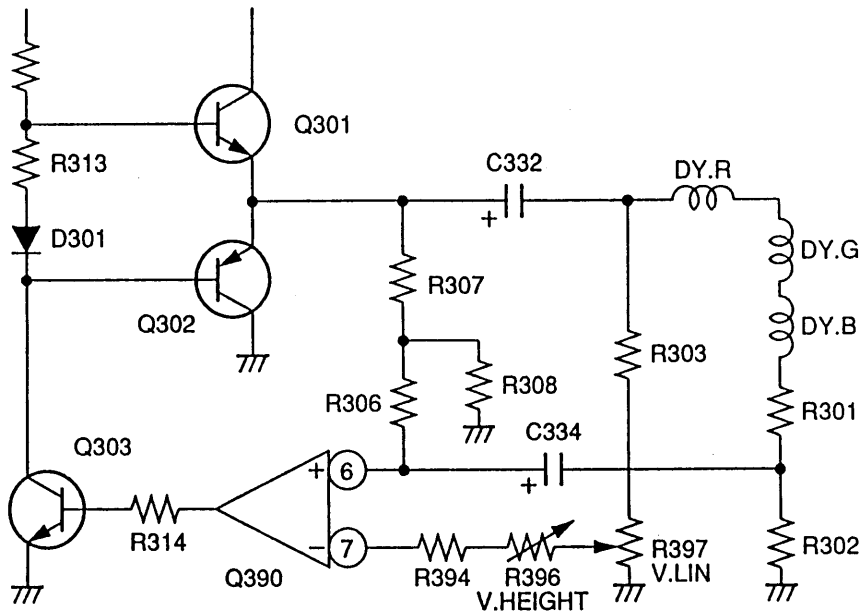


Fig. 5-6

5-3. PROTECTION CIRCUIT FOR V DEFLECTION STOP

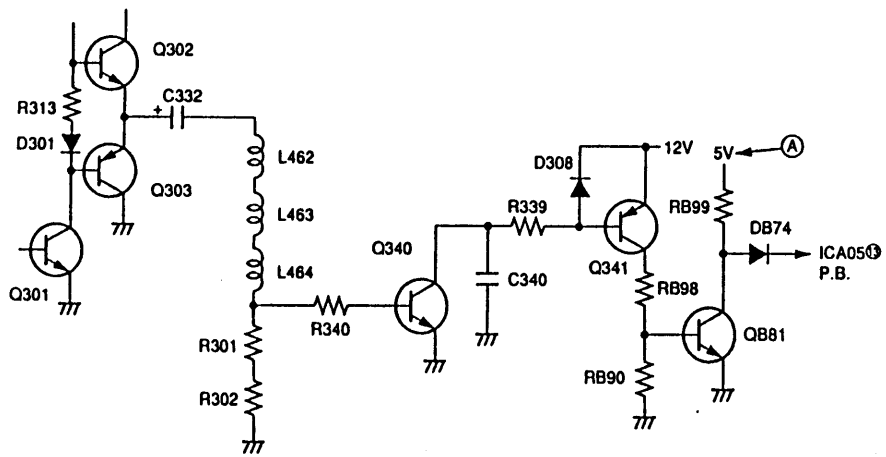


Fig. 5-7

When the deflection current is not supplied to the deflection coils, one horizontal line appears on the screen. If this condition is not continued for a long time, no trouble will occur in a conventional TV. But in the projection TV, all the electron beams are directly concentrated at the fluorescent screen because of no shadow mask used, and burns out the screen instantly.

To prevent this, the stop of the V deflection is detected when the horizontal one line occurs, and the video signals are blanked out so that the electron beams are not emitted.

When the V deflection circuit is operating normally, a sawtooth wave voltage is obtained across (R301 + R302), so Q340 repeats on-off operation in cycle of V sync. In this case, the collector voltage of Q340 is set to develop less than (12V – V_{BE} (Q341)) with R339 and C340 as shown in Fig. 5-8. Accordingly, Q341 and QB81 are continuously turned on. As a result, diode DB74 is turned off, giving no influence on the blanking operation.

Next, when the V deflection stops, the voltage across (R301 + R302) does not develop, so Q340 turns off, and both the Q341 and QB81 are turned off. Then, the picture blanking terminal pin 13 of ICA05 is set to high through RB99 and DB74 connected to 5V power line, thus cutting off the projection tubes. In this case, the 5V marked (A) is supplied from a separate power line not relating to the V deflection circuit so that the protection circuit will operate in any trouble mode.

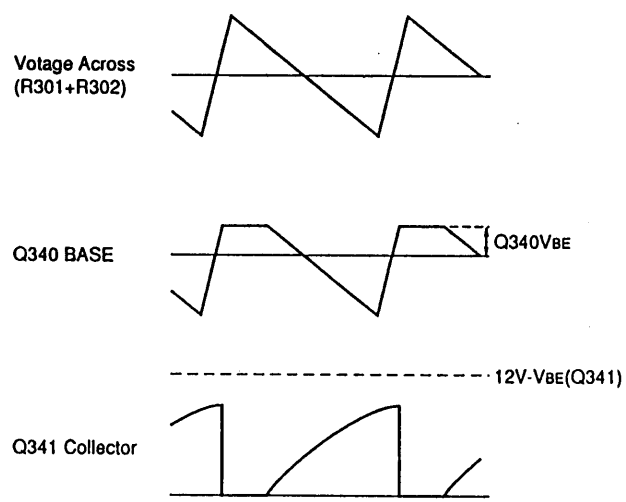


Fig. 5-8

5-4. OUTLINE OF HORIZONTAL DEFLECTION CIRCUIT

The horizontal (H) deflection circuit provides a sawtooth wave current of 15.734 kHz to the horizontal deflection coils to deflect electron beams from left to right horizontally on the screen.

Circuit configuration and ICs used for the synchronization and horizontal oscillator circuit are the same as those of N2DB (CX32C81).

Major differences from N2DB are as follows.

(1) Three deflection yokes are used as three projection tubes are used, and three yokes are connected in parallel and a same deflection current is supplied. (V deflection coils are connected in series).

(2) High voltage circuit and the H output circuit are separated. Accordingly, electrically speaking, the H output transformer is the same as a conventional FBT with a high voltage winding removed and the structure of the transformer is the same as that of a converter transformer used in the power circuit. That is, a pulse transformer is used.

(3) H amplitude adjustment coil is provided to adjust the H height.
In N2DB a diode modulator system is employed to adjust left and right pin cushion distortion correction and H height. But in TP48C51, the left and right pin cushion distortion is corrected in the convergence circuit and the height adjustment is carried out with the height adjustment coil.

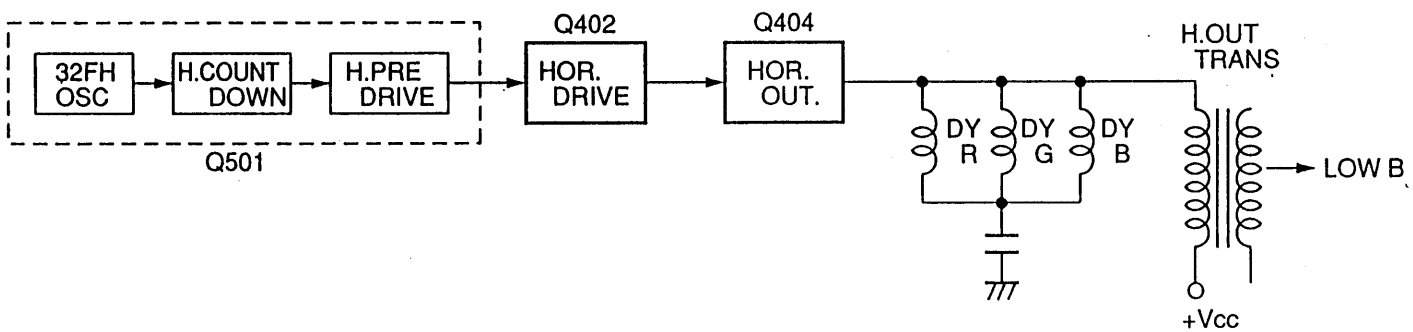


Fig. 5-9 Block diagram of H deflection circuit

5-5. THEORY OF OPERATION (N2DB)

5-5-1. Horizontal Start Circuit

The horizontal start circuit is provided to start the H output circuit by applying a bias voltage to pin 7 of Q501 (TA8845AN) (power supply for the horizontal system) at the power on.

When the power is on, first, the main power line 115V and +15V for Low + B rise at the same time. The 15V is applied to pin 7 of Q501 through R341 and drives the H oscillator circuit.

At the same time, a base current flows into the base of Q402 H drive transistor from pin 8 of Q501 and operates the H drive circuit which in turn drives the H output circuit.

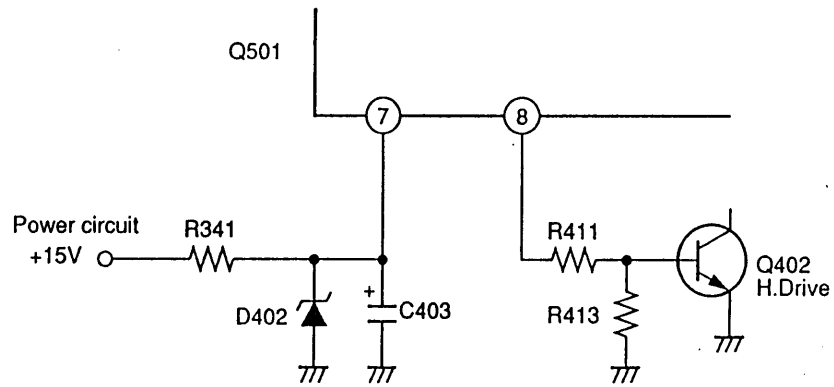


Fig. 5-10 H start circuit

5-5-2. H Drive Circuit

A collector current of the H output transistor is a heavy current as much as several amperes and such heavy current is not driven directly with the output pulse of the H oscillator circuit. So, a drive circuit is provided between the oscillator circuit and the output circuit. The drive circuit amplifies the current in addition to stabilize the output transistor.

The transistor Q_1 inside Q501 repeats on-off operation for the horizontal period and a rectangular pulse with the horizontal period is developed at pin 8 of Q501. When pin 7 (H predrive) of Q501 output develops a forward bias (Q_1 is on), Q402 base is forward-biased through 15V → R341 → pin 7 of Q501 (H.Vcc) → pin 8 of Q501 (H.out) → R411/R413 (resistor divider), and a Q402 collector current flows in passing through 120V → R146//R417 → T401. As a result, an energy is stored in the primary winding of the drive transformer T401.

Under this condition, the H output transistor Q404 is turned off because of its base-emitter is reverse-biased.

Next, when pin 8 is 0V (Q501 is off), the base-emitter of Q402 goes 0V and Q402 is turned off, and a high pulse voltage is developed at the collector of Q402 or the primary winding of T401 by the energy stored in the step just preceding.

The winding ratio between the primary winding and the secondary winding of the drive transformer is as large as 30 : 1, that is, as the winding number of the primary winding is large, the pulse voltage applied to the secondary winding or across the base-emitter of the output transistor is stepped down, but the transmitted energy is the same, so, a sufficient base current can flow into Q404 base.

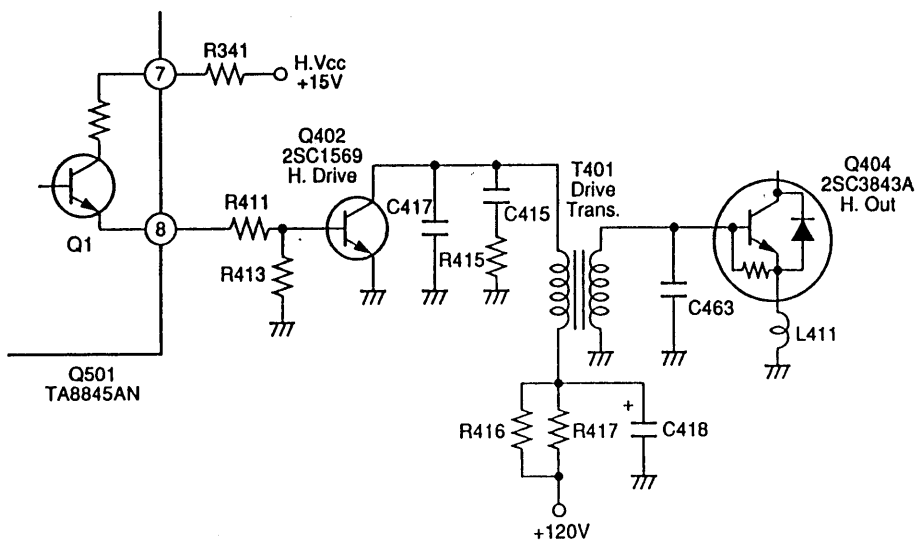


Fig. 5-11 H drive circuit

5-5-3. H Output Circuit

The H output circuit applies the sawtooth wave current of 15.734 kHz current to the H deflection coil by using a mutual switching effect of the H output transistor and a damper diode to deflect the electron beams in horizontal direction.

Moreover, it rectifies a pulse output developed at the output transformer and creates power supply voltages to be supplied to various circuits.

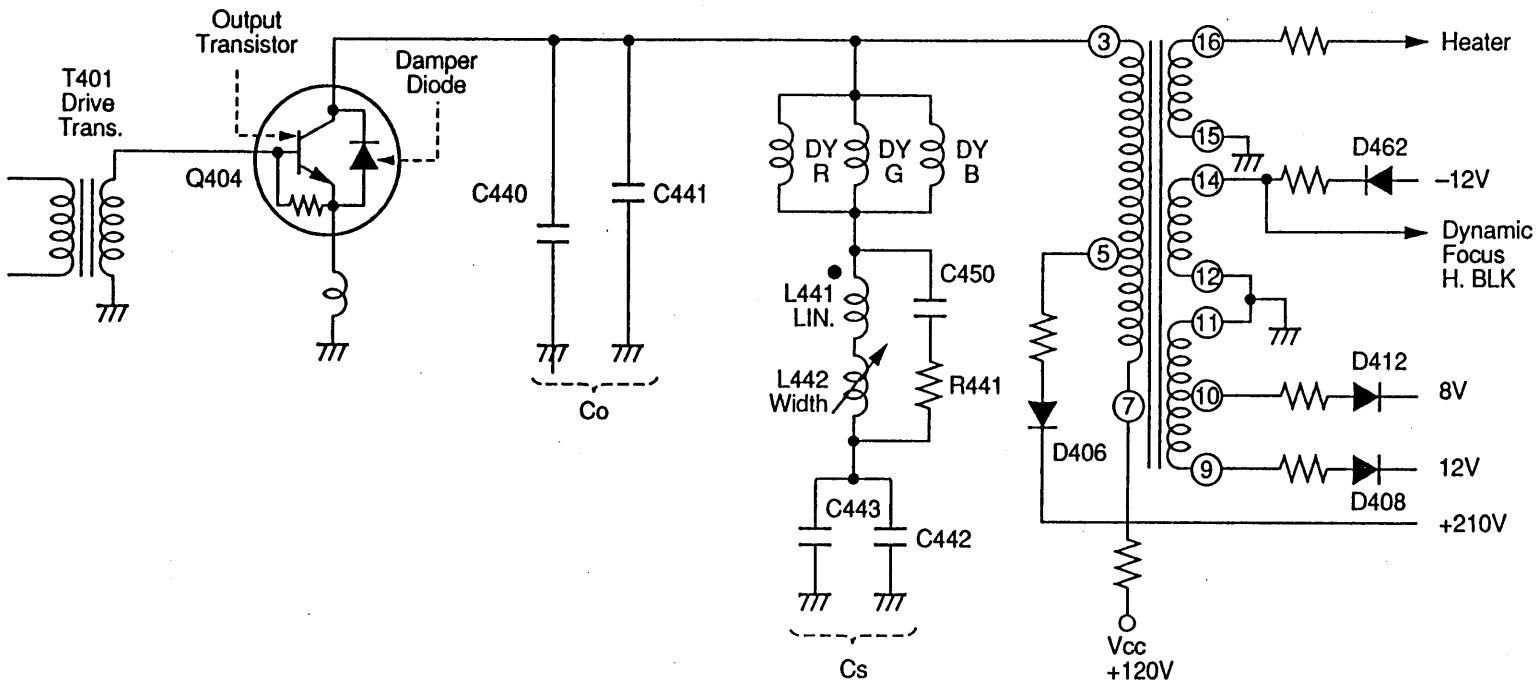
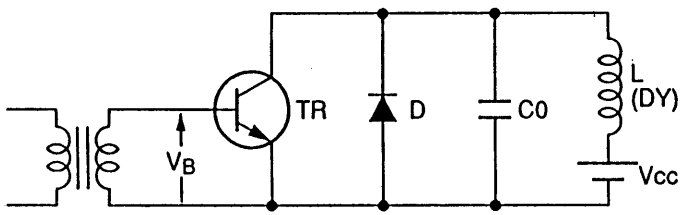


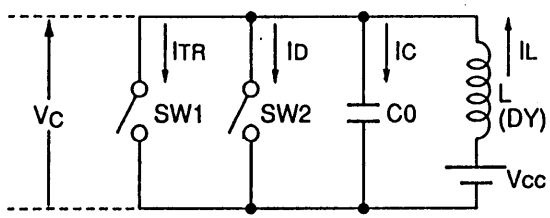
Fig. 5-12 H Output Circuit

5-5-3-1. Operation of basic circuit

Theory of the basic operation will be understood by referring to Fig. 5-13 (a) and (b). The H output circuit shown in Fig. 5-12 can be simplified as shown in Fig.5-13 (a). Moreover, as the output transistor and the damper diode perform switching operations, they can be expressed as shown in Fig.5-13(b).



(a) Basic circuit



(b) Equivalent circuit

Fig. 5-13

Fig. 5-14 shows basic operation waveforms.

(1) $t_1 \sim t_2$

The drive circuit applies a positive pulse to base of the output transistor, a forward base current is flowing, and the output transistor (SW1) is turned on up to a sufficiently saturated level. As a result, the collector voltage lowers to nearly equal to the ground potential (0V) and the deflection current flowing into L increases proportionally from zero with time. The current reaches maximum at t_2, and a right half of picture is scanned up to this period.

(2) t_2

The base drive voltage rapidly changes to negative at t_2 and the base current becomes zero. The output transistor turns off, collector current reduces to zero, and the deflection current stops to increase.

(3) $t_2 \sim t_3$

The output transistor turns off at t_2, but the deflection current can not reduce to zero immediately because of inherent nature of the coil and continues to flow, gradually decreasing by charging the resonant capacitor C_0. On the other hand, the voltage at Co or the collector voltage is slowly increases and reaches a maximum value at time t_3. At the same time, the deflection current goes zero.

Under this condition, all the electro-magnetic energy stored in the deflection coil up to t_2 is converted into a static energy in the resonant capacitor.

As can be seen from above description, the left half operation of the horizontal deflection is carried out with the current flowing through the damper diode and the right half with the horizontal transistor, and the deflection operation for the flyback period is carried out by the resonant current with both the damper diode and the output transistor deactivated.

Moreover, theoretically speaking, an energy is supplied from the power V_{CC} for the on-period of the H output transistor, but the energy is returned to the power source for the on-period of the damper. Both of these energy are theoretically the same, as a result, the power consumption in the H output circuit is zero. (In practice, the power consumption does not become zero because of a switching loss and losses caused by resistance components of the circuit parts, etc.)

5-5-3-2. H amplitude adjustment

The H amplitude can be varied by varying the current of the sawtooth wave flowing into the H deflection coil. In practice, this is carried out by varying inductance of the amplitude adjustment coil L442 connected in series with the H deflection coil. The inductance is varied by adjusting the screw core (changing relative position of the coil and the core) with an alignment screw driver.

5-5-3-3. H linearity correction

(1) S character correction (S character capacitor)

With the deflection angle of the projection tube increased, pictures at left and right on the screen will be expanded if a good linearity sawtooth wave current is applied to the deflection coil. This is caused because distance between center of the deflection magnetic field (a point where the electron beams are deflected by the deflection yoke) and the fluorescent screen is different at the screen center and the screen peripheral. That is, the distance increases at the peripheral area, so the picture becomes large if a good linearity deflection current is applied.

To correct this expansion at screen peripheral, the expansion of the deflection current corresponding to the peripheral must be suppressed. This is realized by superimposing a current of S character waveform on the basic sawtooth wave current. In practice, the S character capacitors (C442, C443) are connected in series with the deflection coil as shown in Fig.5-12.

The S character capacitors work to stop DC as well as to work as an equivalent power supply for the H output circuit. The basic waveform of the deflection current is a sawtooth wave and the current flows into the coil as well as into the S character capacitors. A voltage caused by integrating the flowing current is developed across the capacitors. That is, a voltage showing a parabola is developed across the S character capacitors.

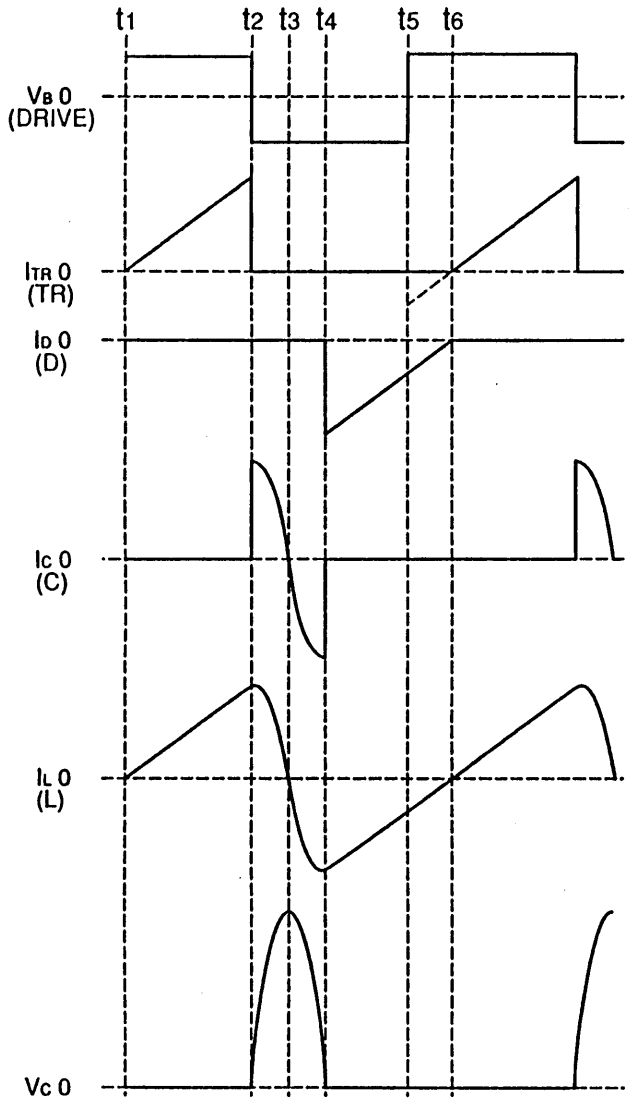


Fig. 5-14

(4) $t_3 \sim t_4$

Since the voltage charged in the resonant capacitor is discharged through the deflection coil, the deflection current increases in reverse direction and the capacitor voltage decreases slowly. This means the static energy in the resonant capacitor is converted into an electro-magnetic energy in the deflection coil.

(5) t_4

When discharging of the resonant capacitor completes and the collector voltage goes zero, the deflection current reaches the maximum in reverse direction. t_2-t_4 is the horizontal flyback period and electron beams are returned from right end to left end on the screen by the deflection current for this period. The operation in this period is carried out by a resonant phenomenon with L and Co, and the operation period is equivalent to the half period. The flyback period is determined by values of L and Co.

(6) $t_4 \sim t_6$

The resonant phenomenon caused for $t_2 \sim t_4$ is going to continue after t4. That is, the resonant capacitor is charged to a negative voltage and this provides a forward bias for the damper diode (SW2) automatically, thus the damper diode is turned on after t_4.

As a result, the deflection current proportionally decreases with time by charging the power (Vcc) through the damper diode and goes zero at time t_6. A left half of the screen is deflected for this period.

5-5-3-4. Power supply circuit for the H output circuit

A choke coil is required to supply the power voltage to the H output circuit. Generally speaking, the choke coil employs a transformer type with a secondary coil wound on the choke coil, and such transformer is called a FBT and used to develop a high voltage and lower voltage powers by rectifying the pulse voltage induced in the secondary coil. However, in TP48C51, the high voltage is made by a separate circuit, so the choke coil is used to develop only the lower voltage supplies.

The H transformer T462 is made by winding a primary coil and secondary coil on an EE type core and has the same structure as that of the converter transformer used in the power supply circuit. But it is called a pulse transformer to discriminate it from the FBT.

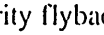
(1) Video output power supply

A positive flyback pulse voltage () obtained at pin 5 of the center tap of primary winding of T462 is rectified and filtered with D406 and C447, and added to +115V main power supply voltage, thereby developing +210V power voltage and supplying it to the video output circuit on the CRT drive P.C. board.

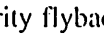
(2) Projection tube heater power supply

A pulse voltage obtained at pin 16 of secondary coil of T462 is directly, without rectifying, supplied to the heater electrode of the projection tube. In this case, the value of R469 is adjusted to provide the heater voltage of 6.3 Vrms.

(3) +12V winding

The negative polarity flyback pulse for scanning period () obtained at pin 9 of T462 is rectified and filtered with D408 and C449 to develop +12V power supply. The +12V supply is fed to the convergence circuit.

(4) +8V winding

The negative polarity flyback pulse for scanning period () obtained at pin 10 of T462 is rectified and filtered with D412 and C445 to develop +8V power supply.

The +8V power supply is fed to Q183 regulator circuit and becomes +5V regulated power supply. The +5V is supplied to the signal circuits on the main P.C. board.

(5) −12V power supply

The positive polarity pulse for scanning period () obtained at pin 14 of secondary winding of T462 is rectified and filtered with D462 and C466 to develop −12V power supply. This voltage is supplied to the convergence circuit. The positive polarity pulse obtained at pin 9 of secondary winding of T462 is supplied to the H blanking circuit and H dynamic focus circuit.

The parabola voltage component also becomes a part of the power supply voltage of Vcc for the H output circuit. As a result, a current with a cubic function waveform or the S character waveform developed by integrating parabola wave of the quadratic function flows into the deflection coil.

The amount of S character correction can be adjusted by varying voltage level of the parabola voltage or the capacitance of the S character capacitors, and set to the value so that the linearity at both the left and right ends of the screen and the center area of the screen shows a flat.

(2) Left and right asymmetry correction (LIN coil)

It is said under item 2-3-1 that "The deflection current changes proportionally with time." However, in practice, the current does not change proportionally and causes a distortion because of influence of resistance component of the deflection coil, collector current vs. saturation voltage characteristics of the collector-emitter, VF of the damper diode, etc. This distortion of the current waveform is of a type which lowers current increasing rate with time. So, the picture expands at left screen and shortens at the right.

To correct this, a linearity coil (LIN coil) which increases the inductance for a negative polarity deflection current (flowing through the damper diode) and decreases the inductance for a positive deflection current (flowing through the output transistor) is connected in series with the deflection coil.

The LIN coil is made by winding a coil on a ferrite core under a near saturating condition with a magnetic bias applied by a permanent magnet, and if direction of the magnetic flux induced by the current flowing into the coil is in the same direction as that of the permanent magnet, the core enters a saturating condition and the inductance decreases.

On the other hand, if the direction of the flux induced by the current is opposite that of the permanent magnet, magnetic permeability increases and the inductance increases. The actual characteristics of the coil depend on size of the core, flux density of the magnet, turn number of the coil, etc. and have been designed to give the best screen linearity.

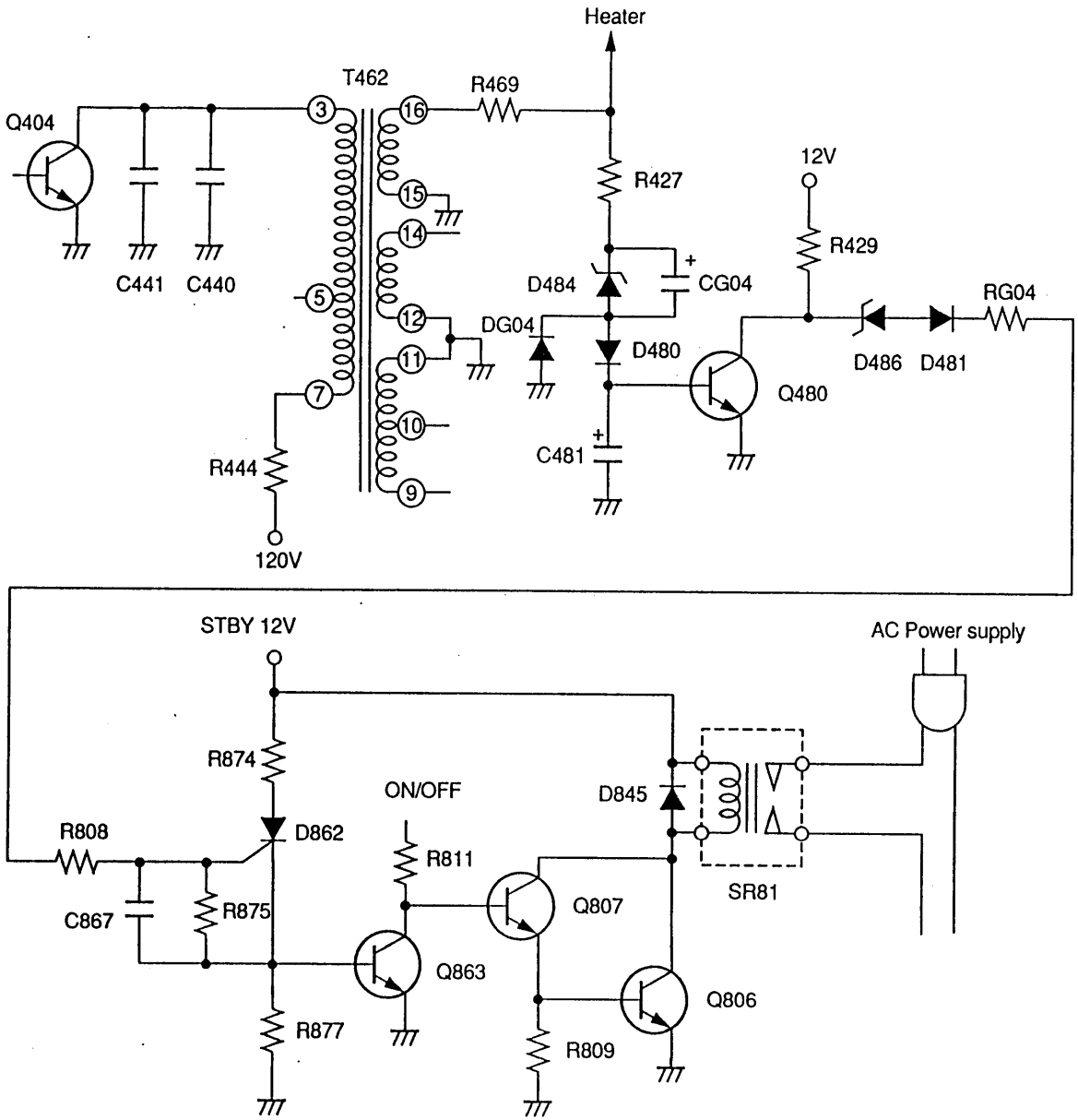

Heater
T462
R469
Q404
C441
C440
R427
12V
R429
D484
CG04
RG04
DG04
D480
D486
D481
Q480
C481
R444
120V
STBY 12V
AC Power supply
R874
ON/OFF
D845
R808
D862
R811
SR81
C867
R875
Q807
Q863
Q806
R877
R809

Fig. 5-15

5-5-4. Protection Circuit for H Output Circuit

If the H output circuit stops, followings will occur.

(1) The H deflection current stops to flow.

(2) Each voltage supplied from the pulse transformer T462 also stop.

If only the item (1) occurs, a "vertical one line" occurs. But if each voltage stops in (2), –12V for the op. amplifier Q390 in the V deflection circuit also stops and the vertical deflection is not conducted. As a result, electron beams concentrate as a spot on the screen and light up.

As previously described under the V deflection circuit, if the beams concentrate at the fluorescent screen of the projection tube of the projection TV, the fluorescent screen is burnt out.

To prevent this, the voltage at pin 16 of T462 pulse transformer is detected when the H output circuit stops, and the main power supply of the TV set is turned off.

This operation is described in more details by referring to Fig. 5-15.

Pin 16 of T462 develops a pulse of about 25 Vp-p in H sync when the H output circuit is working normally. The pulse is applied to the base of Q480 through R427, D484//CG04, D480, and Q480 is turned on. With Q480 turned on, Q480 collector is low. As a result, a thyristor D862 in the power supply circuit is not turned on, so, the relay SR81 is kept closed and the set works normally.

On the other hand when the H output circuit stops, the voltage at pin 16 of T462 disappears, Q480 turns off and collector of Q480 goes high. Since the collector voltage is applied to the gate of D862 thyristor in passing through D486, D481, RG04, so, D862 turns on, Q863 on → Q807, Q806 off, thus a current does not flow into the coil of relay SR81. That is the relay is opened and the main power supply of the set is turned off, thus protecting the projection tubes.

SECTION 6.

CONVERGENCE CIRCUIT

6-1. OUTLINE

The convergence circuit is composed of two P. C. boards of the CONV. CONT (PB4493) and the CONV. OUT (PB4487).

The CONV. CONT P.C. board (PB4493) to which HD synchronizing signal and VD synchronizing signal are input is composed of the correction signal generator circuit to output sawtooth waveform, parabolic waveform, etc., the gain control block to regulate the correction rate of various correction signals, and the composing circuit to add waveforms whose gains are adjusted to each other. A block diagram of the CONV. CONT circuit is shown in Fig. 6-1.

The CONV. OUT P.C. board (PB4487) is mainly composed of the correction current output block to output correction current to the convergence coil in six systems, since there are vertical output circuits and horizontal output circuits provided for R, G, B signals respectively. The output block employs hybrid ICs, each of which has a pack of output circuits for three channels. Moreover, the pump-up circuit, which changes supply voltage to the output circuits for the horizontal blanking period and for the horizontal scanning period, is employed to reduce power consumption of the hybrid ICs.

6-2. CORRECTION SIGNAL GENERATOR CIRCUIT

Convergence correction signals are generated by PA0036 and others based on the horizontal and vertical blanking pulses. Fig. 6-3 shows generated correction waveforms as numbered from 1 to 26, while Fig. 6-2 shows a schematic diagram of the correction signal generator circuit.

In Fig. 6-3, waveforms No. 6 (HS) and No. 4 (VS) are generated by two couples of the constant current generating circuits installed in the IC for horizontal and vertical scanning, and the circuits generate constant current to be supplied to the sawtooth waveform generator circuit. The constant current intensity of those circuits is determined by external resistors R1 and R2. C2 is an integrating capacitor installed outside the sawtooth waveform generator circuit for horizontal scanning, while C1 is an integrating capacitor installed outside the sawtooth waveform generator circuit for vertical scanning.

Waveforms No. 1 (VP) and No. 8 (HP) are generated by two couples of parabolic waveform generating circuits installed inside the IC for horizontal and vertical scanning, and those waveforms are basically obtained by integrating horizontal and vertical sawtooth waveforms.

Waveforms No. 5 (V3) and No. 7 (H3) are generated by two couples of tertiary waveforms generating circuits installed inside the IC for horizontal and vertical scanning, and those waveforms are basically obtained by integrating horizontal and vertical sawtooth waveforms.

Waveform No. 2 (V4) is generated by the biquadratic waveform generating circuit internally installed in the IC for vertical scanning. The vertical scanning biquadratic waveform is obtained by squaring the input of parabolic waveform with the multiplier.

Other waveforms from No. 9 through No. 26 are obtained by calculating the above-mentioned waveforms No. 1 to No. 8, which are used as the fundamental waveforms, with the multiplier.

Single-side correction waveforms, etc., are obtained by slicing and composing the fundamental waveforms No. 1 through No. 8 with the multiplier.

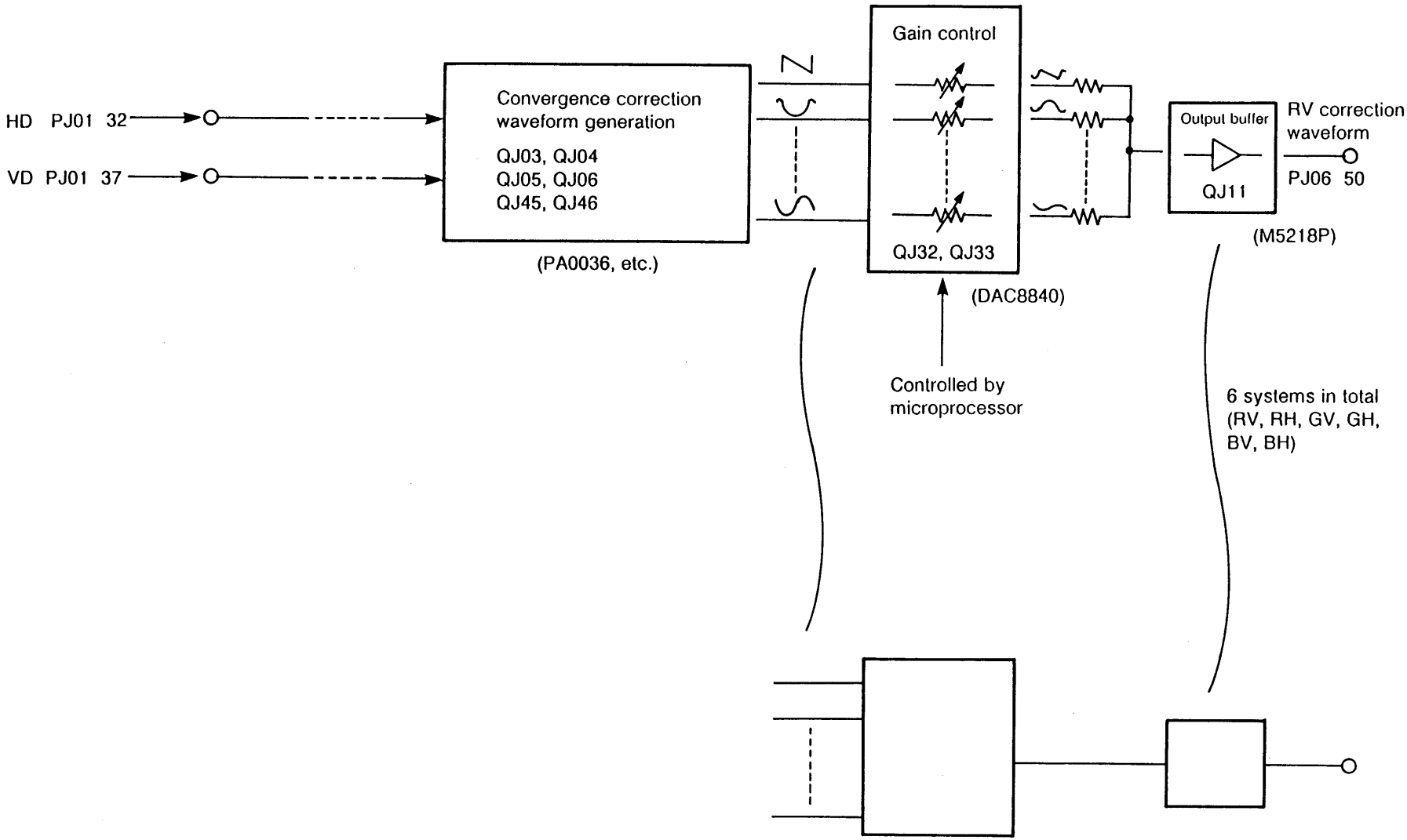


Fig. 6-1 CONV. CONT P.C. board block diagram

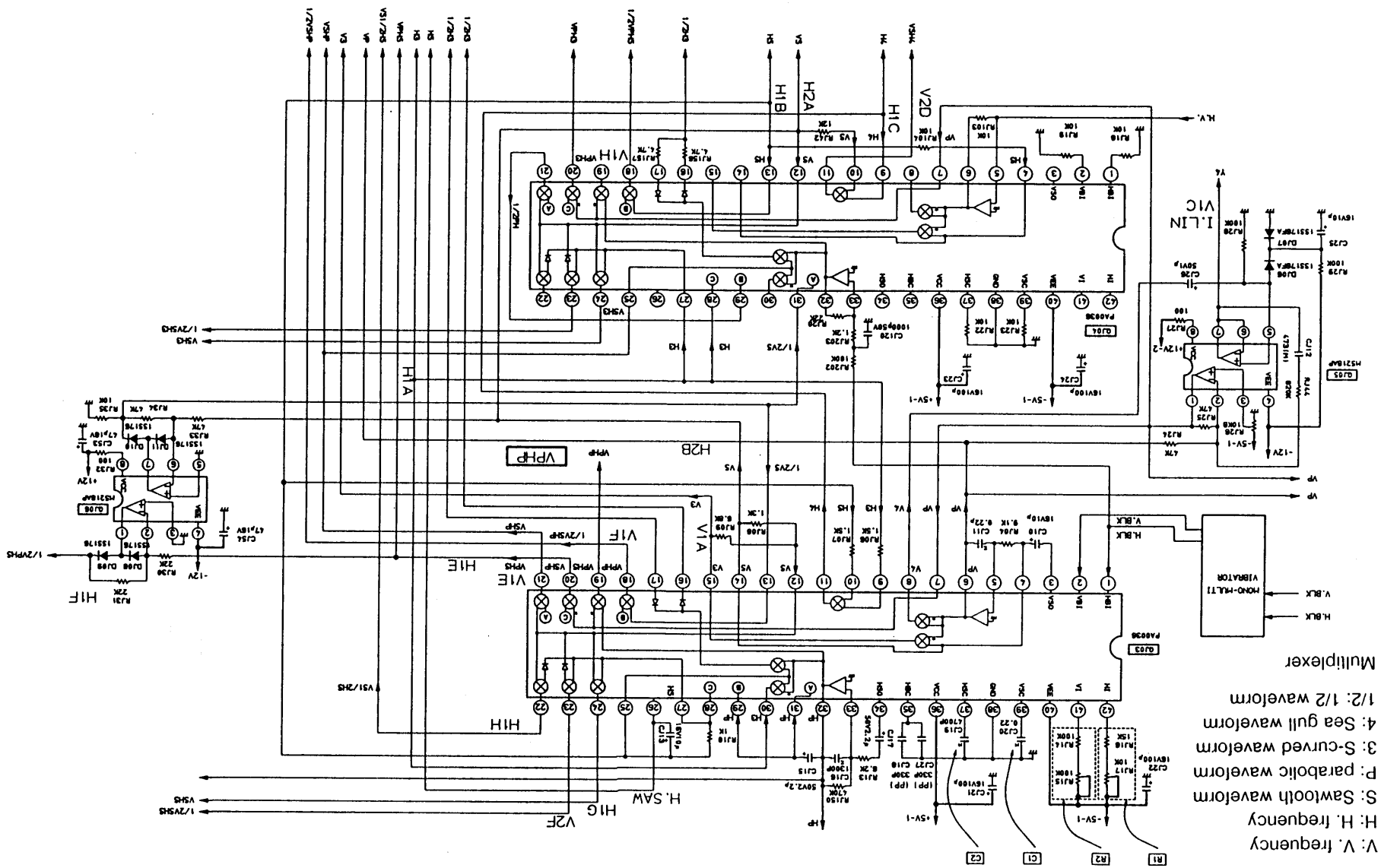
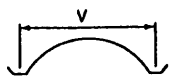
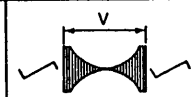
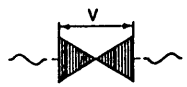
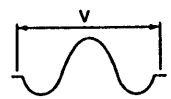
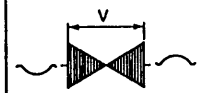
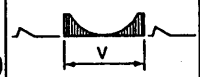
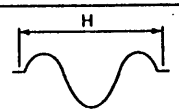
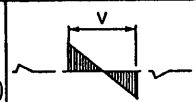
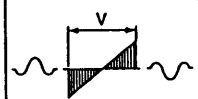
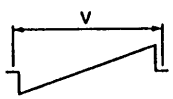
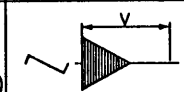
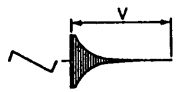
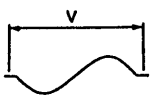
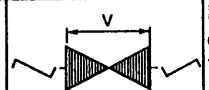
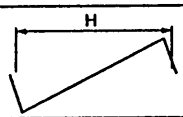
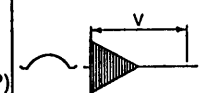
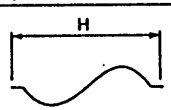
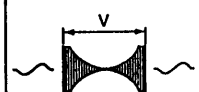
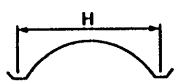
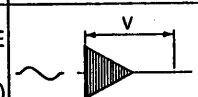


Fig. 6-2 Correction signal generator circuit

No	Name	Wave form	Raster correction	No	Name	Wave form	Raster correction	No	Name	Wave form	Raster correction
1	H-BOW V-O.LIN (VP)		H-bow distortion V-outside linear distortion	9	H-O.PIN V-O.KEY (VPHS)		H-outside pin-cushion distortion V-outside pedestal distortion	17	V-WAVE (VSH3)		V S charactor distortion
2	V-I.LIN (V4)		V-inside linear distortion	10	V-PIN (VSHP)		V-outside pin-cushion distortion	18	H-O.SPIN (1/2VPHS)		H-outside upper side pin-cushion distortion
3	H-I.LIN (H4)		H-inside linear distortion	11	H-SKEY (VS1/2HS)		H-left side pedestal distortion	19	V-WING (VSH4)		V-seagull distortion
4	H-TILT V-O.SIZE (VS)		H-tilt distortion V-outside amplitude distortion	12	V-I.SKEY (1/2VSHS)		V-inside upperside pedestal distortion	20	V-O.SKEY (1/2VPHS)		V-outside upper side pedestal distortion
5	V-I.SIZE (V3)		V-inside amplitude distortion	13	H-KEY V-I.KEY (VSHS)		H-pedestal distortion V-inside pedestal distortion				
6	H-O.SIZE V-TILT (HS)		H-outside amplitude distortion V-tilt distortion	14	V-SPIN (1/2VSHP)		V-upper side pin-cushion distortion				
7	H-I.SIZE (H3)		H-inside amplitude distortion	15	H-I.PIN (VPH3)		H-inside pin-cushion distortion				
8	H-O.LIN V-BOW (HP)		H-outside linear distortion	16	V-SWAVE (1/2VSH3)		V-upper side S character distortion				

Description of words in ( )

- V: V period correction wave
- H: H period correction wave
- 1/2: 1/2 correction wave
- S: Primary wave (saw tooth)
- P: Secondary wave (parabola)
- 3: 3rd wave (S character)
- 4: 4th wave (Seagull)

Fig. 6-3 Convergence correction signal waveforms (1/2)

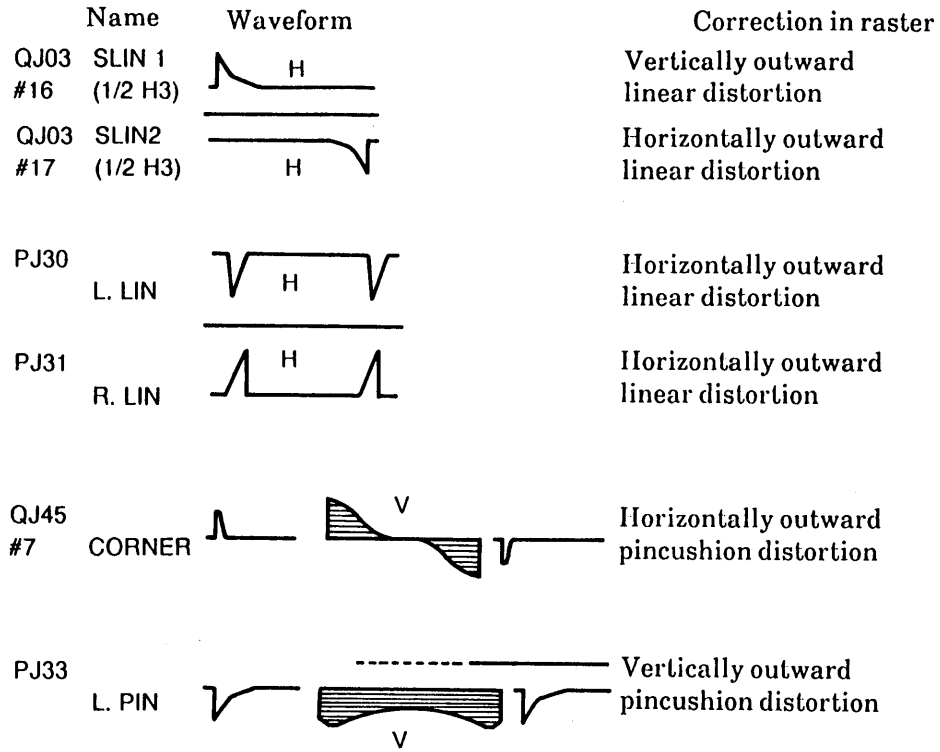


Fig. 6-3 Convergence correction signal waveforms (2/2)

6-3. GAIN CONTROL CIRCUIT

Picture distortion and convergence can be adjusted by the remote control unit thanks to employment of the IC DAC8840, which is developed for convergence adjustment. DAC8840 is convenient for use by the features that it can output unipolarity signal input to the circuit either in positive or negative polarity since buffer amplifiers are built in the output circuit, it can receive input signals regardless of the polarity (AC signal is acceptable), all input terminals of the DAC circuits of the eight systems are independent, and so forth.

The internal construction of DAC8840 is shown in Fig. 6-4. The eight DAC circuits (those are regarded as programmable gain controllers rather than D-A converters), DAC-A through DAC-H, are controlled in their gains by the logic block. The clock (CLK) and 8-bit data (DATA) to be input to the logic block are commonly supplied from the 17 DAC8840's used in the convergence circuit, and selection of the DAC's is performed by the chip select LD. LD pulse is obtained by decoding signals S0 to S3 supplied from the control circuit with QJ43. If input signal is regarded as +V, output signal is −V with as the control data is minimum (0) or it is +V as the control data is maximum (FF). Therefore, output voltage can optionally be varied in the range from +V to −V by changing control data.

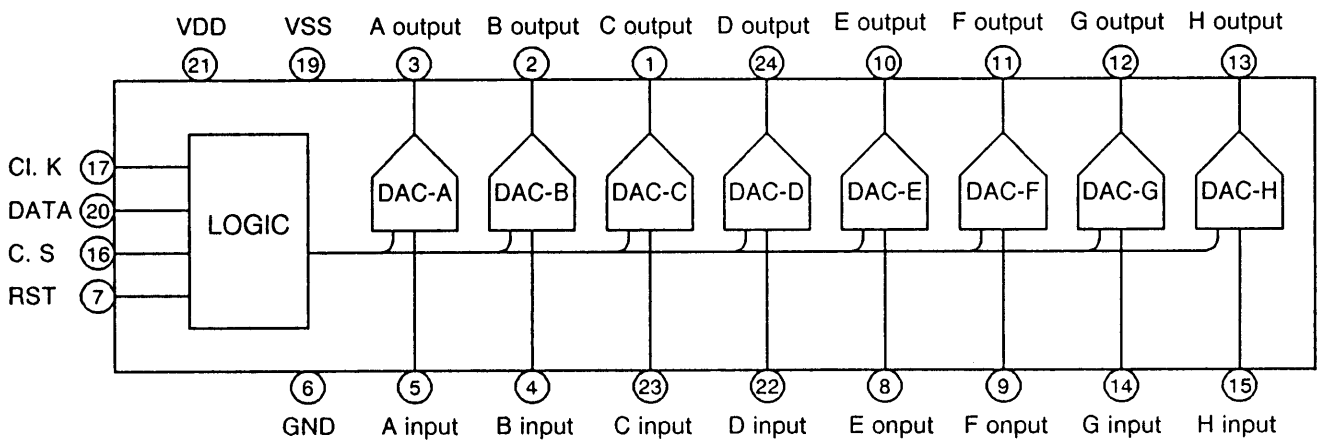


Fig. 6-4 Internal construction of DAC8840

6-4. COMPOSING CIRCUIT

Waveforms whose gains are adjusted by DAC8840 undergo current addition in the operational amplifier (QJ11 to QJ16).

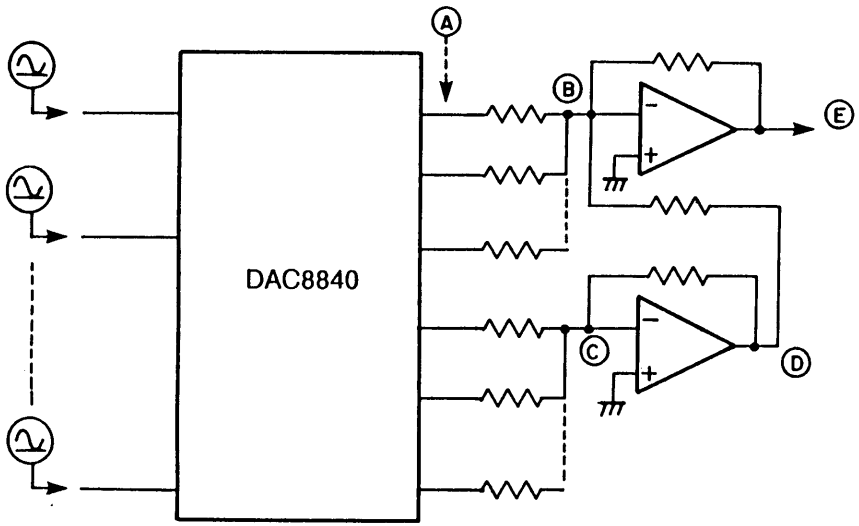


Fig. 6-5 Composing circuit

Refer to Fig. 6-5. When correction waveform is supplied to the input of DAC840, the output terminal A is loaded with voltage. The potential of points B and C of the operational amplifier becomes 0 by imaginary shortcircuit and current is added to them. As a result, mutual interference among correction waveforms is reduced.

The point D has loaded with specified voltage that is inversely output by the operational amplifier. The voltage at the point D is added to the point B in current by imaginary shortcircuit, and then the voltage is output as a composite waveform to the point E. The output gain of each operational amplifier is determined by the ratio of resistances of external resistors.

6-5. CONVERGENCE OUTPUT CIRCUIT

The output block to supply correction current to the convergence coil employs a hybrid IC (STK392-020). Operation of the output circuit is explained in a case of the vertical drive circuit for red signal.

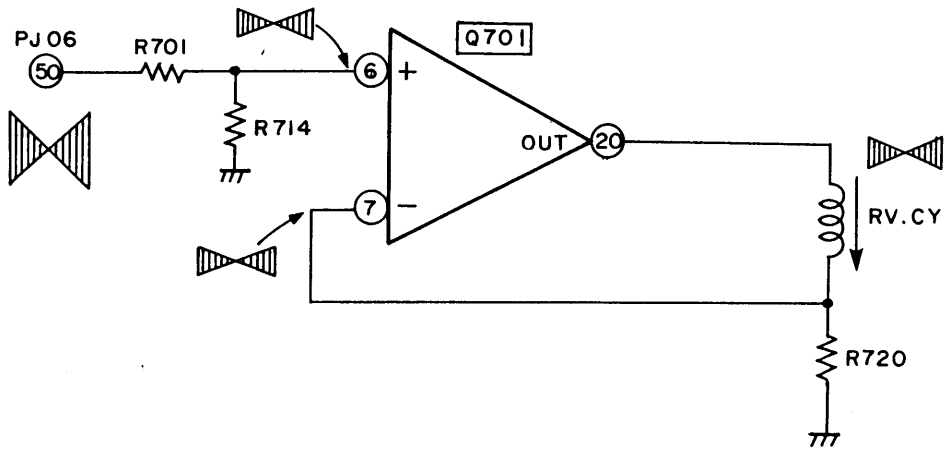


Fig. 6-6 Output circuit

Fig. 6-6 is a simplified illustration of the vertical drive circuit for red signal (RV). The hybrid IC can be regarded as an operational amplifier since its inside is constructed with a differential amplifier at the first stage and the push-pull power amplifier at the last stage.

Vertical convergence correction waveform for red signal is supplied from the CONV. CONT P.C. board to pin 50 of PJ06, and a waveform whose voltage is divided by R701 and R714 is supplied to pin 6 of Q701. On the other hand, voltage generated at the current detection resistor R720 of the convergence coil is fed back to pin 7 of Q701. Therefore, Q701 functions as a current feedback amplifier circuit to equalize voltages at pin 6 and pin 7 of Q701. As a result, a current of the same waveform as the voltage at pin 6 is supplied to the convergence coil (RV, CY).

6-6. PUMP-UP CIRCUIT

To correct vertical keystone distortion (⏢-shaped distortion) and horizontal pincushion distortion (⏥-shaped distortion), it is required to supply a horizontal sawtooth wave current to the convergence coil. When such a current is supplied, voltage at the output terminal of the hybrid IC is of horizontal square wave. For supplying horizontal sawtooth wave current, supply voltage to the hybrid IC needs to be high only in the horizontal blanking period. Therefore, high voltage is supplied it only in the horizontal blanking period, and low voltage is supplied in the scanning period to reduce power consumption of the output circuit. The switching between high and low supply voltages is operated by the pump-up circuit.

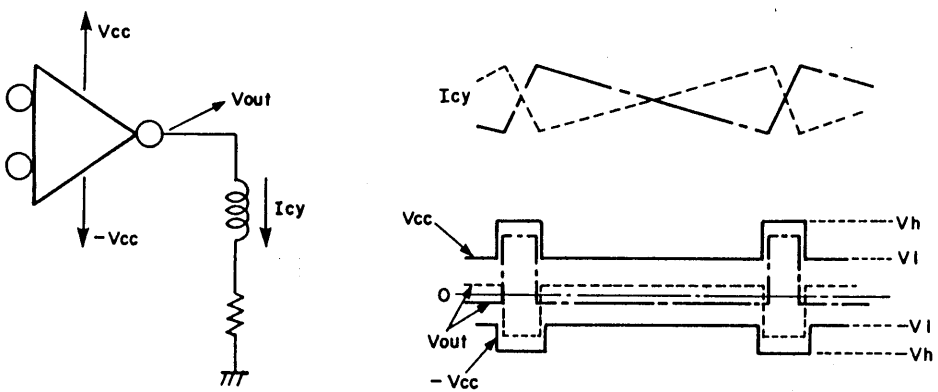


Fig. 6-7

6-6-1. Positive Power Pump-up Circuit

Switching of positive supply voltage is operated output circuits in the five systems of RH, RV, GH, BH and BV.

Fig. 6-8 shows the positive power pump-up circuit. Switching of supply voltage is performed by driving the gates of QH01 and QH02 with the H. BLK pulse.

Horizontal blanking period: In this period, QH02 is on (QH01 is off) and voltage (approx. 7 V) at the both ends of CH10 is accumulated in the +28V power supply. As a result, voltage of 35 V approx. is supplied as Vcc for the convergence circuit. Fig. 6-9 (a) shows a circuit that QH01, QH02, DH01 and DH11 are considered as switches. The current Icc to the convergence output circuit flows in the route of +28 V power supply - QH02 - CH10.

Horizontal scanning period (in the first half): As QH02 is turned off, DH01 is turned on to supply +28 V supply voltage through DH01 to the +Vcc terminal of the convergence output circuit. At the same time, QH01 is turned on and the charge current ICH10 for CH10 flows in the route of +28 V power supply - DH01 - CH10 - LH04 - QH01. (The same amount of charge that is discharged in the horizontal blanking period must be recharged in the scanning period in order to hold the voltage at the both ends of CH10 at 7 V always.) Insertion of a coil LH04 in the flow line of the charge current ICH10 reduces energy loss in QH01. Refer to Fig. 6-9 (b).

Horizontal scanning period (in the second half): As well as the first half of the horizontal scanning period, +28 V supply voltage is supplied through DH01 to the Vcc terminal of the convergence circuit. On the other hand, ICH10 stops charge of CH10 when the voltage at the both ends of CH10 is recharged to 7 V approximately. (Fig. 6-9(c)) The mechanism to stop the charge is as follows. With charge of CH10, DH06's anode potential decreases. When the potential turns down under 2.2 V approx. (voltage at the both ends of CH10 becomes 7 V approx.), QH07 is turned off, QH09 is turned on, QH01's gate potential becomes low, QH01 is turned off, and the charging is accordingly stopped.

When QH01 is off, ICH10 flowing through LH04 enters the +120 V power supply via DH11. As electromagnetic energy ICH10 stored in LH04 has been discharged, DH11 is turned off to recover the condition as shown in Fig. 6-9 (d).

Operation waveforms for each part in the horizontal period are shown in Fig. 6-10.

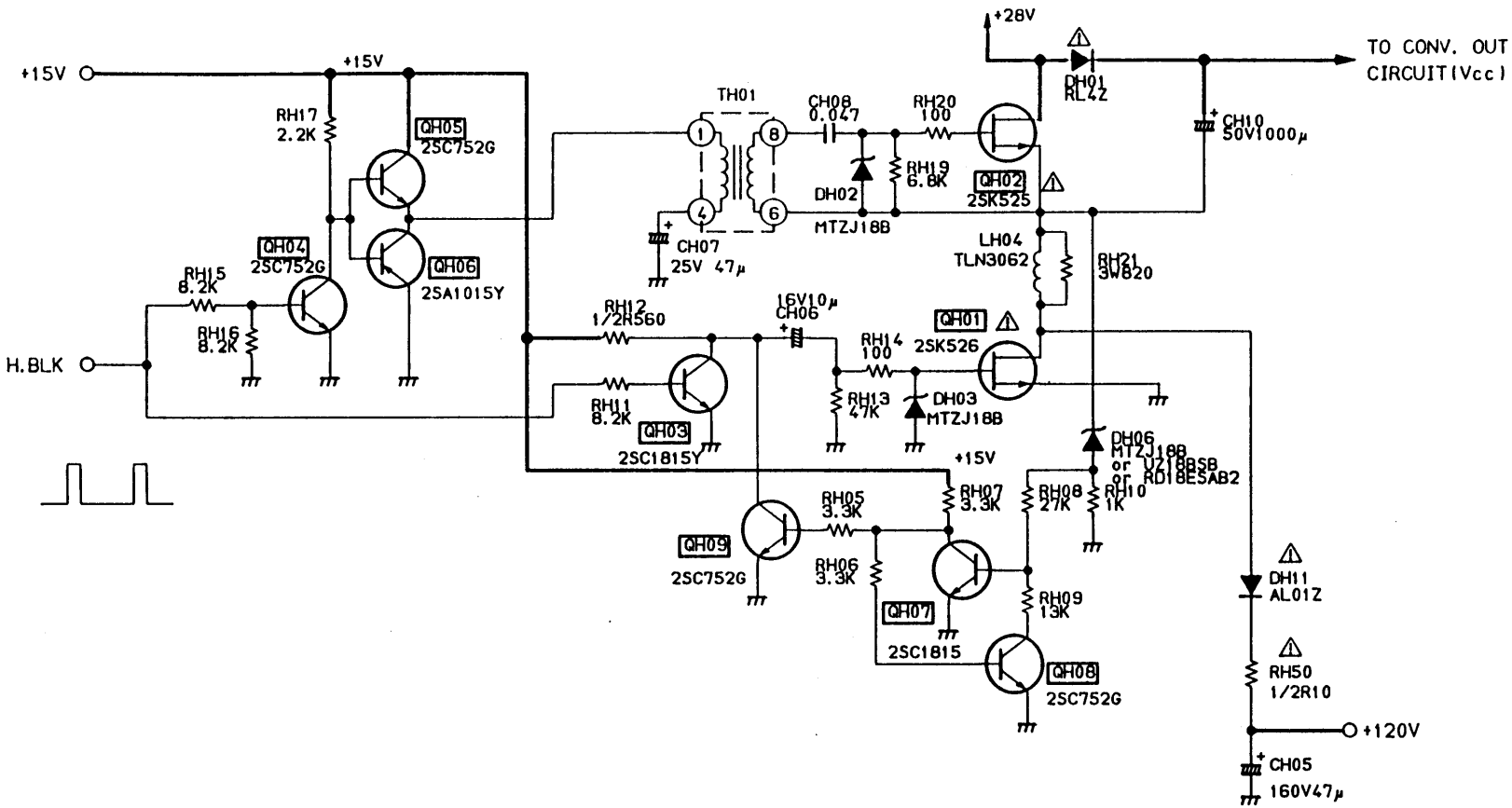


Fig. 6-8 Positive supply voltage pump-up circuit

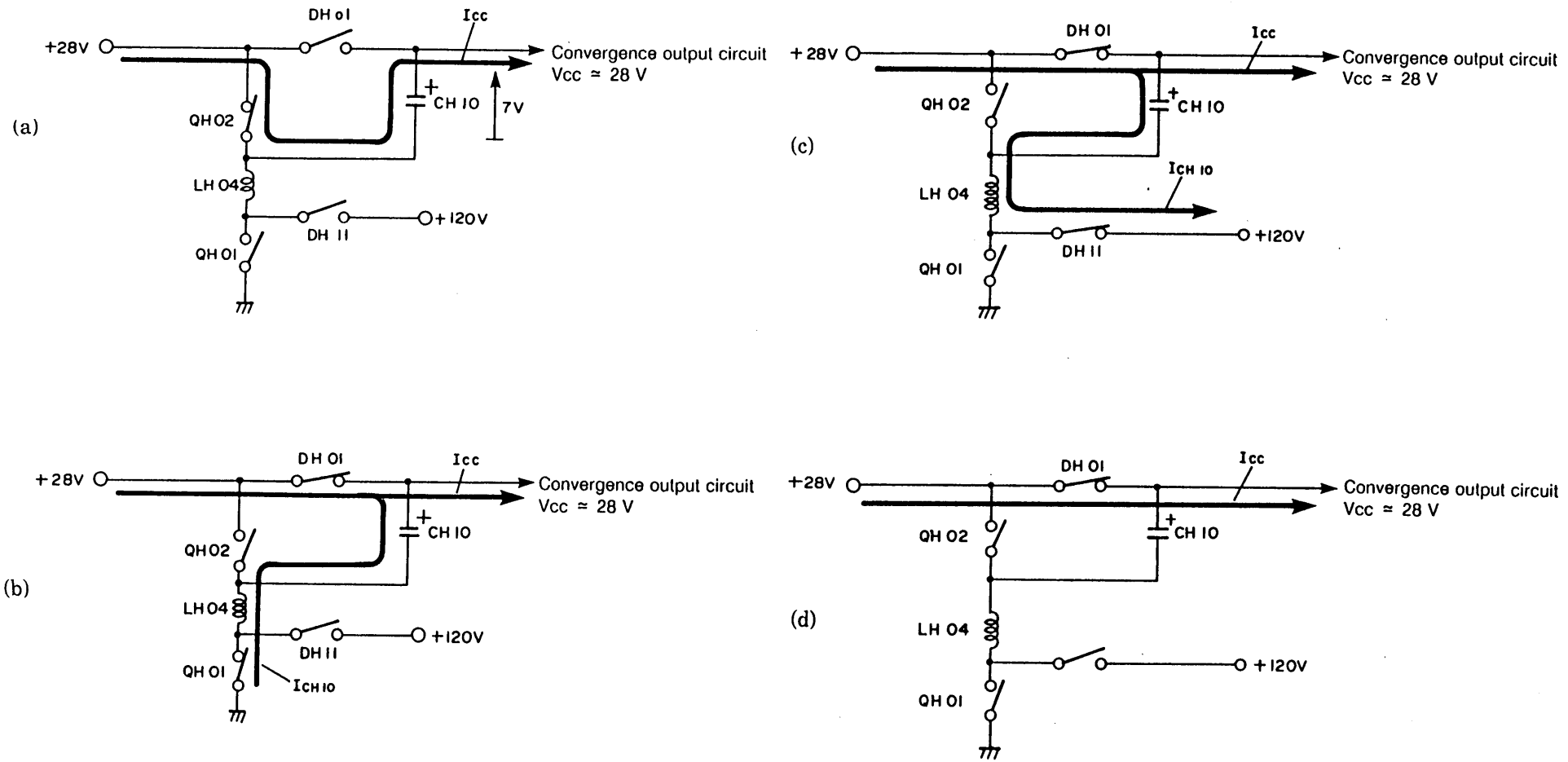

(a)
+28V
DH 01
Icc
Convergence output circuit
Vcc ≈ 28 V
QH 02
CH 10
7V
LH 04
DH 11
+120V
QH 01
(b)
+28V
DH 01
Icc
Convergence output circuit
Vcc ≈ 28 V
QH 02
CH 10
LH 04
DH 11
+120V
QH 01
ICH 10
(c)
+28V
DH 01
Icc
Convergence output circuit
Vcc ≈ 28 V
QH 02
CH 10
ICH 10
LH 04
DH 11
+120V
QH 01
(d)
+28V
DH 01
Icc
Convergence output circuit
Vcc ≈ 28 V
QH 02
CH 10
LH 04
+120V
QH 01

Fig. 6-9

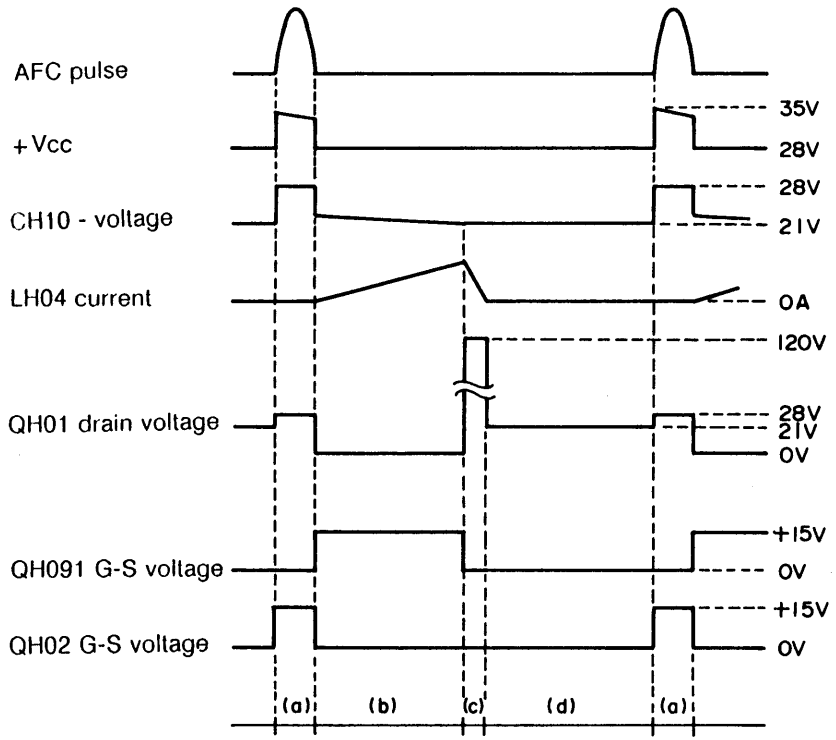


Fig. 6-10

6-6-2. Negative Power Pump-up Circuit

Fig. 6-11 shows the negative supply voltage pump-up circuit.

Switching of negative supply voltage is operated in two systems of RV and BV. In detail, voltage is switched by driving the gates of QH11 and QH12 with the H. BLK pulse.

Horizontal blanking period: In this period, QH11 is on (QH12 is off), voltage at the both ends of CH09 is accumulated in the -28 V power supply. Therefore, voltage of -35 V at the lowest is supplied to the -Vcc terminal. The current of the convergence output circuit flows in the route of -Vcc - CH09 - QH11 - −28 V power supply. (Fig. 6-12 (a))

Horizontal scanning period: In this period, with QH11 being off, DH09 is on to supply -28 V through DH09 to the -Vcc terminal of the convergence output circuit. At the same time, QH12 is turned on, and charge current of CH09 flows in the route of QH12 - RH27 - CH09 - DH09 - −28 V power supply. The parallel connection of CH09 and the zener diode DH08 with each other prevents the charge voltage of CH09 from exceeding 7.5 V. (Fig. 6-12 (b))

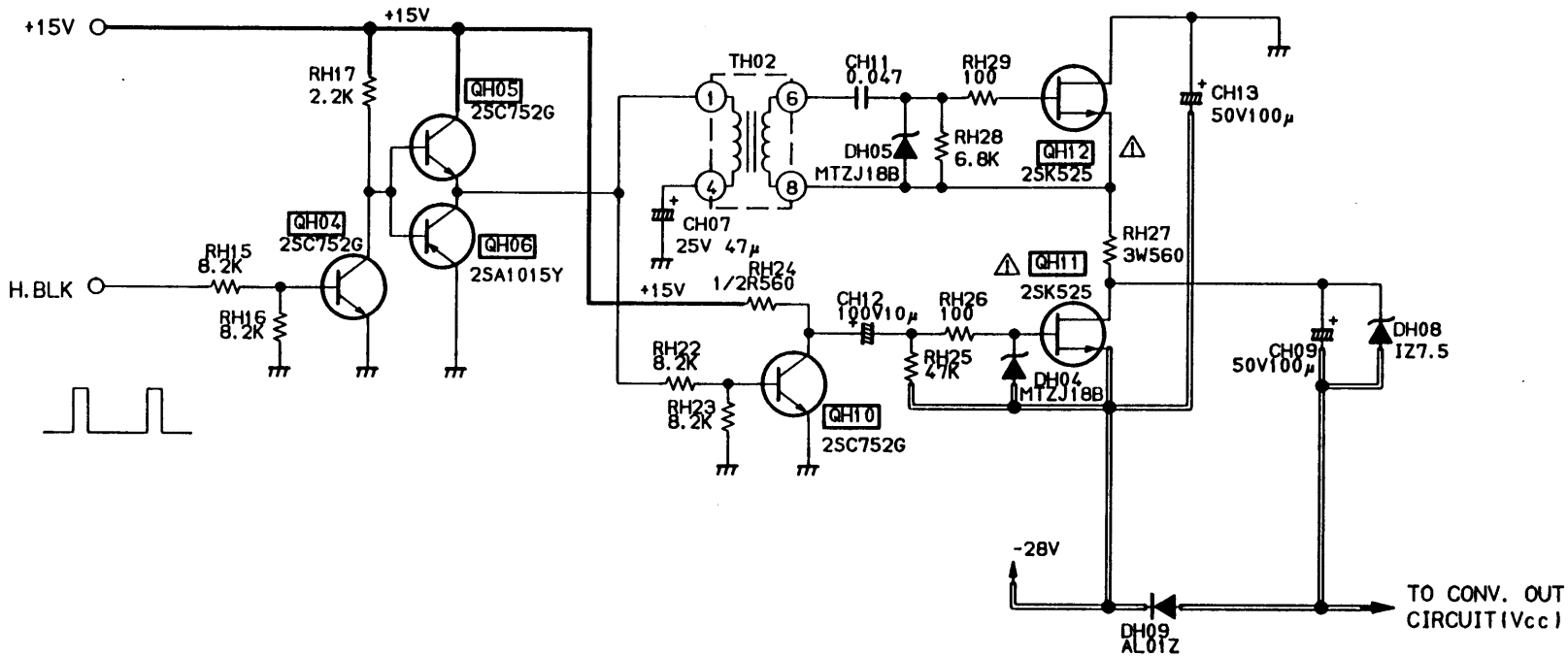
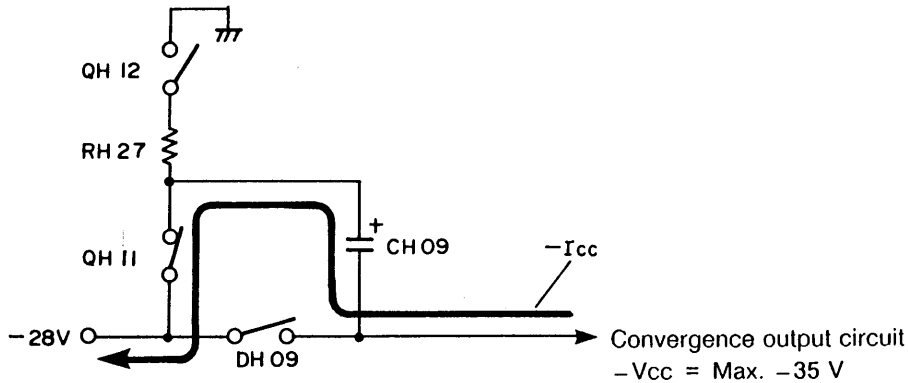


Fig. 6-11 Negative supply voltage pump-up circuit

(a)


QH 12
RH 27
QH 11
+
CH 09
−Icc
−28V
DH 09
Convergence output circuit
−Vcc = Max. −35 V

(b)

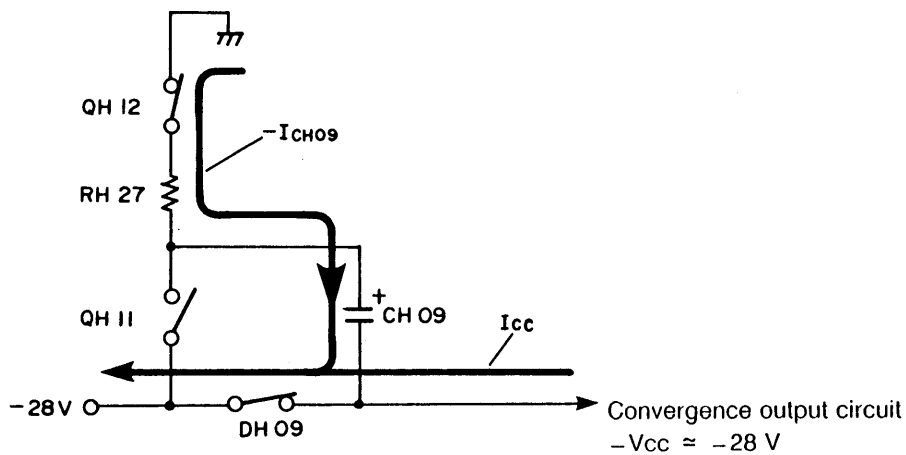

QH 12
−ICH09
RH 27
QH 11
+
CH 09
Icc
−28V
DH 09
Convergence output circuit
−Vcc ≃ −28 V

Fig. 6-12

SECTION 7.

HIGH VOLTAGE CIRCUIT

7-1. OUTLINE

The high voltage circuit provides a high voltage of 31.5 kV to the anode of projection tube. Major difference from that of a conventional TV is the high voltage circuit is separated from the H output circuit and employs a high voltage stabilization circuit.

The high voltage circuit consists of a high voltage generation circuit, high voltage regulation circuit, and a X ray protection circuit. The high voltage circuit accepts the H OSC output pulse as its input and operates with +120V main power supply and +12V power supply.

7-2. HIGH VOLTAGE GENERATION CIRCUIT

An H oscillation pulse is applied to base of Q420 from pin 8 of Q501 (TA8845AN) and Q420 performs a switching operation in H sync period. (Q501 is located on the main P.C. board.)

Q431 base is connected to Q420 collector and Q431 also performs the switching operation in H sync period.

The switching circuit consisting of Q432 and T420 is a high voltage drive circuit and its operation is exactly the same as that of the H drive circuit. In other word, The switching circuit consisting of Q420 and Q431 works as a simple buffer connected between the H oscillation circuit and the high voltage drive circuit. Insertion of the buffer circuit is to prevent cause of screen bending, jitter, etc. due to interference from the high voltage circuit varying its operating condition with the high voltage load current change (varies as picture changes) to the H deflection circuit.

Q433 is a high voltage output transistor and C431, C432, C433 are resonant capacitors. This circuit is the same as that of the H output circuit with the deflection coil removed and the pulse transformer replaced with the FBT. So, the operation theory is also the same exactly.

However, in the H output circuit, its purpose is to provide the sawtooth wave current into the deflection coil, but in the high voltage generation circuit, the purpose is to obtain a pulse voltage which equivalent to the flyback pulse in the H output circuit developed by the resonance of the resonant capacitors and the inductance of FBT primary coil.

The pulse voltage of about 1000 Vp-p obtained at primary side of FBT is stepped up, rectified, filtered, and output as the high voltage of 31.5 kV. The voltage is applied to the anodes of three projection tubes. The filtering capacitor inside the FBT works to reduce high voltage ripples due to dynamic variation of the load current. Moreover, a resistor is also incorporated to detect the high voltage. The detected voltage is fed back to the high voltage stabilization circuit.

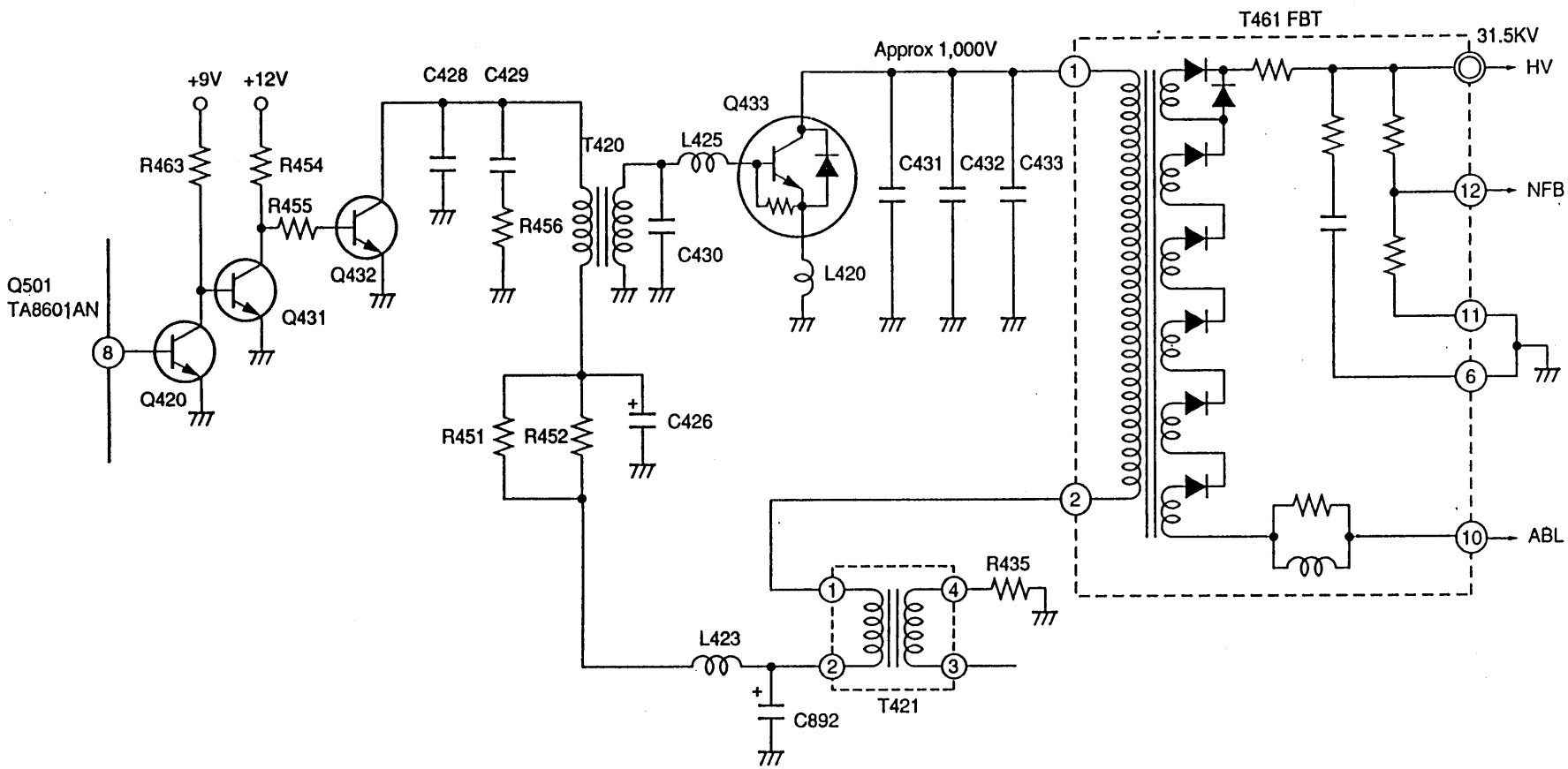


Fig. 7-1 High voltage generation circuit

7-3. HIGH VOLTAGES STABILIZATION CIRCUIT

The TP48C51 employs the high voltage stabilization circuit to prevent high voltage variations due to change of high voltage current and to stabilize screen amplitude (raster size). This allows setting of the high voltage to a value near the maximum rating voltage of the projection tube. As a result the screen brightness can be increased. Moreover, it makes the raster size small. That is, it allows reproduction of more picture information.

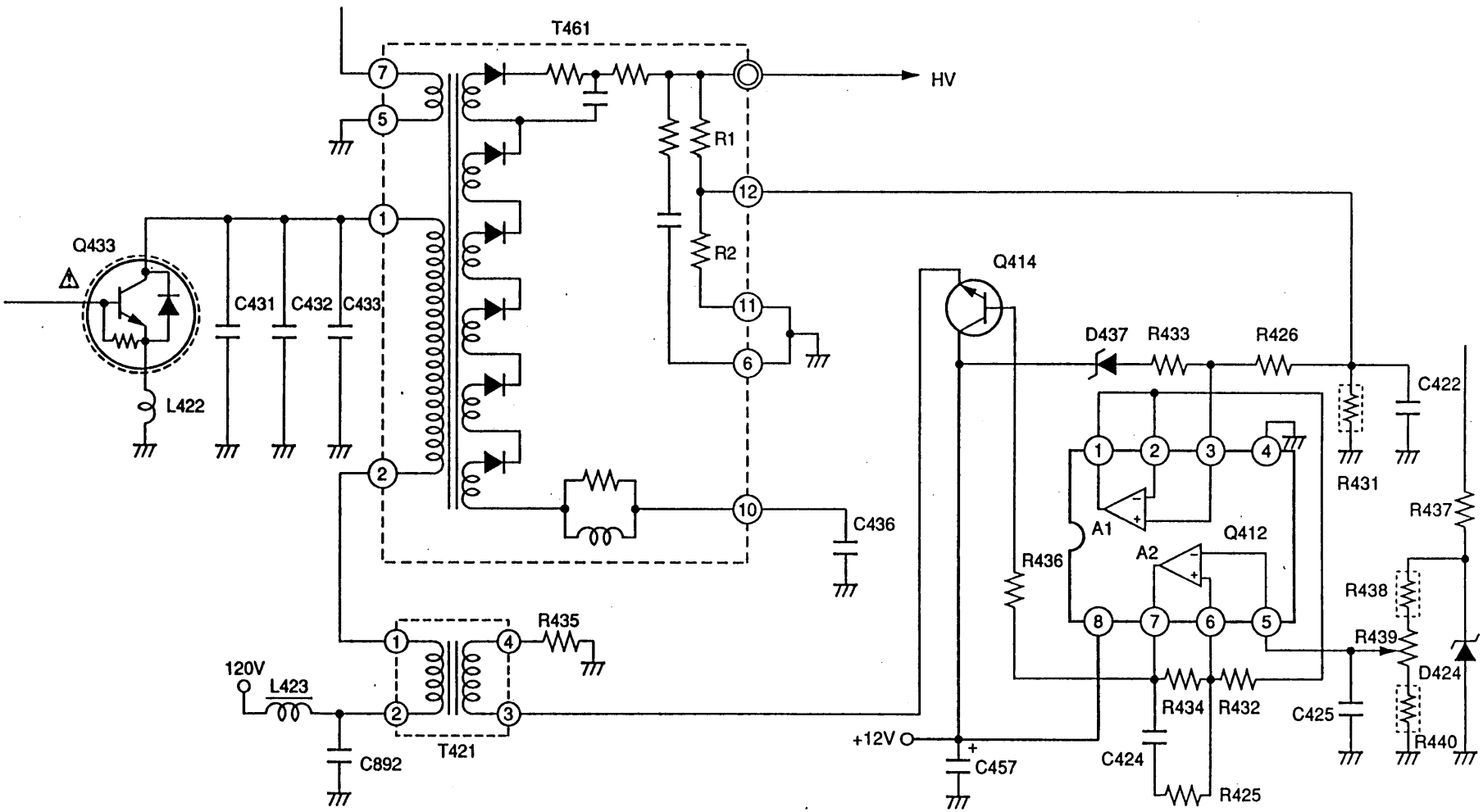


Fig. 7-2 High voltage stabilization circuit

7-3-1. Circuit Operation

The high voltage is obtained by stepping up (n times) the collector pulse (Vcp) generated at the primary side of the flyback transformer and rectifying it. The high voltage E_H will be given by following relation.

$$E_H \propto Vcp$$

That is, the high voltage (E_H) can be stabilized by controlling the Vcp.

(1) The FBT has high voltage detection resistors R_1 and R_2, and a high voltage detection voltage VD is developed across the external resistor of R431. The VD enters pin 3 of Q412 amplifier control IC which contains two op. amplifiers. The pin 3 is a non inverting input terminal of the first stage op. amplifier A_1.

(2) Pin 2 and pin 1 of A_1 are short-circuited and A_1 operates as a buffer amplifier. That is, the detection voltage VD directly appears at the output terminal pin 1 and enters pin 6 of the next op. amplifier A_2.

(3) A reference voltage obtained by dividing the zener voltage developed by D424 with R438, R439 and R440 is being applied to pin 5 of A_2, and the high voltage detection voltage is compared with the reference voltage. The error is amplified and developed at pin 7 of A_2.

(4) The output voltage of A_2 is fed to base of Q414 and controls the collector current of Q414. With the collector current of Q414 varied, a current flowing through a secondary winding of T421 (saturable reactance transformer) varies and this changes inductance value of the primary winding of T421. In practice, when the secondary current increases, the value of L in the primary winding decreases.

(5) When L of the primary winding of T421 connected in series with Lp of the FBT changes, the voltage across Lp of the FTB also changes. So, Vcp changes, thus controlling the high voltage.

(6) For example, actual operations are carried out as follows .

- When the high voltage current I_H increases and the high voltage E_H is going to decrease.

  1) High voltage E_H decreasing
  2) High voltage detection voltage V_D decreasing
  3) A_1 output voltage at pin 1 decreasing
  4) Voltage at pin 6 of A_2 decreasing
  5) A_2 output voltage at pin 7 increasing
  6) Base current of Q414 increasing
  7) Collector current of Q414 increasing
  8) Secondary current of T421 increasing
  9) Primary current of T421 decreasing
  10) Voltage across Lp of FBT increasing
  11) Vcp increasing
  12) High voltage E_H increasing

- When the high voltage current I_H decreases and the high voltage E_H is going to increase, the variations for all the operations occur in reverse direction.

In this way, with the correction loops shown above, the high voltage is stabilized if the high voltage current I_H varies.

R439 is a high voltage adjustment control and adjusts the high voltage to 31.5 kV.

D437 is a zener diode to control the lower limit of the high voltage detection voltage and prevents a latch up for the op. amplifiers due to high voltage spark, etc.

7-4. X RAY PROTECTION CIRCUIT

Generally speaking, when high speed electrons collide with an object, a X ray will be emitted. In the projection tubes using the high voltage, if the high voltage increases excessively due to failure of the high voltage circuit or abnormal operation, the emission of X ray will increase and gives undesirable affection on human body. To prevent this, a X ray protection circuit is provided with TP48C51.

In a general TV receiver, if the high voltage shows an excessive increase, followings may consider as failure modes.

As previously stated above, operation theory of the H output circuit and the high voltage output circuit is the same and the collector pulse voltage of the output transistor is obtained by using a resonant phenomenon due to the resonant capacitor C and the inductance L.

When assuming the pulse width (a half of the resonant period equivalent to H flyback period) as tr, a time corresponding to H scanning period ts, and the power supply voltage fed to the output circuit as Vcc, the peak value of the pulse voltage is given by following equation.

$$Peak\ value\ Vp = Vcc \times (1+\frac{\pi \times ts}{2 \times tr})$$

As can be seen from the above equation, the Vp increases when

(1) Vcc is high

(2) tr is short

(3) ts is long

The tr is determined by a resonance of L and C, and tr is obtained as

$$tr = \pi \times \sqrt{(L \times C)}$$

That is, tr becomes short when C or L lowers. Accordingly, in a conventional TV, when the Vcc increases due to (1) abnormal operation of the power circuit, (2) lower capacitance of the resonant capacitor, or lower inductance due to broken core of FBT, and (3) ts increased with H frequency drop, the high voltage increases to a higher value than the normal value.

On the other hand, in the TP48C51, a variation of the high voltage is detected with a pulse voltage Vx (Vx ≒ Vcp x Nx/Np) stepped down with a winding ratio of Nx/Np, here Np is a primary winding of the FBT. The Vx is rectified with D471 and C451, and the Vx of about 21V is obtained. If the high voltage increases excessively due to some reasons, the Vcp increases, Vx increases, and Va increases. With the Va increased, a voltage divided by R487, R488//R461 or emitter voltage of Q451 increases. Since, the base voltage of Q451 is fixed at a zener voltage of 6.2V, Q451 turns on when the emitter voltage of Q451 becomes 6.2V + V_{BE}. Then, Q452 turns on.

With Q452 turned on, the thyristor D862 turns on in passing through D473 R495, R808. Then Q863 turns on, and Q807, Q806 turn off. That is, the power relay SR81 is opened and the main power supply of the set is turned off.

The operation voltage of the X ray protection circuit is set to a higher value so that the protection circuit does not operate under the normal operation.

When the unit is completed, operation check for the X ray protection circuit is carried out by short-circuiting the test points Ⓡ and Ⓧ. When the Ⓡ and Ⓧ are short-circuited, R487 and R486 are connected in parallel. This rises Q451 emitter voltage and makes Q451 turn on, thus allowing the check for operation of the X ray protection circuit.

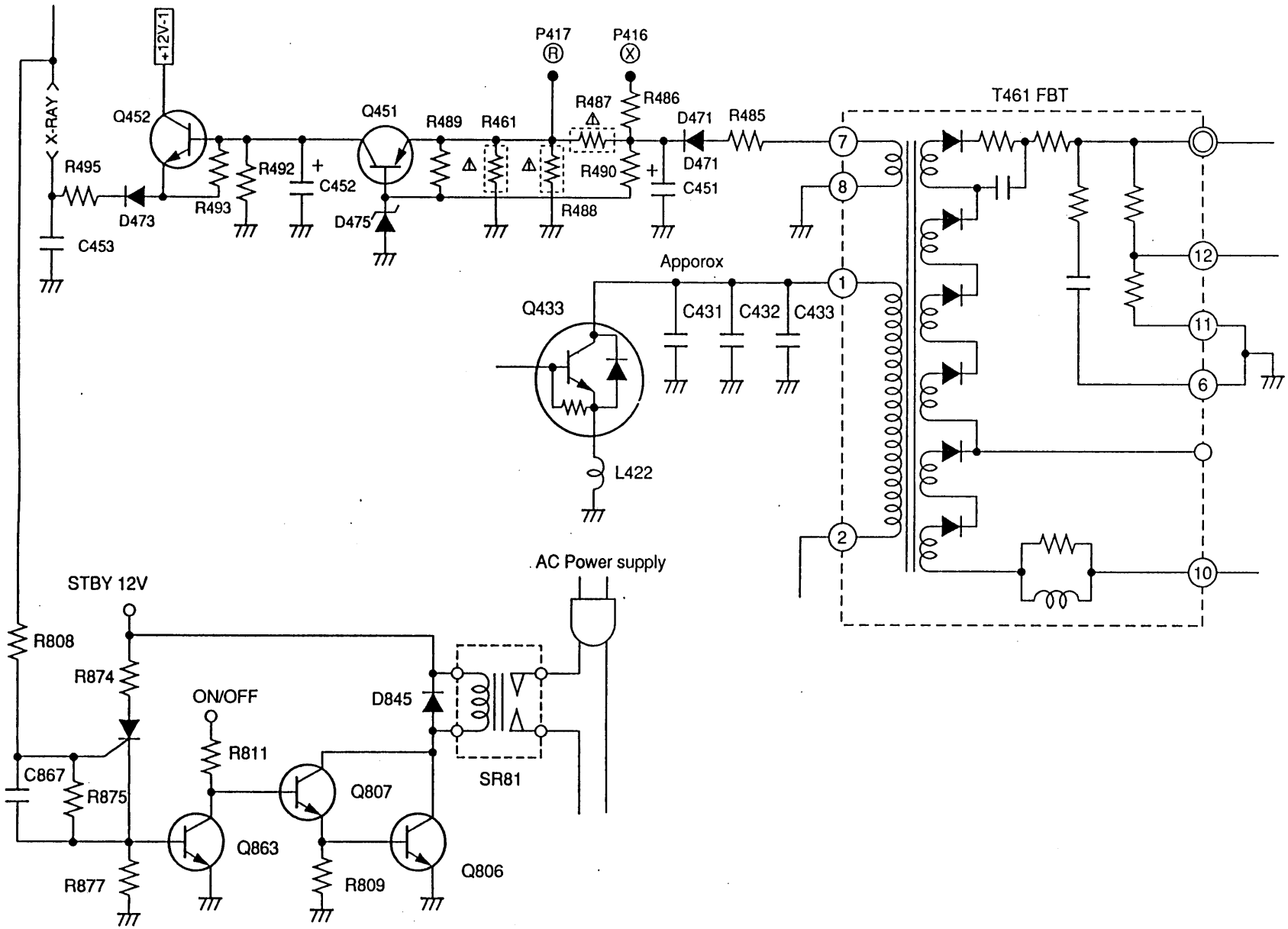

+12V-1
X-RAY
Q452
Q451
P417
P416
R487
R486
R489
R461
D471
R485
T461 FBT
R495
R492
C452
R490
C451
R493
D473
D475
R488
C453
Apporox
Q433
C431
C432
C433
L422
AC Power supply
STBY 12V
R808
R874
ON/OFF
D845
R811
C867
R875
Q807
SR81
Q863
Q806
R877
R809

Fig. 7-3

SECTION 8.
DYNAMIC FOCUS CIRCUIT

8-1. OUTLINE

In TP48C51, a static focus system is employed in the projection tube. Degradation of the focus quality at peripheral screen is improved by applying focus correction voltages (parabola voltages in H/V periods). The dynamic focus circuit creates this focus correction voltage and consists of an H and a V dynamic focus circuit.

To obtain a flat focus characteristics at center and peripheral of the screen, the focus correction is carried out by applying the H sync parabola correction voltage (efH = 700 Vp-p) and the V sync parabola correction voltage (eifv = 300 Vp-p) to the focus electrode in addition to the focus DC voltage of Ef (= EH x 0.27 ~ 0.29).

8-2. H DYNAMIC FOCUS CIRCUIT

8-2-1. Theory of Operation

Fig. 8-1 shows a block diagram of the circuit which develops an H parabola correction voltage.

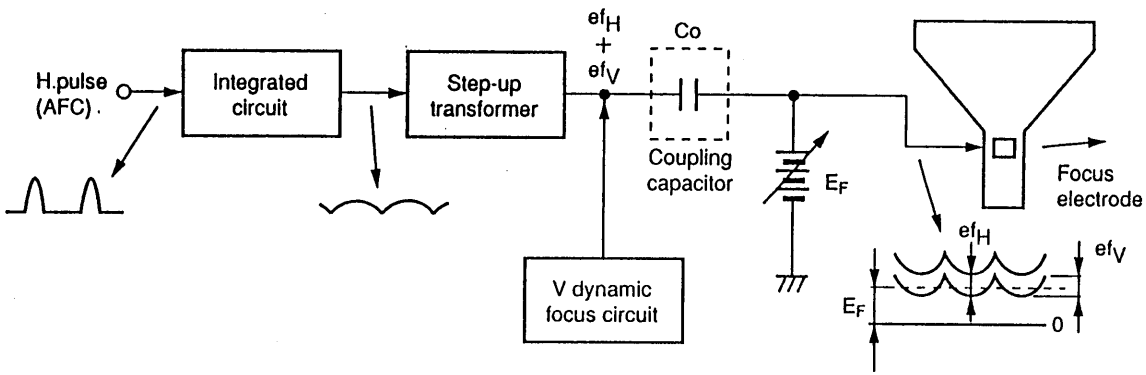


Fig. 8-1 Block diagram of H dynamic focus circuit

8-2-2. Circuit Operation

The H pulse developed at pin 14 of the pulse transformer T462 enters the integration circuit consisting of L470 and C_1. The C_1 does not exist in the actual circuit as shown in a dotted line. The C_1 is an equivalent capacitance of the stray capacitance of Cs in secondary side of the step-up transformer T405 converted into the primary side and can be expressed as:

$$C_1 = n^2 C_s$$

The H pulse is integrated with L470 and C_1, and a sawtooth wave current of I_{C1} flows into C_1.

Accordingly, a parabola voltage V_1 integrated is developed across C_1 and this is used as the input voltage (primary side voltage) for the step-up transformer. A parabola voltage V_2 stepped-up and inverted is obtained at secondary side (F, P terminals) of T470. This parabola voltage is mixed with the V parabola voltage described under the V dynamic focus circuit, and the mixed voltage is superimposed with the focus DC voltage (about 9 kV) through a coupling capacitor Co, and supplied to the focus electrodes of three R, G, B tubes.

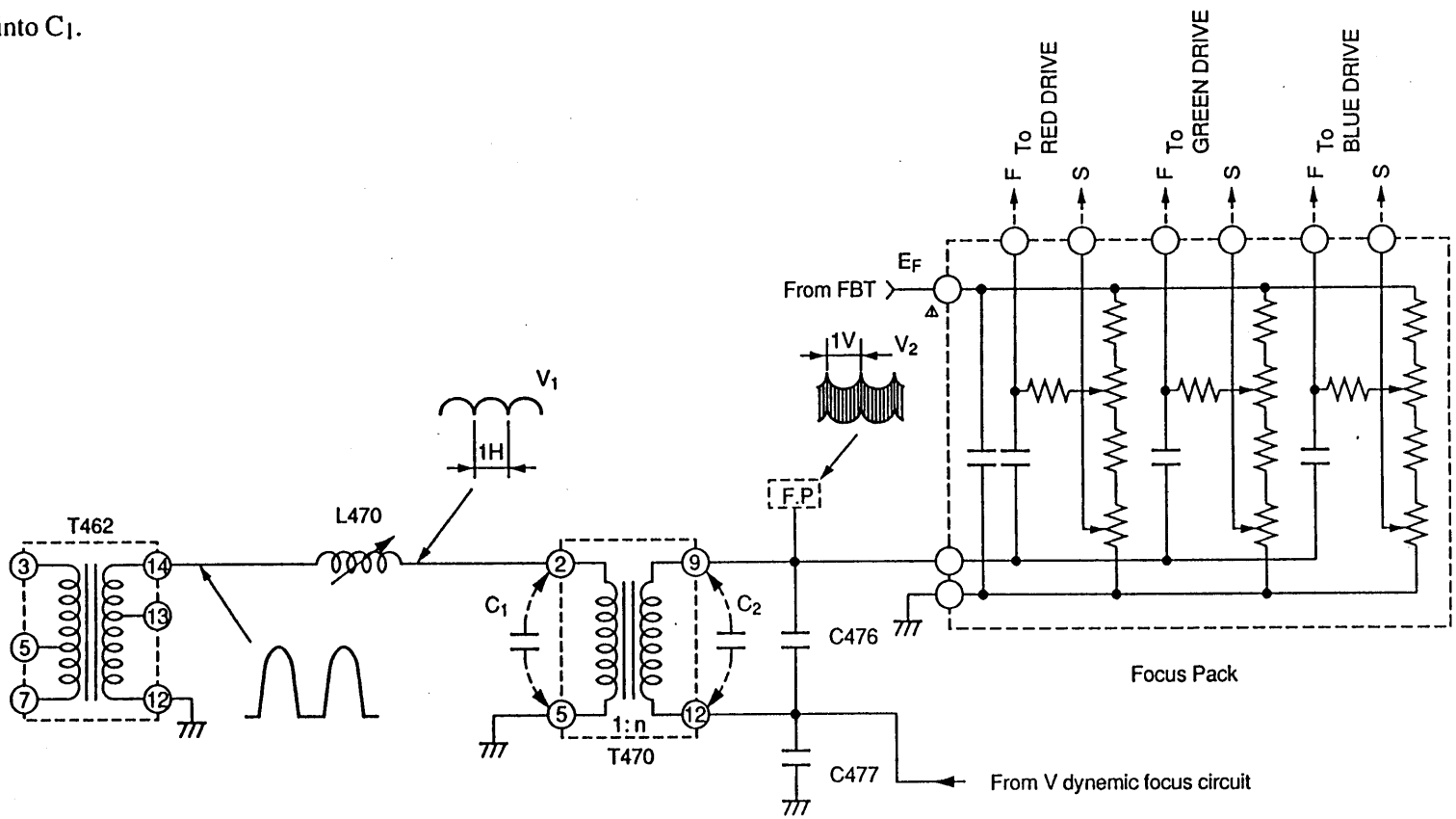


Fig. 8-2

8-3. V DYNAMIC FOCUS CIRCUIT

8-3-1. Theory of Operation

Fig. 8-3 shows the circuit which develops the V parabola correction voltage.

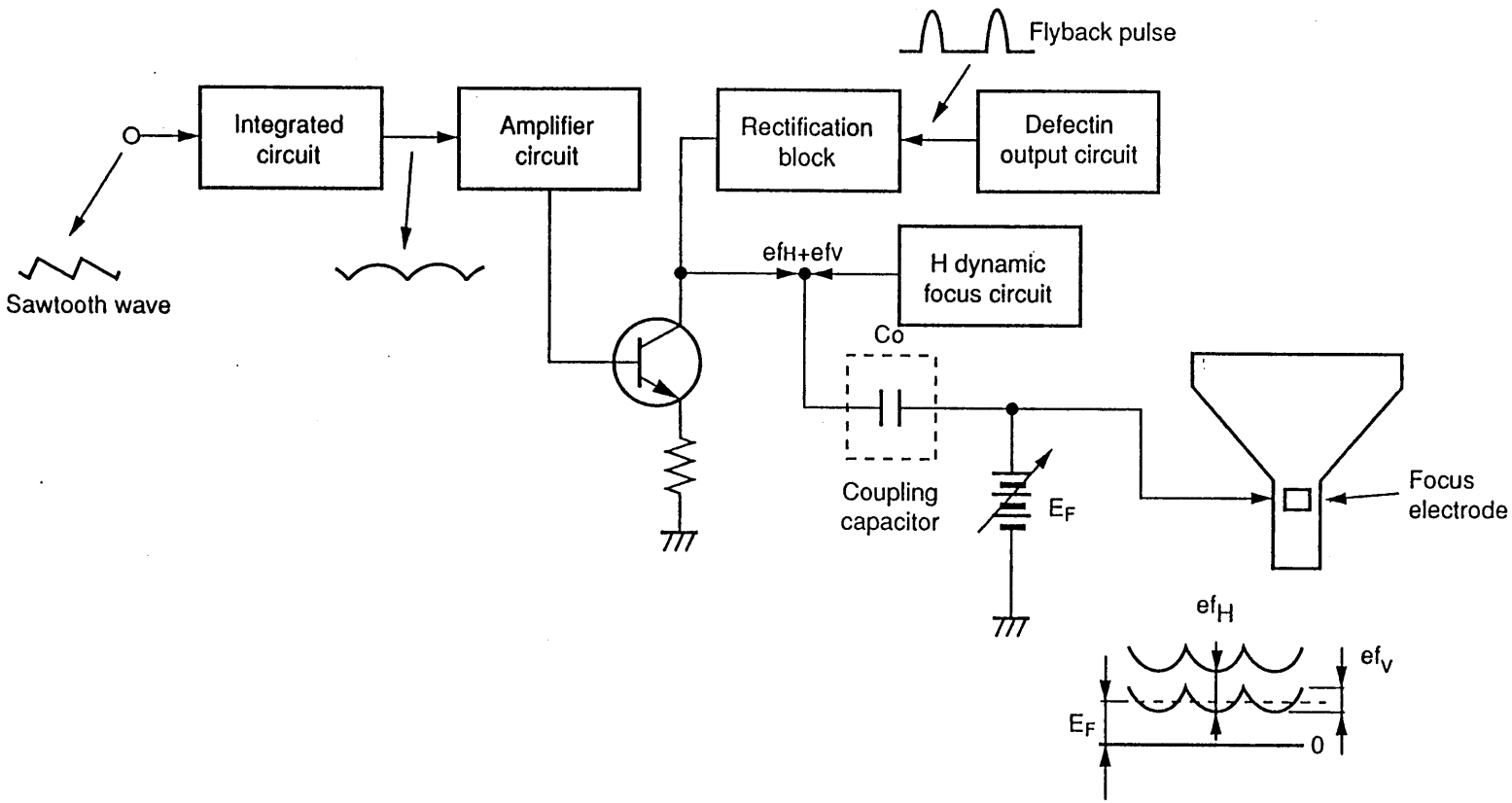


Fig. 8-3 Block diagram of V dynamic focus circuit

8-3-2. Circuit Operation

A sawtooth wave voltage developed across (R301+R302) in the V output circuit is cut in its DC component and the AC components of the voltage is integrated into a parabola form by a mirror integrator in the first stage and amplified with a specified gain level set by R471/R470. The amplified parabola wave enters an op. amplifier in the next stage and again amplified. The op. amplifier works as an inverting amplifier and the gain is determined by (R478/R475)/R477. The parabola voltage amplified in this way enters base of Q471, amplified in an inverted form, and developed as the V focus parabola voltage (300 Vp-p, DC component 60V). This voltage is mixed with the H focus parabola voltage in passing through R483, resulting in a mixed parabola voltage consisting of a H component of 700 Vp-p and a V component of 300 Vp-p. Thus obtained mixed output is fed to the focus electrodes of R, G, B projection tubes through the coupling capacitor stated under 2-2.

The parabola level of the V focus parabola output voltage can be adjusted by varying R475 and the DC voltage level by varying R482.

The power for Q471 is obtained by rectifying collector pulse of the deflection output circuit with the rectification circuit Z470. The rectification circuit Z470 is assembled as a separate block in considering safety because of its high rectified output voltage of about 1000V.

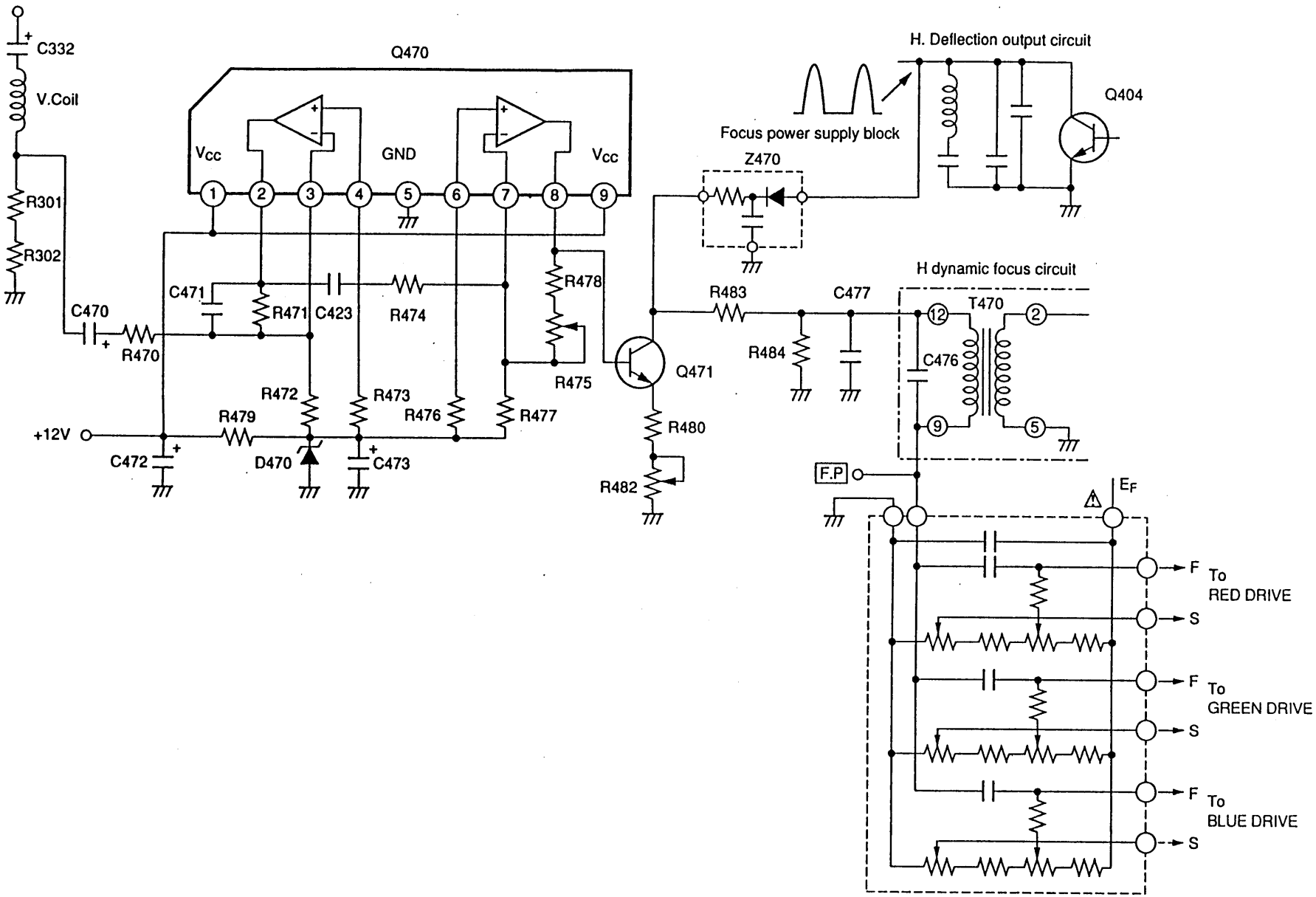


Fig. 8-4 V output circuit

SECTION 9.
POWER SUPPLY CIRCUIT

9-1. OUTLINE

The power supply circuit of the P4100 series video wall projection unit comprises of the three power supply circuit systems of the following.

(1) Standby power supply circuit

(2) Main power supply circuit

(3) Sub power supply circuit

A block diagram of the power supply circuit of the P4100 series unit (P4100U, P4100J) is shown in Fig. 9-1-1.

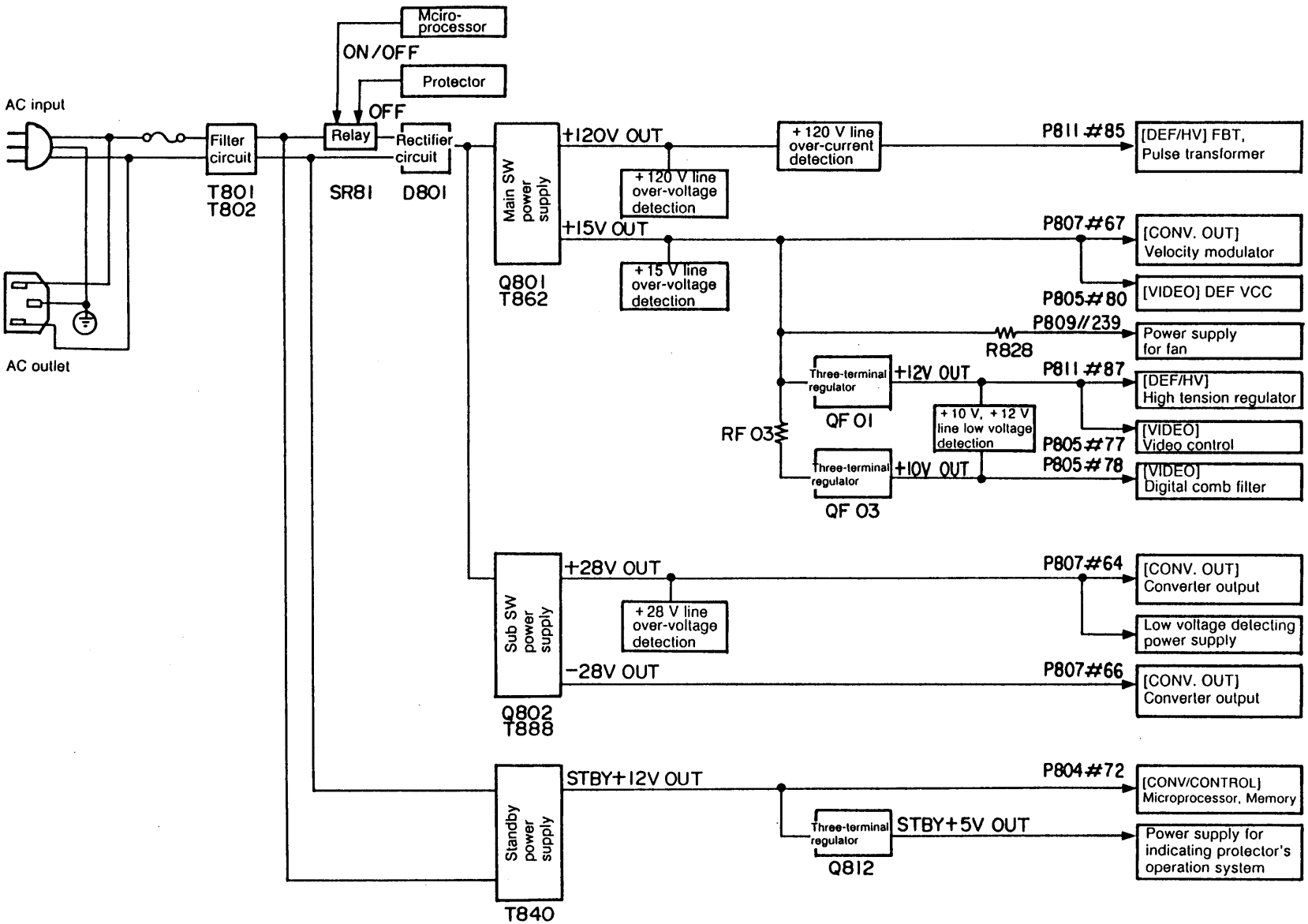


Fig. 9-1-1 P4100 series power supply circuit block diagram

9-2. RECTIFIER CIRCUIT (Fig. 9-1-2)

Commercial supply voltage input through the power cord plug is supplied to the AC input terminal of the bridge rectifier diode D801 through the two line filters (T801, T802) provided to suppress unnecessary radiation and the power relay switch SR81.

D801 which incorporates four bridge-connected diodes inside outputs rectified ripple voltage from the output terminal. This rectified ripple voltage is smoothed by the smoothing capacitor C810 and then supplied as DC voltage to the main power supply circuit and the sub power supply circuit.

R810 and R812 are resistors to limit rush current at the time of power on.

The relay switch SR81 is activated with ON/OFF signal from the remote controlled microprocessor to turn on/off the main and sub power supply circuits. Moreover, this relay switch turns off the power supply circuits when over-voltage is output owing to malfunction of the power supply circuit and protectors for the X-ray protection circuit, etc. are activated.

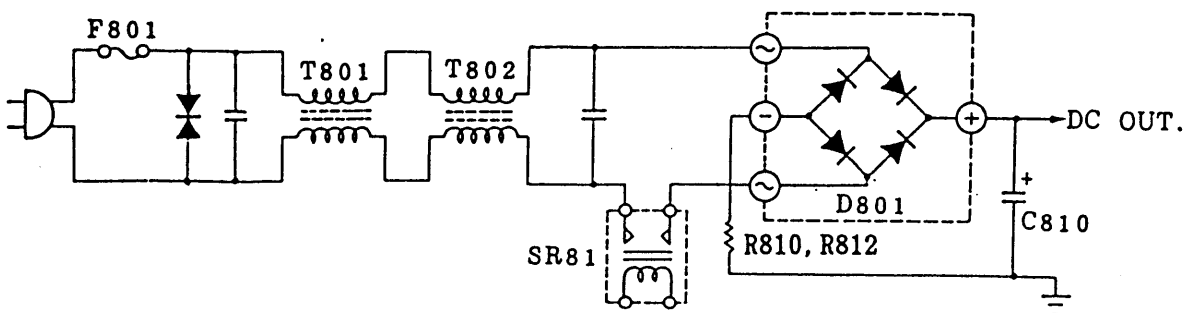


Fig. 9-1-2

9-3. STANDBY POWER SUPPLY CIRCUIT

(Fig. 9-1-3)

The power transformer T840 turns down commercial AC supply voltage, and four diodes of D840, D841, D842 and D843 rectifies full waves to yield DC voltage. The resultant voltage is +12 V, which is used to drive the power relay switch SR81. This voltage is transformed to +5 V regulated power supply by the regulator ICs (Q812, QA41) of the POWER and CONVER/CONTROL P.C. boards to be supplied to the protector's operation system indication circuit, microprocessor and its peripheral components.

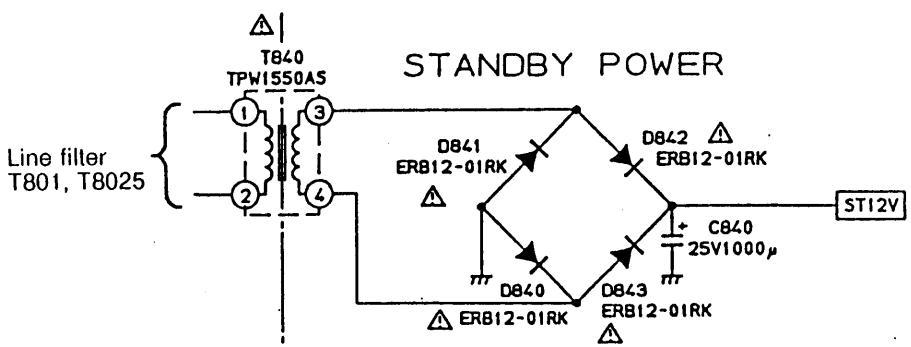


Fig. 9-1-3

9-4. MAIN POWER SUPPLY CIRCUIT

(Fig. 9-1-4)

The main power supply circuit supplies supply voltage mainly to the horizontal output circuit and the high tension output circuit. The system is a self-excited ringing choke type converter, in other words, secondary winding is applied to around the oscillation transformer of the blocking oscillation circuit, and the resultant pulse voltage is rectified to be supplied to the load. This circuit employs a hybrid IC (Q801: STR-M6515) in which the switching transistor and the control circuit are unified. The circuit operation will be explained later in the subsection 9-6-1.

Output voltages of this circuit are +120 V and +15 V, and the latter is fine divided into +10 V and +12 V to be supplied to the digital comb filters and the high tension regulation circuit, etc. Besides the above-mentioned voltages, 220 V, 12 V, etc. are generated by the pulse transformer to be supplied to the CRT drive, high tension drive, vertical sawtooth wave generator circuits, moreover, the regulator IC yields 5 V from +12 V to supply it as the supply voltage for the converter control.

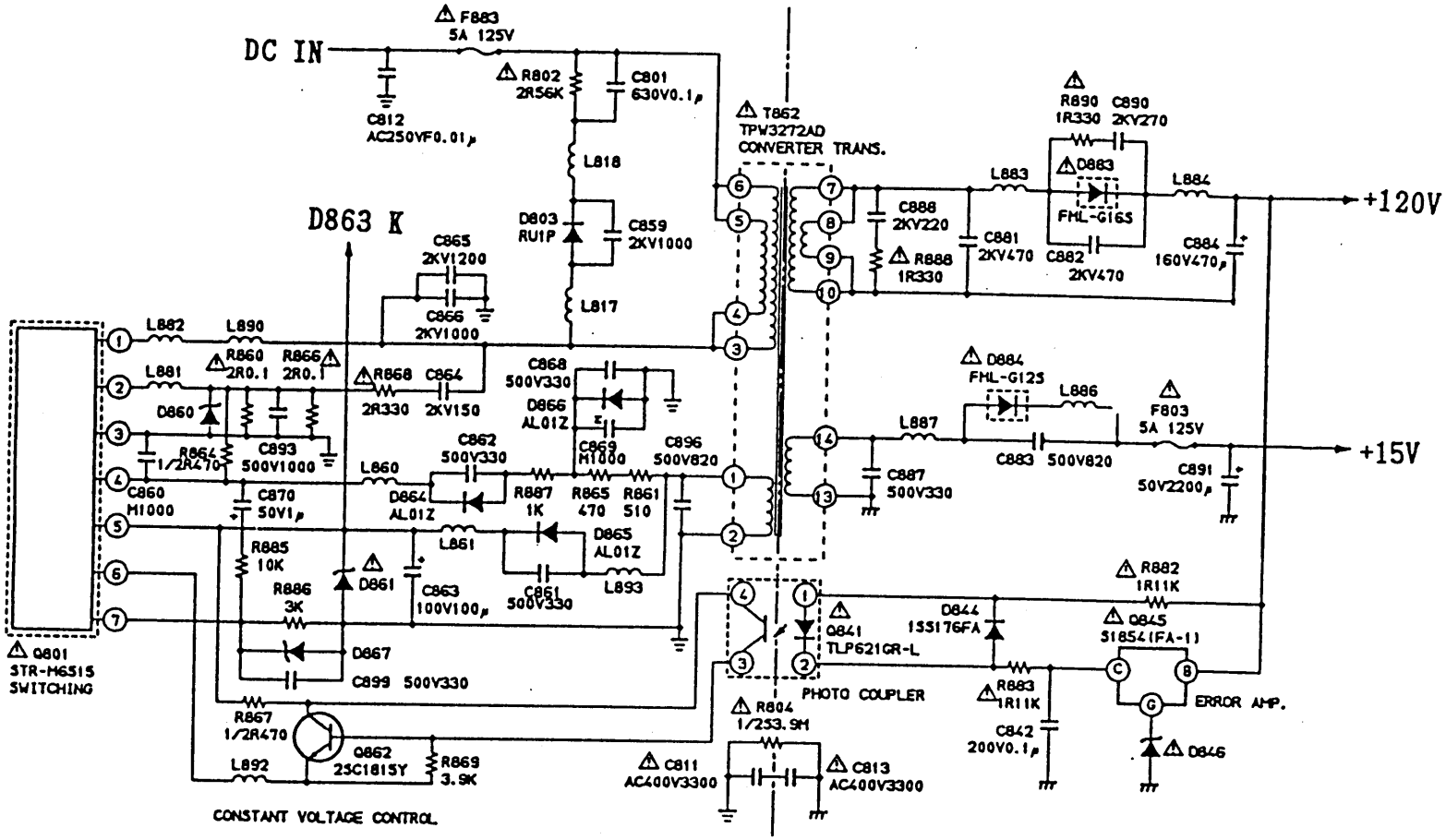

DC IN
F883
5A 125V
C812
AC250VF0.01μ
R802
2R56K
C801
630V0.1μ
L818
D803
RU1P
C859
2KV1000
L817
D863 K
C865
2KV1200
C866
2KV1000
T862
TPW3272AD
CONVERTER TRANS.
R890
1R330
C890
2KV270
D883
FHL-G16S
L883
L884
+120V
C888
2KV220
R888
1R330
C881
2KV470
C882
2KV470
C884
160V470μ
L882
L890
L881
R860
2R0.1
R866
2R0.1
R868
2R330
C864
2KV150
D860
R864
1/2R470
C893
500V1000
C860
M1000
C870
50V1μ
C868
500V330
D866
AL01Z
C862
500V330
C869
M1000
C896
500V820
L860
D864
AL01Z
R887
1K
R865
470
R861
510
D865
AL01Z
L861
L893
C861
500V330
D884
FHL-G12S
L886
F803
5A 125V
L887
C883
500V820
C891
50V2200μ
+15V
C887
500V330
R885
10K
R886
3K
D861
C863
100V100μ
D867
C899 500V330
R882
1R11K
Q841
TLP621GR-L
D844
1SS176FA
Q845
S1854(FA-1)
PHOTO COUPLER
R883
1R11K
C842
200V0.1μ
ERROR AMP.
D846
R804
1/253.9M
C811
AC400V3300
C813
AC400V3300
Q801
STR-M6515
SWITCHING
R867
1/2R470
Q862
2SC1815Y
R869
3.9K
L892
CONSTANT VOLTAGE CONTROL

Fig. 9-1-4

9-5. SUB POWER SUPPLY CIRCUIT

(Fig. 9-5-1)

The sub power supply circuit is a switching regulator circuit to output 28 V supply voltage for the convergence output circuit. This circuit also employs the hybrid IC (Q802: STR-M6515) which internally unifies the switching transistor and the control circuit. The circuit construction and the circuit operation are the same as those of the main power supply circuit.

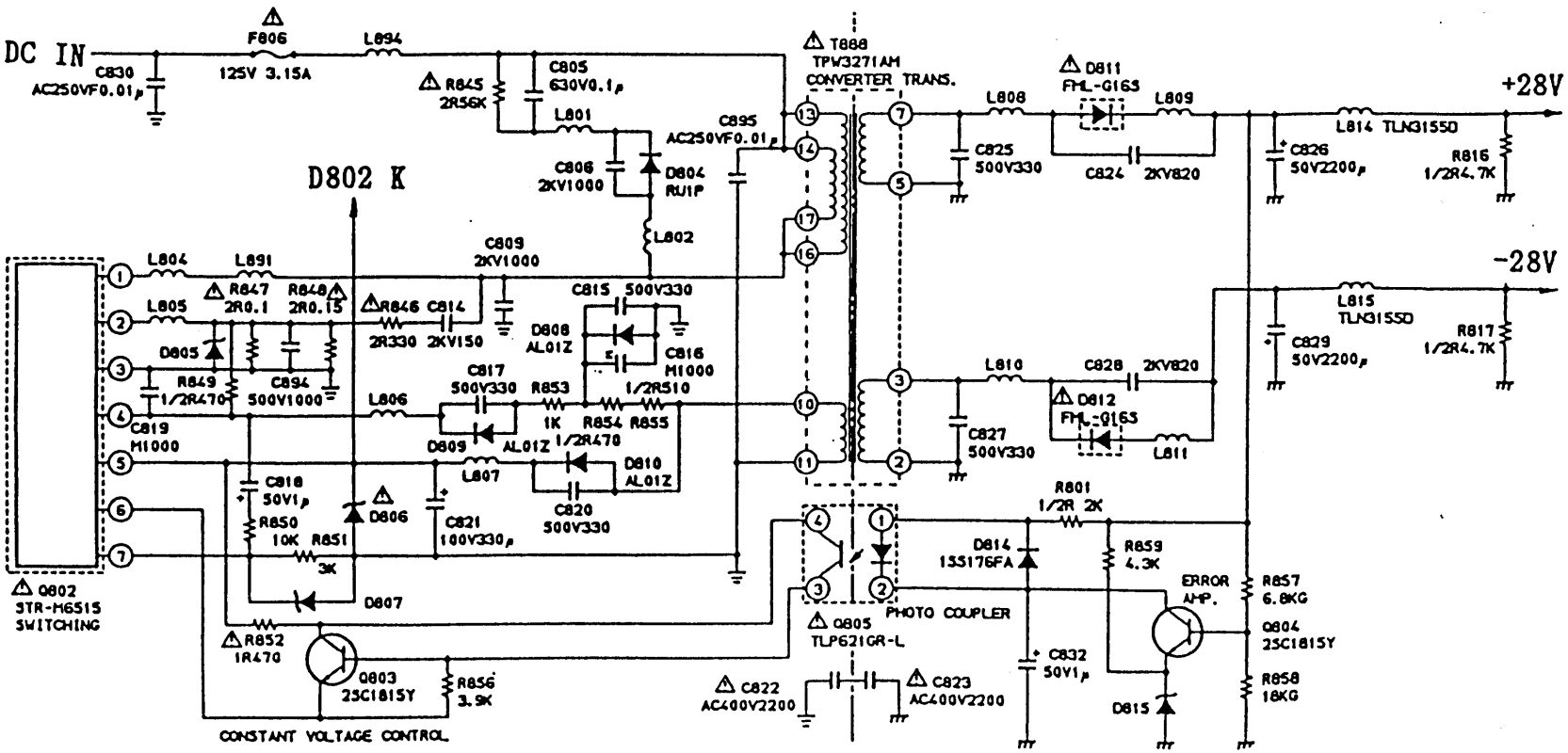


Fig. 9-5-1

9-6. OPERATION OF VOLTAGE CONTROL IC Q801 (STR-M6515)

STR-M6515 Block Diagram and Pin Functions

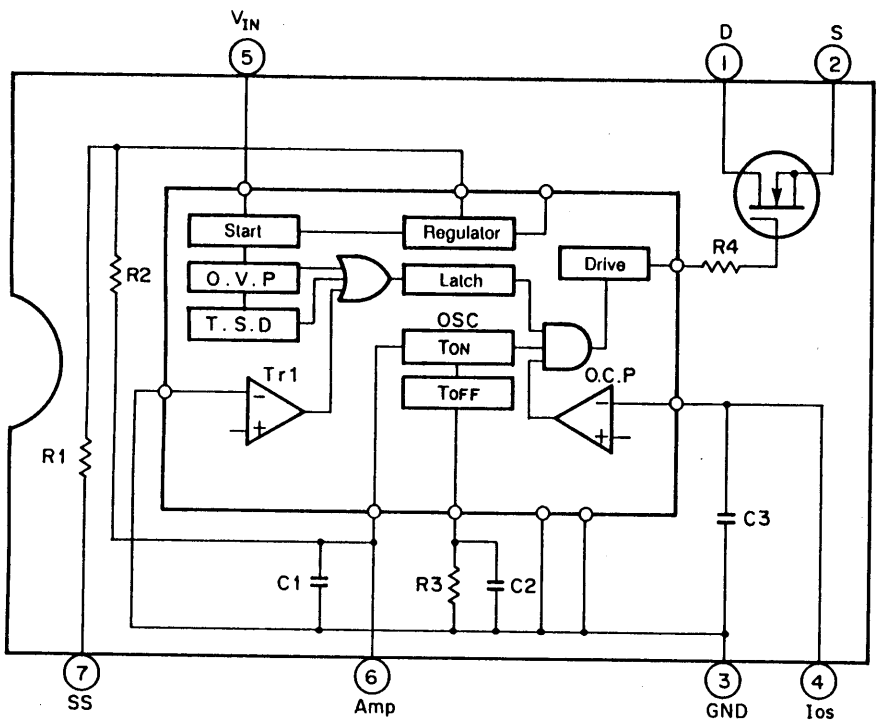


Fig. 9-2-1 STR-M6515 block diagram

Table 9-2-1 STR-M6515 pin functions

Pin No.	Symbol	Name	Function
1	D	DRAIN	MOS FET drain
2	S	SOURCE	MOS FET source
3	GND	GROUND	Ground
4	I_{OS}	OVER-CURRENT	Over-current detection signal input
5	V_{IN}	POWER	Control circuit power input
6	Amp	FEED-BACK	Constant voltage control signal input
7	SS	SOFT START	Soft starting voltage output

9-6-1. Operation of STR-M6515 Terminals and Its Peripheral Circuits

1) V_{IN} terminal (pin 5), Starter circuit

The starter circuit functions to start and stop the operation of the control IC with detection of voltage at the V_{IN} terminal (pin 5). The circuit (V_{IN} terminal) shown in Fig. 9-2-2 is used as the power supply circuit of the control IC.

When the power is turned on, C863 is charged by the starting resistors R862 and R863 with D863. As the V_{IN} terminal voltage reaches 16 V (typical), the control circuit is started by the function of the starting circuit.

As shown in Fig. 9-2-3, circuit current is limited to 100 μA maximum (V_{IN} = 14 V TC at 25C) until the control circuit starts, therefore, R862 and R863 are capacitated to have high resistance.

After the control circuit has started, winding voltage generated in the auxiliary winding ND of the transformer is rectifiably smoothed by D865 and C863 and the resultant voltage is supplied to the V_{IN} terminal (pin 5).

Since this voltage does not go up to the set voltage just after the control circuit starts operation, the V_{IN} voltage begins going down. However, the voltage of the auxiliary winding reaches the set value before the V_{IN} voltage extremely drops down since the operation stop voltage is set to 10 V (typical), and the control circuit accordingly continues operation.

The waveform of the V_{IN} voltage at the start of operation is shown in Fig. 9-2-4.

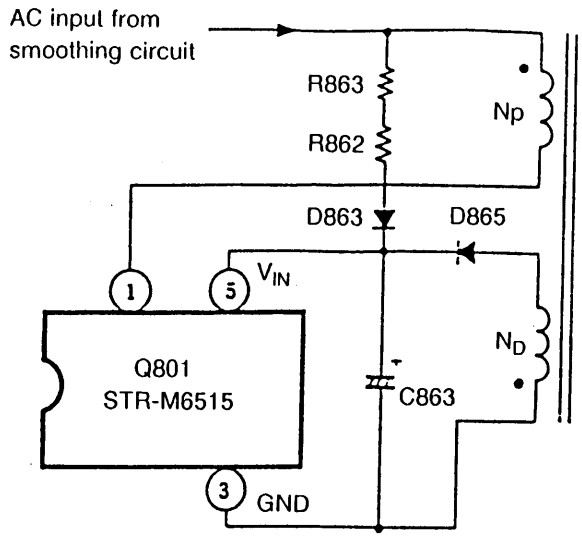


Fig. 9-2-2 Starter circuit

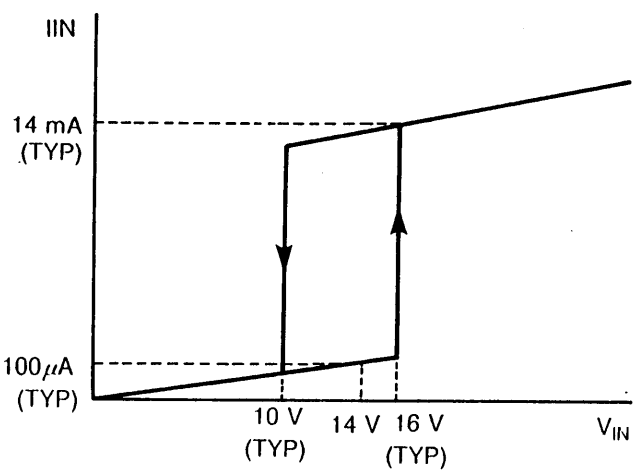


Fig. 9-2-3 V_{IN} terminal voltage, circuit current I_{IN}

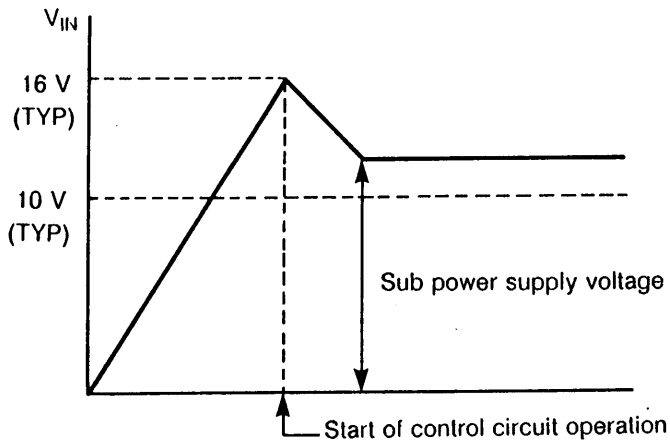


Fig. 9-2-4 Waveform of V_{IN} terminal voltage at start of operation

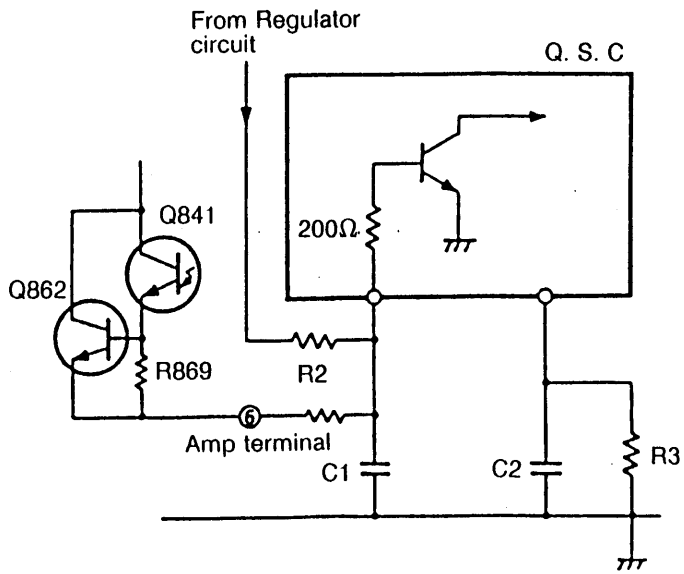


Fig. 9-2-5

9-6-2. Amp Terminal (pin 6), Oscillator, Constant-voltage Control Circuit

The oscillator is what charge and discharge of C1 and C2 built in the hybrid IC (HIC) are utilized, and it generates pulse signals to turn on and off the MOS FET.

In the switching power supply configuration, constant voltage control is operated by varying ON time of the MOS FET with its OFF time fixed except the case of light load, and ON time is varied by directly changing output pulse width of the oscillator.

Fig. 9-2-6 shows an operation of the oscillator with isolated operation of HIC (without constant voltage control), in which case the MOS FET is on and C2 is charged to the constant voltage (5 V approx.). On the other hand, C1 is charged through R2 from 0 V approximately, and the both end voltage is raised along a slope slope that is determined by the product of C1 and R2.

When the both end voltage of C1 reaches 0.75 V (Tc = 25C), oscillator output is inversed and the MOS FET is accordingly turned off. At the same time, the both end voltage is rapidly discharged by the internal circuit of the oscillator until it goes down to 0 V approximately.

As the MOS FET is turned off, R3 makes C2 begin discharge and C2's both end voltage goes down taking a slope that is determined by the product of C2 and R3.

When the both end voltage of C2 goes down to 3 V approximately, the oscillator output is again inversed and the MOS FET is accordingly turned on. At the same time, C2 is rapidly charged up to 5 V again.

By repetition of the above-mentioned operation, the MOS FET continuously turns on and off, therefore, C3 is charged with voltage that is shown in Fig. 9-2-7 and supplied through R861, R860, R887 and D864 from the ND winding in the off period of the MOS FET. In the next on period of the MOS FET, of course, it does not start turning-on operation since the both end voltage of C3 is higher than the threshold voltage (0.75 V) of the IOS terminal. But, when the both end voltage goes down under 0.75 V, the MOS FET is turned on after the period of T. The delay time is obtained by this operation.

C865 and C866 are resonance capacitors, while C869 is a capacitor to delay the turning-on time of the MOS FET. The circuit performing such operation as mentioned above is called the partial resonance circuit.

ON time is controlled by changing the charge current for C1. In detail, the photocoupler Q841 connected with the Amp terminal (pin 6) of the IC supplies a current corresponding to the output signal of the error amplifier Q845 which is connected with the secondary output to C1, and the charge current of C1 is resultingly changed.

As AC voltage of the power supply increases and load current decreases, current flowing into the Amp terminal increases and the ON time of the MOS FET becomes short.

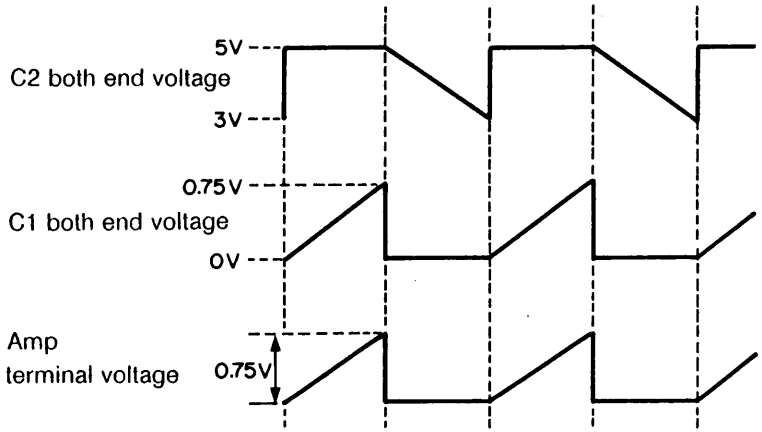


Fig. 9-2-6

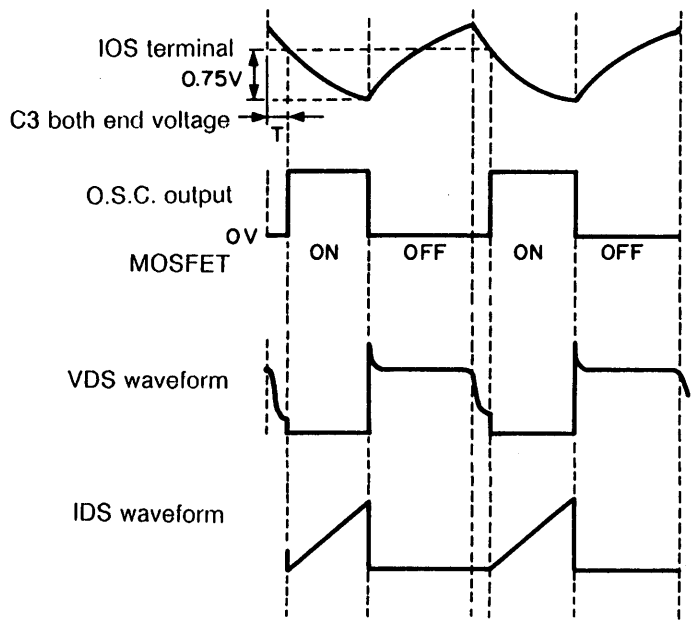


Fig. 9-2-7

9-6-3. Partial Resonance Circuit

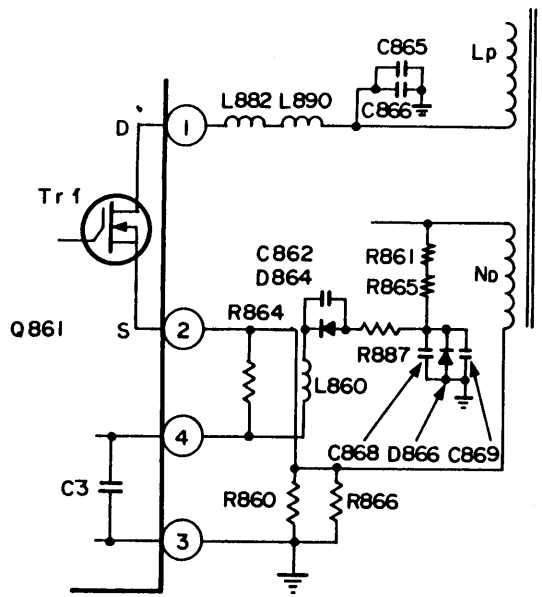


Fig. 9-2-8

In the OFF period of the MOS FET, charge current for C3 of the IOS terminal (pin 4) is supplied from the ND winding through R861, R865, R887, D864, L860 as shown in Fig. 9-2-9. However, the over-current protection circuit is not released from the duty in the OFF time since the threshold voltage of the IOS is 0.75 V or higher. Therefore, the MOS FET is turned on t period after the threshold voltage goes down under 0.75 V and the oscillator output is inversed.

In that period resonance ($2\pi\sqrt{LC}$) is yielded by the transformer Lp and C865, C866 to make C869 control delay of the turning-on time Tr. At the same time, a constant is set for the bottom point of the resonance voltage. As a result, loss in turning-on time and switching noise are remarkably reduced. D866 is a clamping diode to limit negative charge voltage of the integrating circuit consisting of R861, R865, C869. C862 and C868 are noise prevention capacitors.

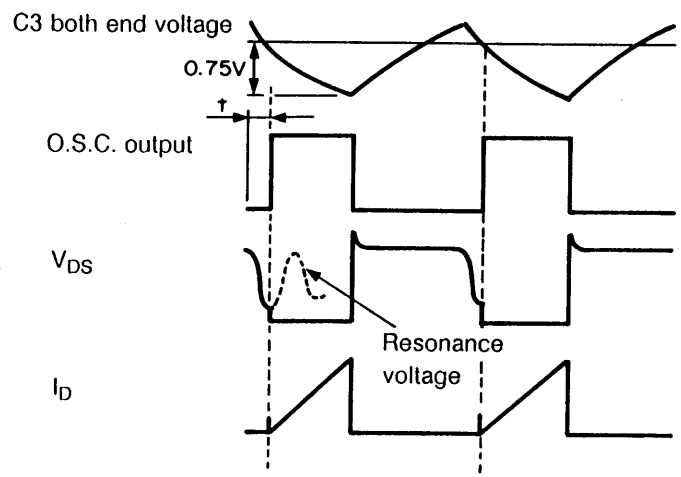


Fig. 9-2-9 Partial resonance circuit

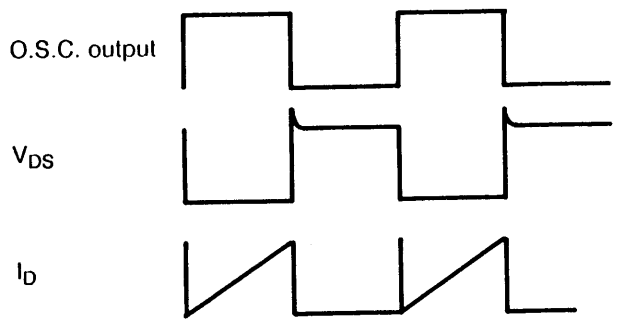


Fig. 9-2-10 Conventional circuit

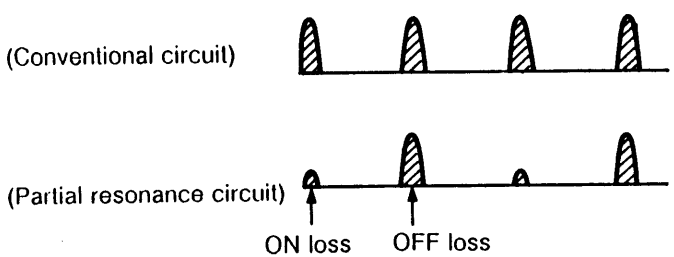


Fig. 9-2-11 Loss

9-6-4. Drive Circuit

With reception of pulse signal from the oscillator, this circuit charges and discharges capacitance between the gate and source of the power MOS FET.

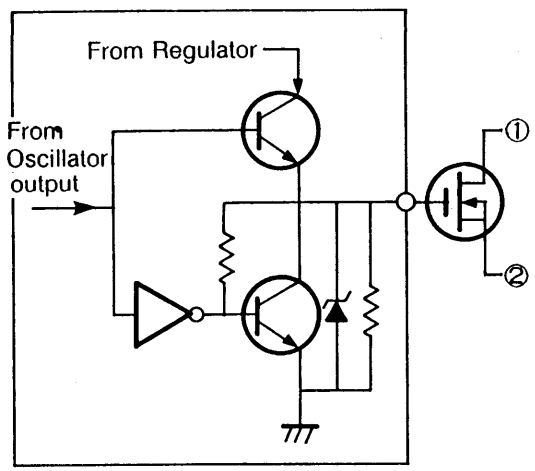


Fig. 9-2-12 Drive circuit

9-6-5. I_{OS} terminal (pin 4), O.C.P. (Over Current Protection) Circuit

Drain current of the MOS FET is detected by connecting R860 and R866 between the source terminal (pin 2) and the ground terminal (pin 3) of the MOS FET and inputting the resultingly dropped voltage to the I_{OS} terminal.

Threshold voltage of the I_{OS} terminal to the GND is 0.75 V approx. at the time that Tc = 23-C.

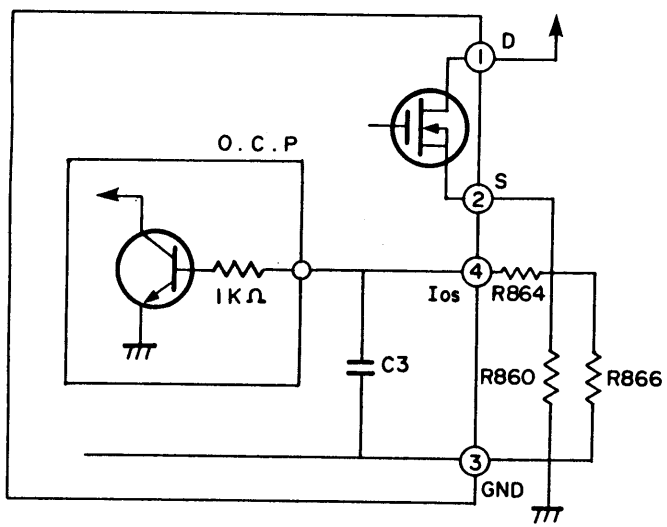


Fig. 9-2-13 Over-current detection circuit

9-6-6. Latch Circuit

The latch circuit is provided for protection of the over-voltage protection (OVP) circuit, the over-heat protection (TSD) circuit Q801. When the V_{IN} terminal voltage becomes abnormally high or the temperature of Q801 becomes high owing to something abnormal, this circuit holds the oscillator output at low level to stop the operation of the power supply circuit.

Even when the latch circuit is activated, the constant voltage power supply (Reg) circuit of the control circuit is in operation, thus, circuit current is still high and the V_{IN} terminal voltage drops down rapidly. When the V_{IN} terminal voltage drops down under the operation stop voltage (10 V, typical), the circuit current decreases under 400 μA and V_{IN} terminal voltage accordingly goes up.

Moreover, when the V_{IN} voltage reaches the operation start voltage (16 V, typical), the circuit current again increases and the voltage accordingly drops down again.

As mentioned above, the V_{IN} terminal voltage goes up (16 V, typical) and down (10 V, typical) repeatedly without abnormal increase during operation of the latch circuit, and Q801 is accordingly protected. Fig. 9-2-14 shows the waveform of the V_{IN} terminal voltage in the operation time of the latch circuit.

The operation of the latch circuit is cancelled by turning down the V_{IN} terminal voltage to 6.5 V or under. This operation is generally performed by switching off the AC power input once and switching it on again for restarting.

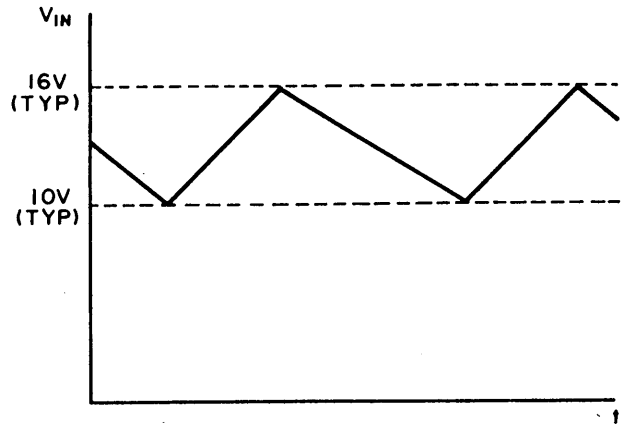


Fig. 9-2-14 Waveform of V_{IN} terminal voltage as latch circuit is in operation

9-6-7. Overheat Protection Circuit

This circuit activates the latch circuit when the frame temperature of the HIC (hybrid IC) exceeds 150C (typical). Temperature sensing is actually performed by the control circuit element, which is effective for overheat of the MOS FET because of the structure that the both are installed on the same frame.

9-6-8. Over-voltage Protection Circuit

This circuit activates the latch circuit when the V_{IN} terminal voltage exceeds 28.5 V (typical).

This circuit basically functions to prevent the V_{IN} terminal voltage of the control circuit from getting over-voltage. However, input to the V_{IN} terminal is generally supplied from the ND winding of the transformer and the input voltage is proportional to the output voltage, therefore, this circuit is activated with over-voltage of the secondary output when the control circuit is in open state. In this case, the secondary output power supply with the over-voltage protection operation can be explained by the following equation.

$$\text{Vout (OVP)} = \frac{\text{Output voltage (Vout) in normal operation}}{V_{IN}\text{ terminal voltage in normal operation}} \times 28.5\ \text{V (typ.)}$$

In actual operation, the over-voltage protection circuit of the secondary side has the priority over this circuit.

9-7. PROTECTION CIRCUITS (Fig. 9-3-1)

Outline

The P4100 series units are provided with some protection circuits to prevent the CRT and circuit devices from getting damage or trouble originating from something abnormal, over-voltage and over-current in the other circuit.

There are protection circuits of eight systems in the POWER and DEF P.C. boards, and, if any of those circuits detects something abnormal, the power relay is cut off.

Even when the main power supply to the unit is cut off, the thyristor (D862: SF0R3G42) is supplied with holding current from the standby power supply circuit through the resistor R874, and those protector circuits are held in operation. To release the unit from this condition, it is required to disconnect the power cord from the AC outlet once and connect it again and turn on the main switch a few seconds after the disconnection.

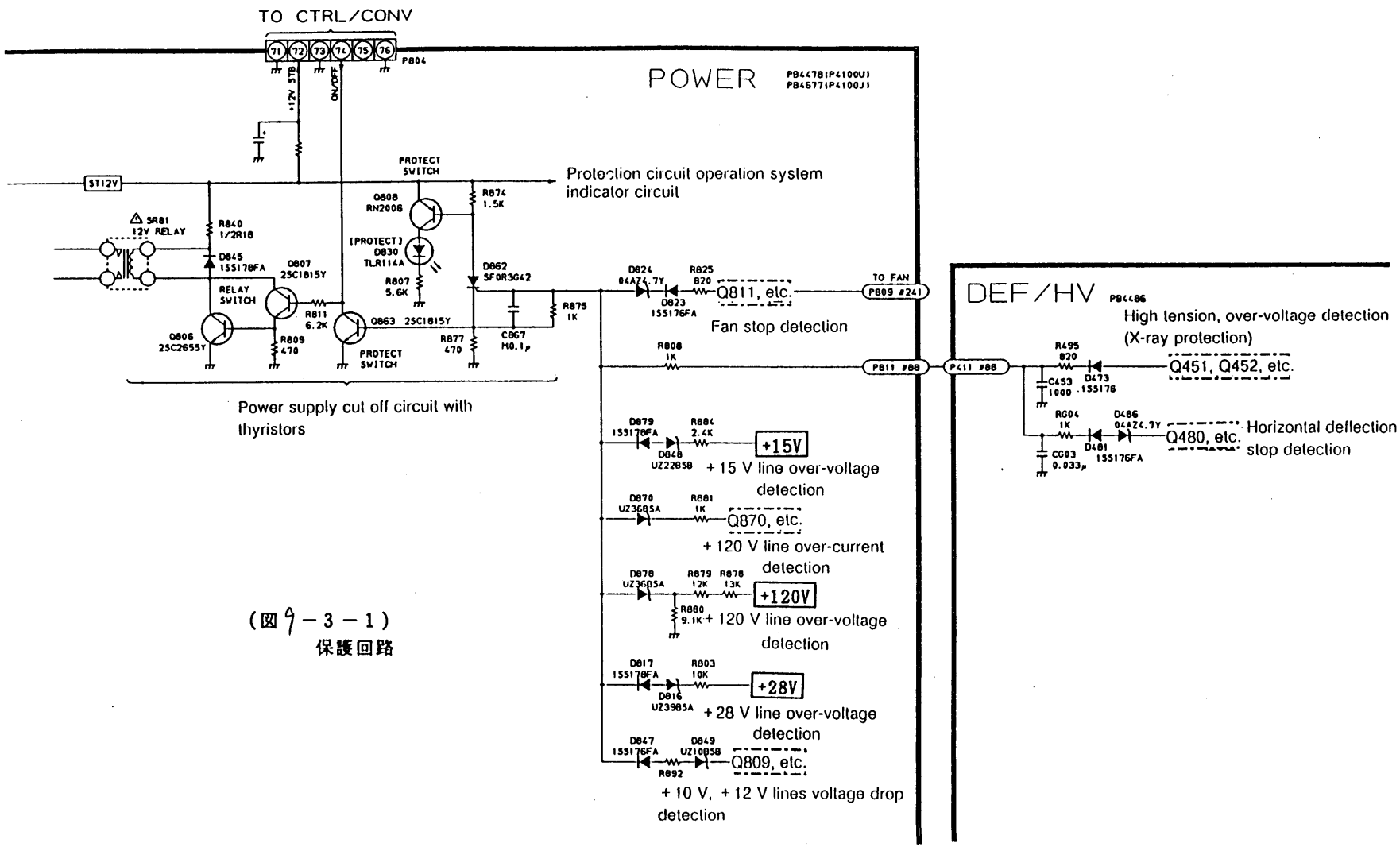
All the protection circuits of eight systems also serve as the power cutoff circuit with the thyristor, and the power relay is turned off to cut off the main power supply to the unit when any protection circuit is activated. Therefore, this unit employs the operation system indication circuit to show the system in trouble with LEDs. Explaining in detail, a green LED is provided for every protection circuit to indicate the activated protection circuit clearly and individually.

Addingly, a red LED (**PROTECT** : D830) is turned on being coupled with a green LED whenever there is a protection circuit in operation.

When the main power supply to the unit is cut off, for example, the red LED (**PROTECT** : D830) and a green LED (**X-RAY** : D850) are on to indicate that the X-ray protection circuit is activated and the main power is accordingly turned off. Detail of the LEDs is shown in the following table.

However, those LEDs are invisible from outside of the unit. For observing the LEDs, it is required to open the rear cover of the unit as the main power supply is kept connected.

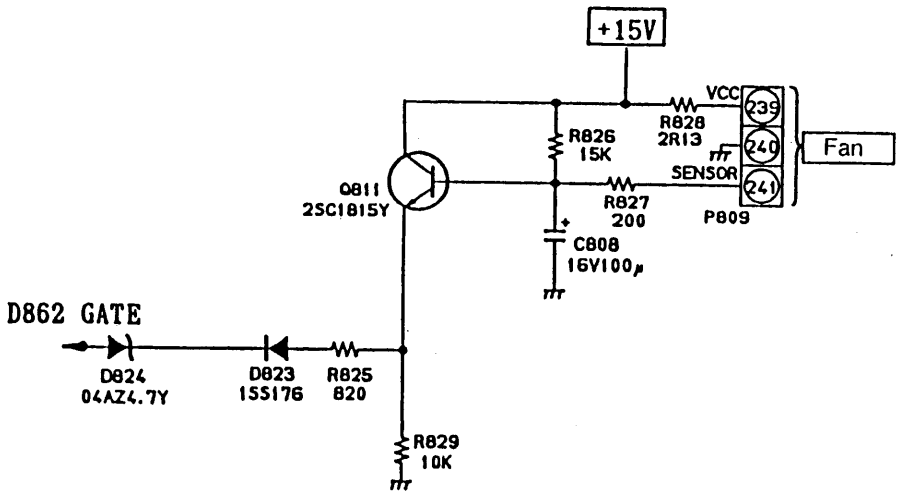
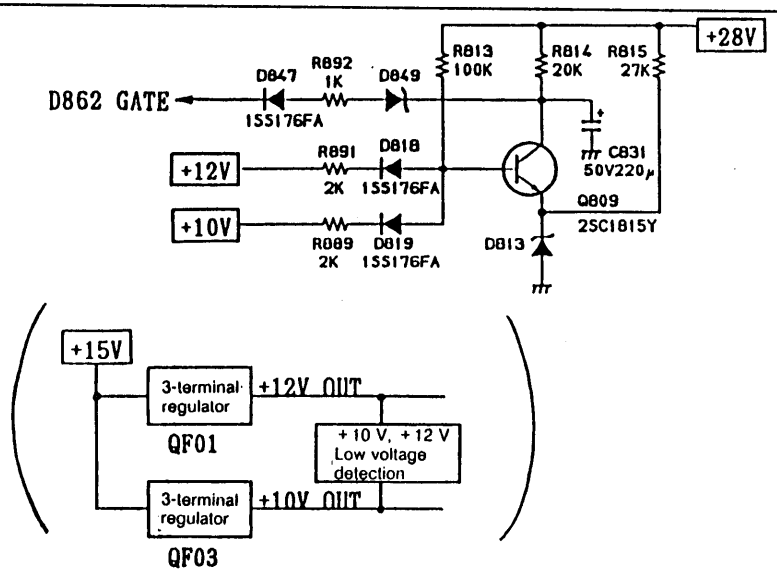
Part No.	P.C. board indication	Name of protection circuit
D850	**X-RAY**	High tension, over-voltage detection (X-ray protection)
D851	**H. STOP**	Horizontal deflection stop detection
D852	**FAN**	Fan stop detection
D853	**120 o. c**	+120 V line over-current detection
D854	**120 o. v**	+120 V line over-voltage detection
D855	**15 o. v**	+15 V line over-voltage detection
D856	**28 o. v**	+28 V line over-voltage detection
D857	**LOW V.**	+10 V, +12 V lines voltage drop detection
D830	**PROTECT**	———



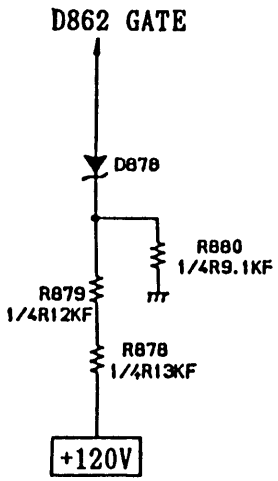
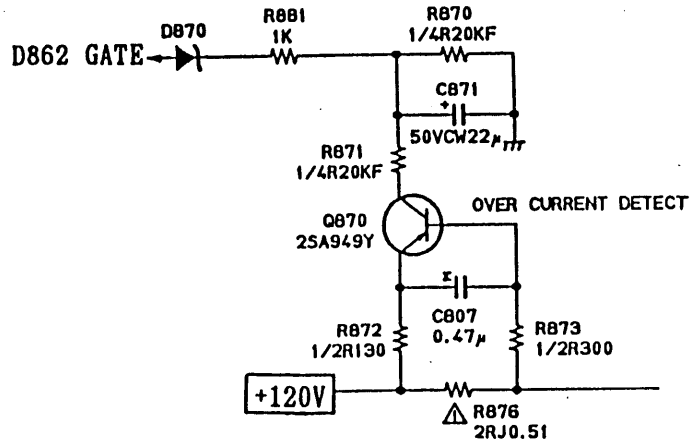
(図9－3－1)
保護回路

Fig. 9-3-1 Protection circuits

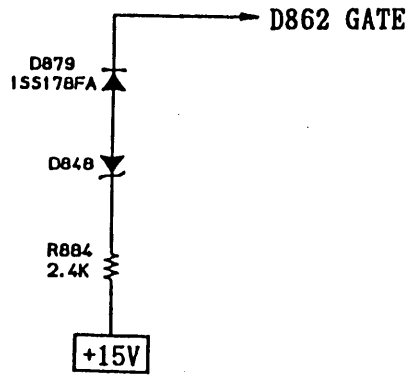
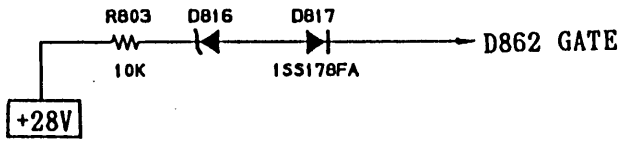
Protection Circuit (1)

Protection circuit name	Circuit construction	Detection point	Protection purpose	Cause of protector operation
Fan stop detection (POWER)		Operation status of fan inside the unit	Prevention of internal temperature increase when fan stops	1) Operation stop of fan 2) Disconnection of mini-connector P809
Low voltage detection (POWER)		Monitoring of each voltage in +10 V and +12 V lines	Prevention of abnormal heating of converter transformer (T862: TPW3272AD) for main power supply	1) Voltage drop of +10 V line 2) Voltage drop of +12 V line 3) Voltage drop of +15 V line

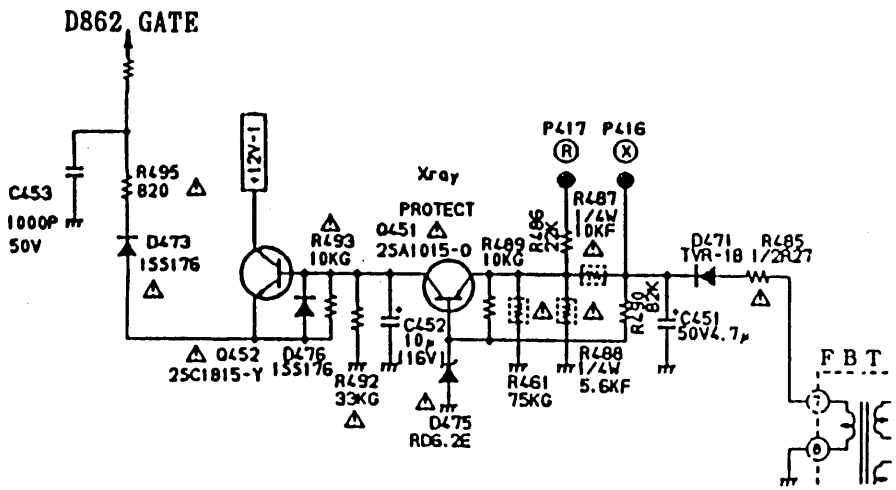
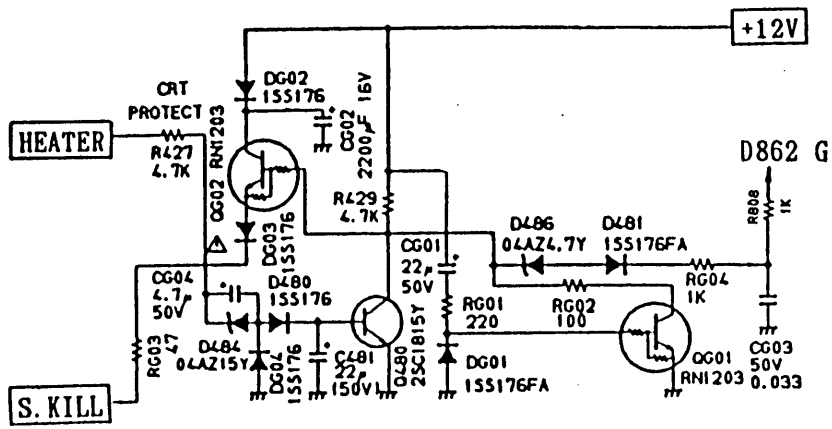
Protection Circuit (2)

Protection circuit name	Circuit construction	Detection point	Protection purpose	Cause of protector operation
+120 V line over-voltage detection (POWER)		Monitoring of each voltage in +120 V line	To prevent parts from getting damaged or increased in temperature caused by flyback of secondary voltage (high tension, +12 V, etc.) of flyback transformer and pulse transformer.	1) Fault in main power supply circuit (Shortcircuit between C and B of Q845, between pins 1 and 2 of Q841)
+120 V line over-current detection (POWER)		Detection of current intensity of +120 V line current at R876	Prevention of abnormal heating of converter transformer T862 (TPW3272AD)	1) Over-load resulting from faulty circuit, etc.

Protection Circuit (3)

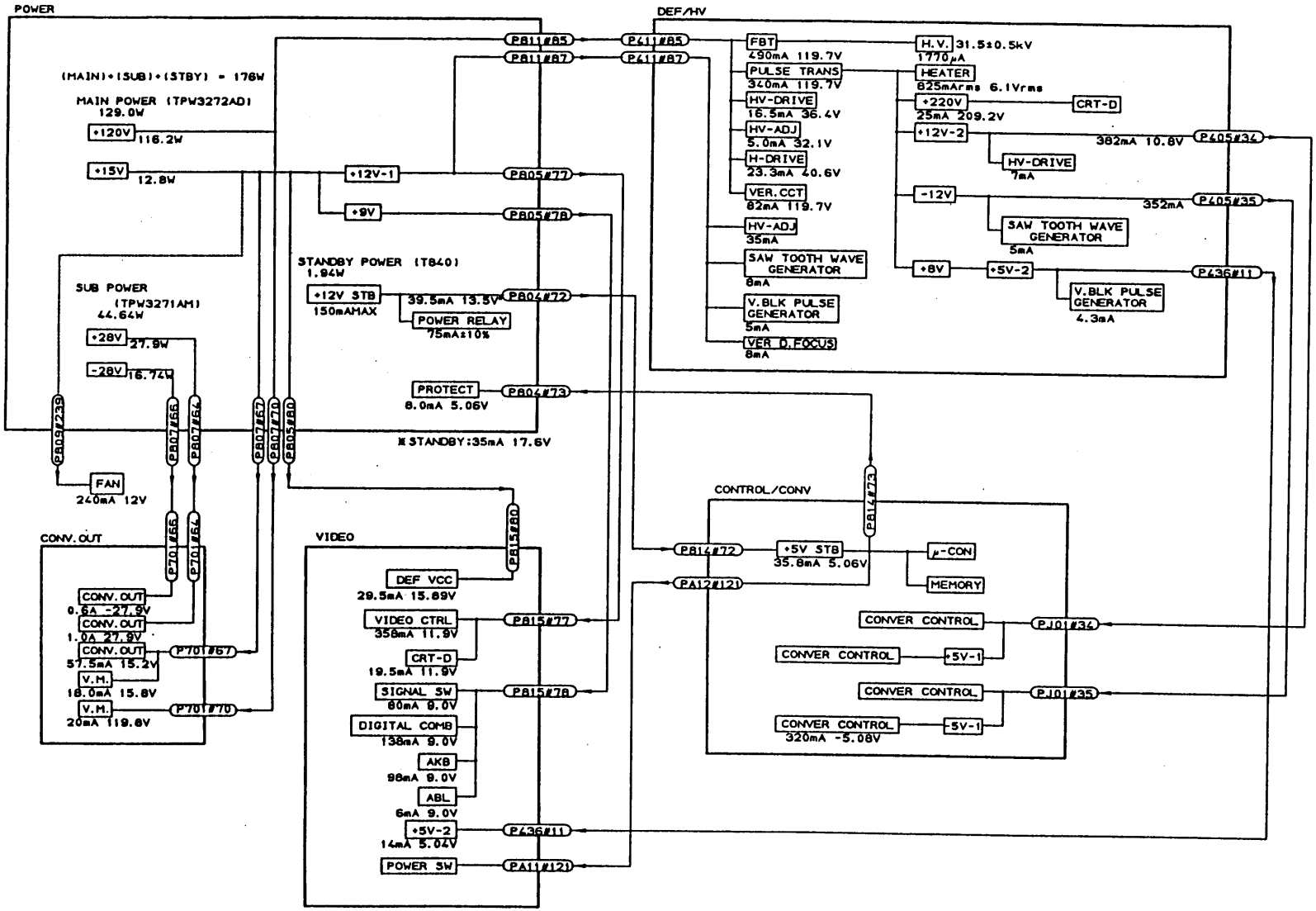
Protection circuit name	Circuit construction	Detection point	Protection purpose	Cause of protector operation
+15 V line over-voltage detection (POWER)		Monitoring of each voltage in +15 V line	Prevention of abnormal heating of 3-terminal regulator QF01, QF03 (input: +15 V, output: +10 V/ +12 V)	1) Fault in main power supply circuit (same as 120 V line over-voltage)
+28 V line over-voltage detection (POWER)		Monitoring of each voltage in +28 V line	To maintain reliability of converter output circuit	1) Fault in sub power supply circuit (shortciruit of R858, etc.)

Protection Circuit (4)

Protection circuit name	Circuit construction	Detection point	Protection purpose	Cause of protector operation
High tension, high voltage detection (X-ray protection) (DEF/HV)		Monitoring of voltage of high voltage detection (at pin 7 of Q461)	Prevention of increase in X-ray leakage caused by flyback of high tension	1) Increase of high tension level caused by fault in circuit (high tension output circuit, high voltage stabilizing circuit), etc. 2) Shortcircuit between test pins X and R (P416 and P417)
Horizontal deflection stop detection (DEF/HV)		Monitoring of heater voltage	CRT protection	1) Fault in horizontal deflection circuit

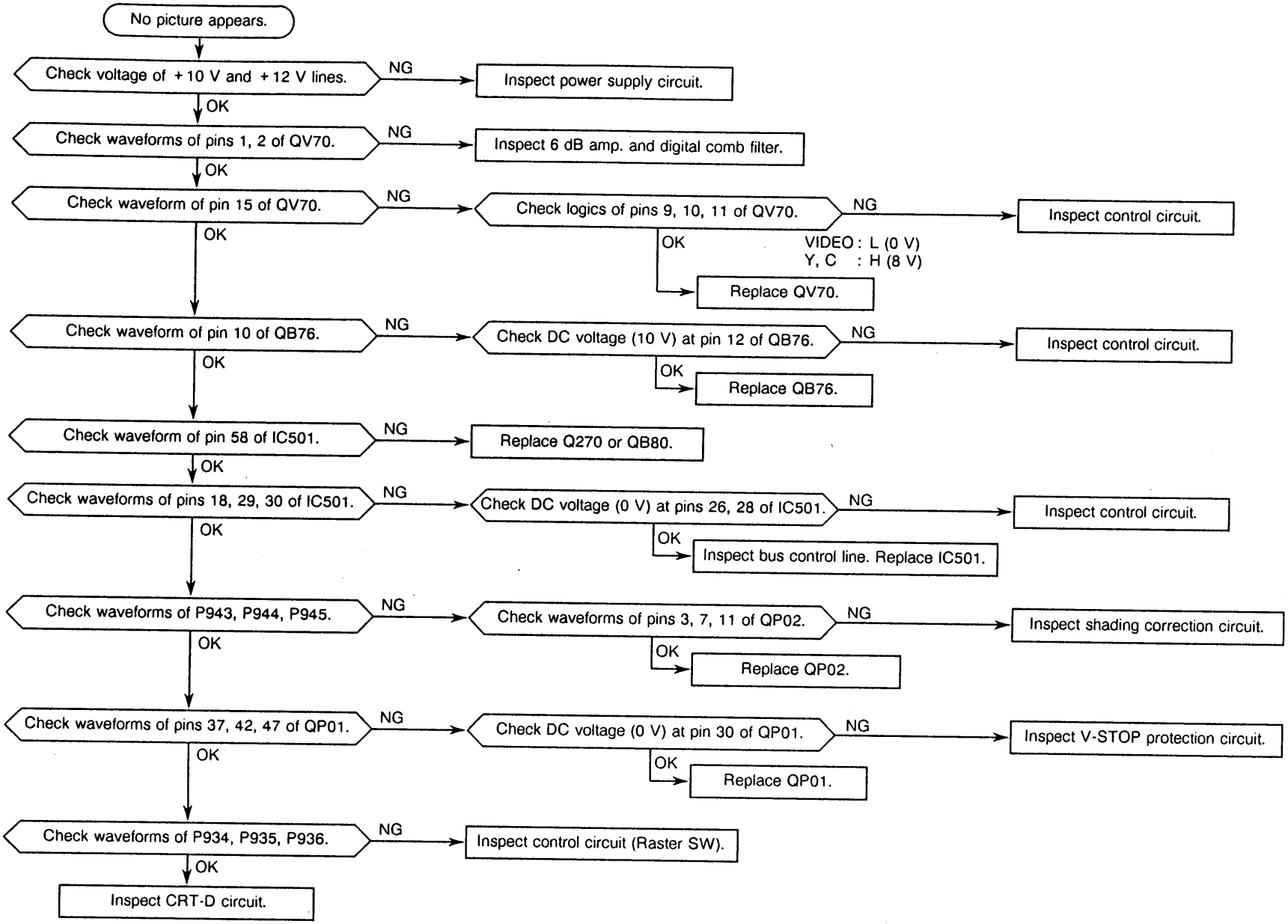
VIDEO WALL PJ (P4100) LOAD MAP

Measurement condition: In reception of NTSC RETMA signal (or 100 % white signal)

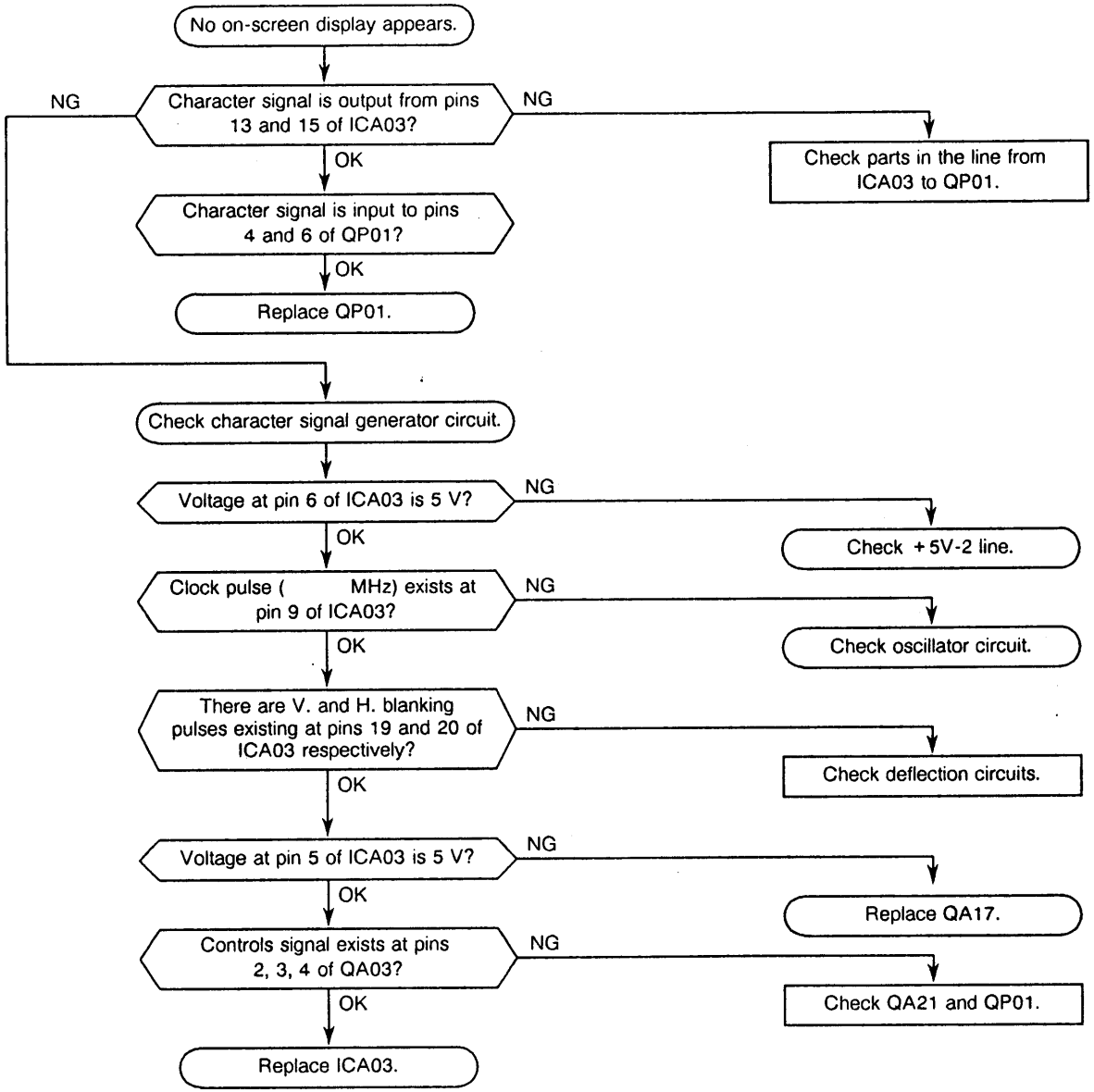


SECTION 10.
TROUBLESHOOTING

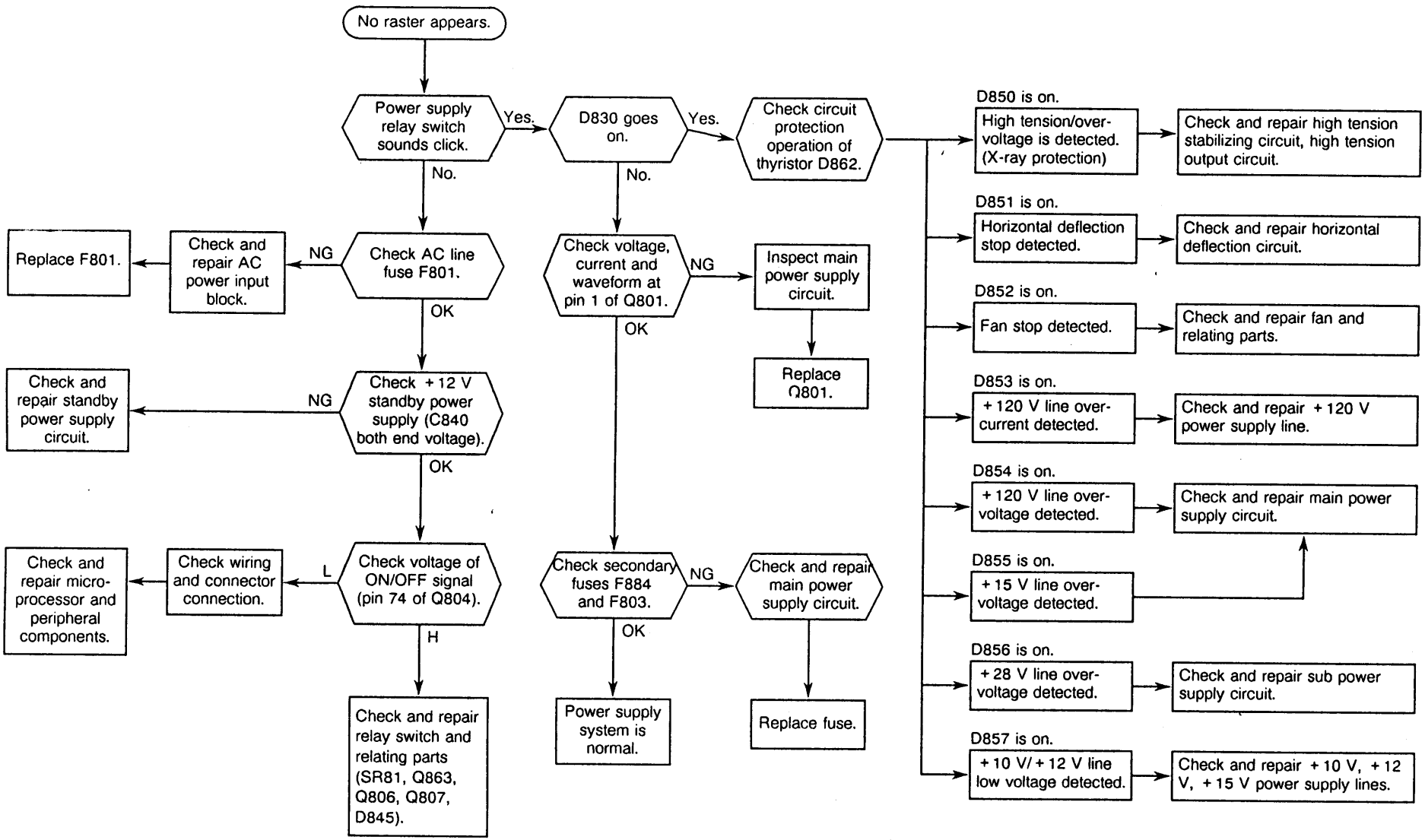
VIDEO BLOCK (with VIDEO signal, Y/C signal input)



No display of on-screen indication



Troubleshooting Procedure



TOSHIBA CORPORATION
1-1, SHIBAURA 1-CHOME, MINATO-KU, TOKYO 105, JAPAN