Circuit Descriptions, List of Abbreviations, and IC Data Sheets

Index of this chapter:

Notes:

- Only **new** circuits compared to the M8 (L01.1 for other regions) chassis are described in this chapter. For the other circuit descriptions, see the manual of the M8 (L01.1) chassis.
- Figures can deviate slightly from the actual situation, due to different set executions.
- For a good understanding of the following circuit descriptions, please use the diagrams in sections “Block Diagrams, ...”, and/or “Electrical Diagrams”. Where necessary, you will find a separate drawing for clarification.

Introduction

The 'L04' chassis is a global TV chassis for the model year 2004 and is used for TV sets with large screen sizes (from 21 to 36 inch), in Super Flat and Real Flat executions (both in 4:3 and 16:9 variants).
There are three types of CRT namely the 100 degrees, 110 degrees and Wide Screen CRT.

- The 100 deg. 4:3 CRT is raster-correction-free and does not need East/West Correction (except when used in AP regions), therefore the corrections needed are Horizontal Shift, Vertical Slope, Vertical Amplitude, Vertical S-Correction, Vertical Shift, and Vertical Zoom for geometry corrections.
- The 110 deg. 4:3 CRT comes with East/West Correction. In addition to the parameter mentioned above, it also needs the Horizontal Parallelogram, Horizontal Bow, Horizontal Shift, East/West Width, East/West Parabola, East/West Upper and Lower Corners, and East/West Trapezium correction.
- The Wide Screen TV sets have all the correction of the 110 deg. 4:3 CRTs and also have additional picture format like the 4:3 format, 16:9, 14:9, 16:9 zoom, subtitle zoom, and the Super-Wide picture format.

In comparison to its predecessor (the M8/L01.1), this chassis is has the following (new) features:

- Audio: The sound processor is part of the UOC processor (called “Hercules”).
- Video: Enhanced video features, video drivers, and Active Control.
- Control: Comparable to M8/L01.1 (e.g. Dual clock, I/O mapping, I/O switching).

- Power Supply: Adapted to supply the Hercules IC, and to enable 0.5 W Standby power dissipation. Also provisions are made for future extensions like DVD and iDTV.

The standard architecture consists of a Main panel (called 'family board'), a Picture Tube panel, a Side I/O panel, and a Top Control panel. The Main panel consists primarily of conventional components with some surface mounted devices in the audio and video processing part.
The functions for video/audio processing, microprocessor (P), and CC/Teletext (TXT) decoder are all combined in one IC (TDA1200x, item 7200), the so-called third generation Ultimate One Chip (UOC-III) or “Hercules”. This chip is mounted on the “solder” side of the main panel, and has the following features:

- Control, small signal, mono/stereo, and extensive Audio/Video switching in one IC.
- Upgrade with digital sound & video processing.
- Alignment free IF, including SECAM-L/L1 and AM.
- FM sound 4.5/5.5/6.0/6.5, no traps/bandpass filters.
- Full multi-standard color decoder.
- One Xtal reference for all functions (microprocessor, RCP, TXT/CC, RDS, color decoder, and stereo sound processor).

The tuning system features 181 channels with on-screen display. The main tuning system uses a tuner, a microcomputer, and a memory IC mounted on the main panel.
The microcomputer communicates with the memory IC, the customer keyboard, remote receiver, tuner, signal processor IC and the audio output IC via the I2C bus. The memory IC retains the settings for favorite stations, customer-preferred settings, and service / factory data.
The on-screen graphics and closed caption decoding are done within the microprocessor where they are added to the main signal.

The chassis uses a Switching Mode Power Supply (SMPS) for the main voltage source. The chassis has a 'hot' ground reference on the primary side and a cold ground reference on the secondary side of the power supply and the rest of the chassis.

Power Supply

Block Diagram

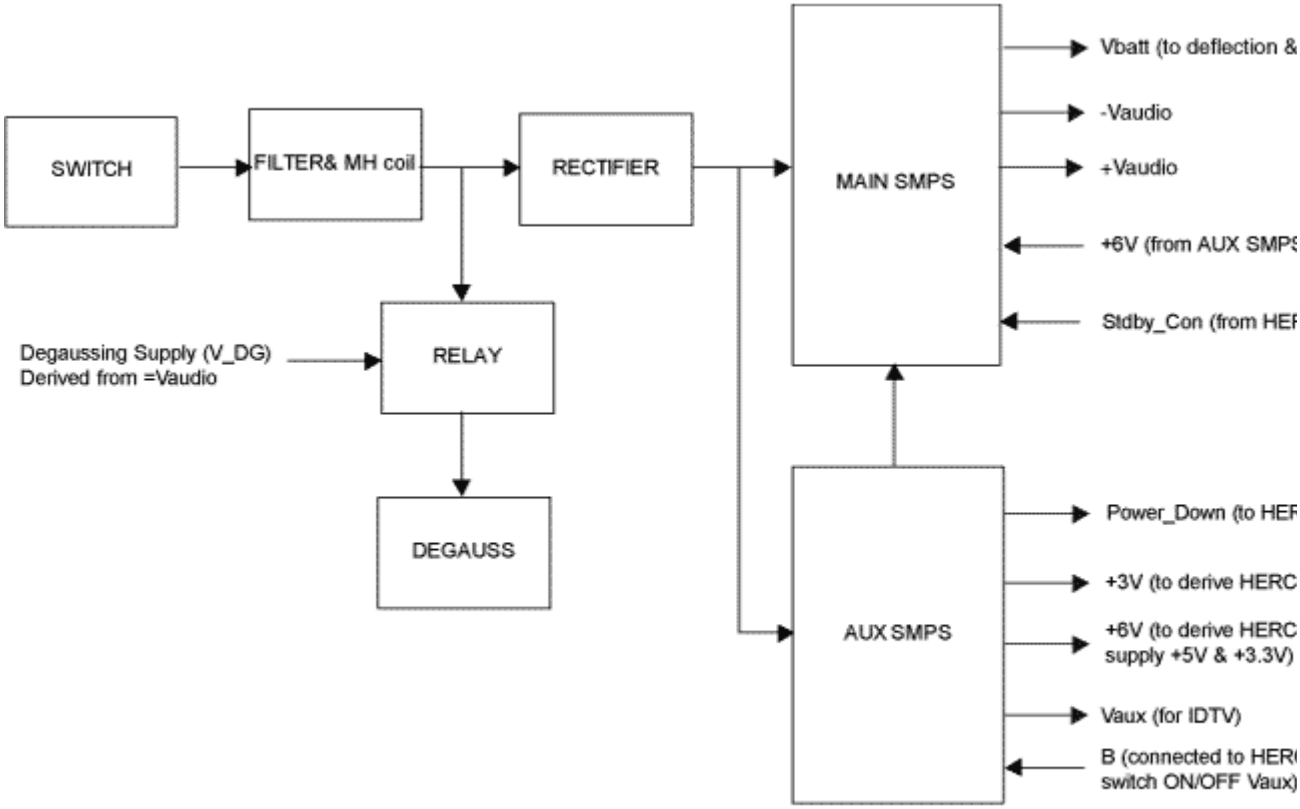


Figure: Block diagram power supply

Stdby_con signal

The Hercules generates this signal. This line is logic “low” (0 V) under normal operation and in semi-Standby of the TV, and is “high” (3.3 V) during Standby.

Power_down signal

The AUX SMPS generates this signal. It is logic “high” (3 .3 V) under normal operation of the TV and goes “low” (0 V) when the AC power (or Mains) input voltage supply goes below 70 V_ac.

B (Hercules port)

This port is used to switch the AUX SMPS output V_aux “On/Off”. This is required for DVD and iDTV (for future extensions).

Timing Diagrams

Power ON - To Standby - Out of Standby - Power OFF

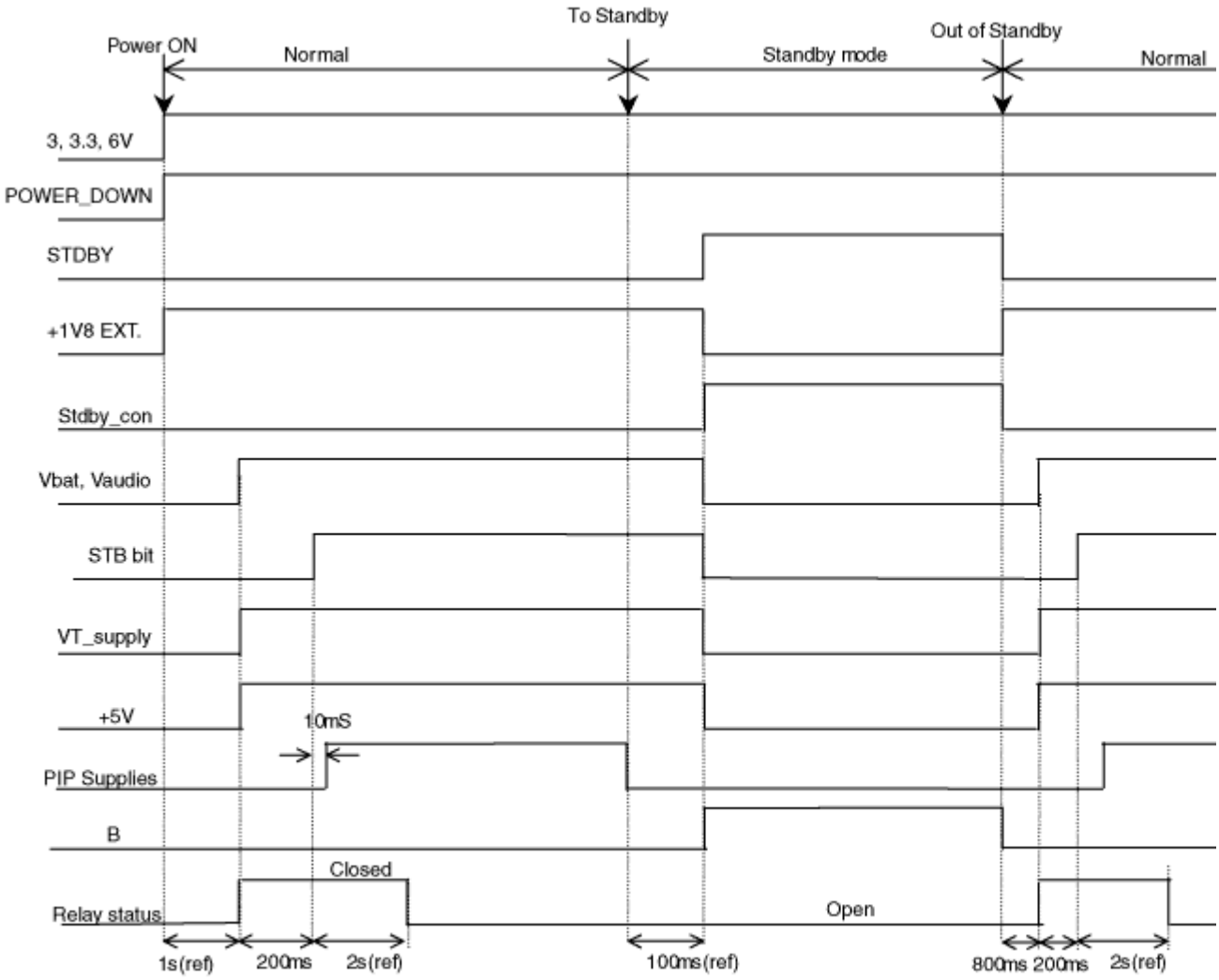


Figure: Timing diagram Standby

Power ON - To Semi Standby - Out of Semi Standby - Power OFF

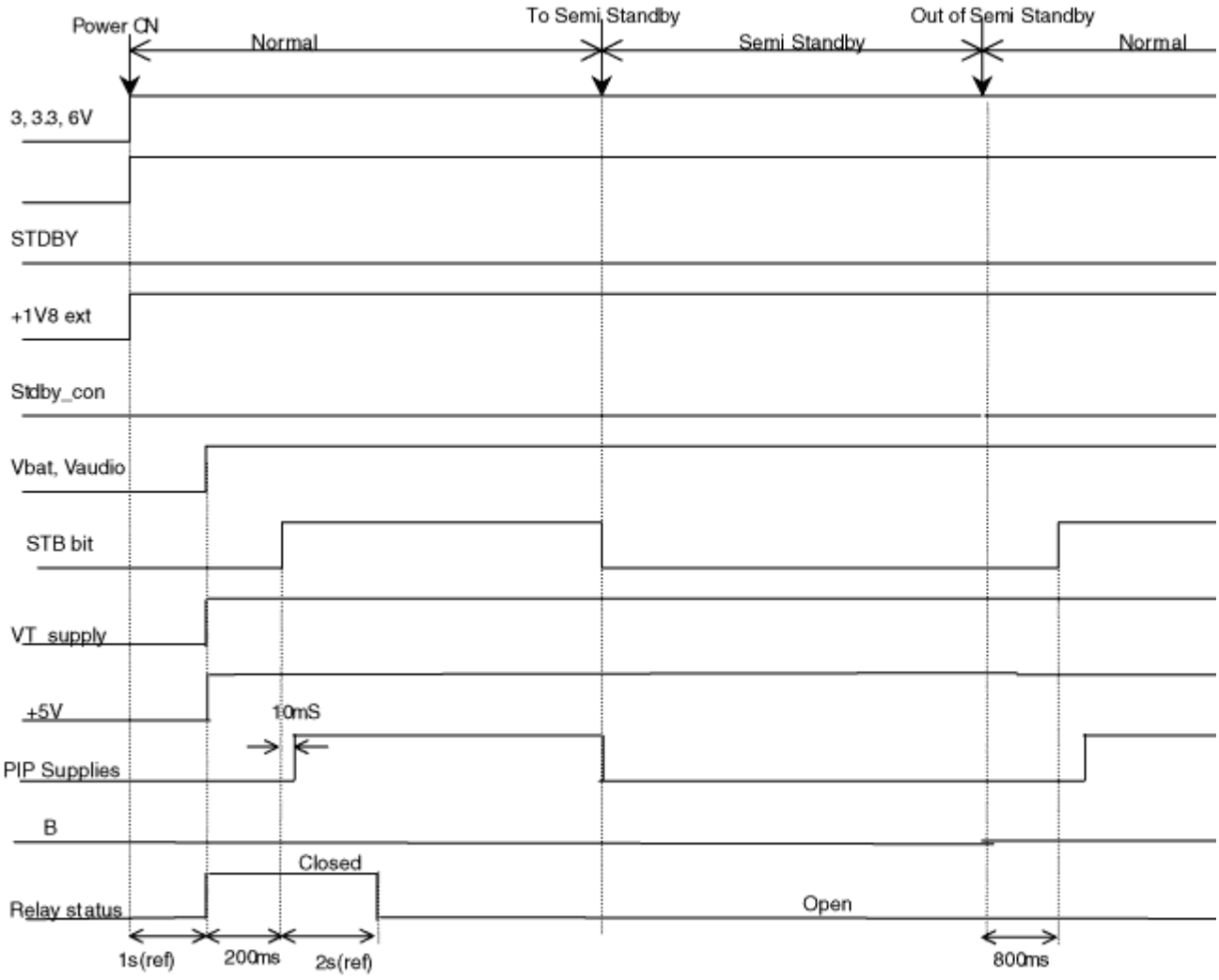


Figure: Timing diagram Semi Standby

Startup Sequence

When the set is connected to the AC power, the rectified line voltage (via winding 4-5 of L5531 connected to pin 14 of IC7531) will start the internal voltage source to charge the V_cc capacitor (C2532). The IC starts to switch as soon as the V_cc reaches the V_cc start level of 9.5 V. This supply is automatically taken over by winding 1-2, as soon as the V_cc is high enough, and the internal supply source will stop (for high efficiency switching).

Table: Pinning overview TEA1523

Pin	Symbol	Description
2	Gnd	This pin is Ground of the IC.
3	V_cc	This pin is connected to the supply voltage. An internal current charges the V_cc capacitor (2532), and the start-up sequence is initiated when this voltage reaches a level of 9.5

		V. Note: The output power is disabled when the voltage gets below 9 V (UVLO). Operating range is between 0 to 40 V.
5	RC	Frequency setting
6	REG	This pin is connected to the feedback loop. The pin contains two functions: 1) Between 1 to 1.425 V it controls the 'on' time. 2) Above the threshold of 3.5 V, it is possible to initiate 'burst mode' standby.
11	Demag	This pin is connected to the V_cc winding of 5531. It has three functions: 1) During Magnetisation, the input voltage is sensed to compensate OCP level for OPP. 2) During demagnetisation, the output voltage is sensed for OVP and 3) A comparator is used to prevent continuous conduction when output is overloaded.
12	Sense	This pin contains three different functions.: 1) Dectection of soft start, protection levels of 2) OCP, and 3) SWP.
14	Drain	This pin is connected to the drain of the switch or center tap of the transformer. It contains three functions: 1) M-level (mains-dependent operation-enabling level), 2) Supply for start-up current, and 3) Valley detection.

As C2532 of IC7531 is charged, it will also start to charge the V_cc capacitor (C2511) of IC7511. Via resistor R3519 and C2511, the TEA1506 starts to switch as soon as the V_cc voltage reaches the V_cc start level of is about 11 V. The V_cc voltage is automatically taken over by the main transformer L5512 (winding 2-3) when the V_cc is high enough (when this voltage is even higher than the voltage on C2511, there is no current flow from C2532 to C2511 due to diode D6512).

Table: Pinning overview TEA1506

Pin	Symbol	Description
2	Vcc	This pin is connected to the supply voltage. When this voltage is high (Vcc_start level, about 11 V), the IC will start switching. When the voltage is lower than Vcc_uvlo (about 8.7 V), the IC will stop switching.Note: This pin is not self supplied by internal source like in TEA1507
3	Gnd	This pin is Ground of the IC.
6	Ctrl	This pin is connected to the feedback loop. The pin will control the 'on' time between 1 V to 1.5 V.
7	Demag	This pin is connected to the Vcc winding of 5512. It contains three functions: 1) During magnetisation, the input voltage is sensed to compensate OCP level for OPP, 2) During demagnetisation, the output voltage is sensed for OVP and 3) a comparator is used to prevent continuous conduction when the output is overloaded.
9	Sense	This pin contains three different functions: 1) dectection of soft start, protection levels of 2) OCP, and 3) SWP.
11	Driver	This pin will drive the (MOSFET) switch.

12	HVS	This is High Volt Spacer (n.a.)
14	Drain	Connected to the Drain of the external MOSFET switch, this is the input for valley sensing and initial internal supply.

Standby Mode

In this mode, IC7511 (TEA1506) will be totally disabled. So there is no voltage on the main transformer output. But IC7531 (TEA1523) will still work and will provide the necessary output voltages (6V -> 5V, 3.3V, 3V -> 1.8V) to the Hercules (IC7200).

Table: PSU voltage overview

Voltage	Normal operation	Stdby mode
V_batt	130 - 143 V	0 V
V_audio	+/- 15.5 V	0 V
+6V	6 V	6 V
+3V	3 V	3 V
Stdby_con	0 V	3.3 V

Deflection

Synchronization

Before the Hercules (IC7200) can generate horizontal drive pulses, the +3.3V supply voltages must be present. After the start up command of the microprocessor (via I2C), the Hercules outputs the horizontal pulses. These horizontal pulses begin “initially” with double line frequency and then change “gradually” to line frequency in order to limit the current in the line stage (slow-start).

The VDRA and VDRB signals are the balanced output currents (sawtooth shaped) of the frame oscillator (pins 106 and 107 of the Hercules). These output signals are balanced, so they are less sensitive to disturbances.

There is a current source inside the UOC at pin 102. This pumps energy in the capacitor connected to this pin producing a pure saw tooth. The vertical drive signals and the E/W correction signal are derived.

Pin 108 is the East-West drive (or AVL), and it is a single ended current output. The correction for “horizontal width for changed EHT” from this pin is available by setting the HCO bit to “1”.

The Phase-2 Compensation available at pin 113 gives frame correction for high beam currents. The phase compensation signal is used to correct the phase of the picture from the horizontal drive signal.

Pin 63 is the SANDCASTLE output (contains all sync info) and also HORIZONTAL FLYBACK (HFB) input.
Pin 97 is the EHT tracking/over-voltage protection pin. The HCO bit can switch on the tracking on EW. If the voltage at pin 97 exceeds 3.9 V, the over-voltage protection will be activated and the horizontal drive is switched “off” via a slow stop.

Horizontal Deflection

There are several executions (depending on the CRT):

- **Sets with no East-West correction.** The principle of the horizontal deflection is based on the quasi-diode modulation circuit. This horizontal deflection circuit supplies the deflection current and auxiliary voltages from the LOT.
- **Sets with East-West correction.** The principle of the horizontal deflection is based on a diode modulator with east-west correction. This horizontal deflection circuit supplies the deflection current and auxiliary voltages from the LOT.
- **Sets with dynamic East-West correction.** The principle of the horizontal deflection is based on a diode modulator with dynamic east-west correction for picture tubes with inner pincushion. This horizontal deflection circuit supplies the deflection current and auxiliary voltages from the LOT.

Basic Principle

During a scan period, either the Line Transistor or diode(s) conduct to ensure a constant voltage over the deflection coil (that results in a linear current). During the flyback period, the Line Transistor stops conducting, and the flyback capacitor(s) together with the inductance of the deflection coil creates oscillation.

First Part of Scan

Pin 62 of the UOC delivers the horizontal drive signal for the Line Output stage. This signal is a square pulse of line frequency. L5402 is the flyback drive transformer. This transformer de-couples the line output stage from the UOC. It has a direct polarization. The flyback drive circuit works with the start-up supply taken from +6V of the Aux supply (and subsequently taking from VlotAux+9V). When the H-drive is high, TS7404 conducts, and transformer L5402 starts to store energy. The base of the line transistor TS7405 is low and therefore blocks. The current in the deflection coil returns from diode D6404.

Second Part of Scan

When the H-drive is low, TS7404 does not conduct, and the energy that is stored in the transformer will transfer to the secondary, making the base of the Line Transistor high. Then the Line Transistor starts to conduct. The current in the deflection coil returns from the transistor in another direction.

Flyback

At the moment the H-drive becomes high, the base of the Line Transistor becomes low. Both the Line Transistor and the Flyback Diode will block. There is an oscillation between the flyback capacitor C2412 and the deflection coil. Because of the inductance of the LOT, the Line Transistor cannot stop conducting immediately. After the Line Transistor is out of conduction, the flyback pulse is created. The flyback capacitor charges until the current in the deflection coil reduce to zero. Then it discharges through the deflection coil and the deflection current increases from the other direction. The flyback diode conducts and is back to the first part of the scan.

Linearity Correction

Because the deflection coil has a certain resistance, a picture without any linearity issues cannot be expected. L5401 is the linearity coil to compensate for this resistance. It is a coil with a pre-magnetized core. This correction is called linearity correction.

Horizontal S-Correction

Because the electronic beam needs to travel a longer distance to both sides of the screen than the center, the middle of the screen would become narrower than both sides. To prevent this, a parabolic voltage is applied across the deflection coil during scan. To create this parabolic voltage, a capacitor called S-cap (C2417/C2418) is used as a voltage source during scan. The sawtooth current of the deflection through this capacitor creates the required parabolic voltage. This correction is called S-Correction.

Mannheim-Circuit

When the EHT is heavily loaded with a bright line, the flyback time can be increased a bit in this situation. As a result, the scan delays a bit causing a DC-shift to the right in the next line, which would create a small spike on the S-cap. This spike oscillates with the inductance of the deflection coil and the primary of LOT. The result is visible in vertical lines under horizontal white line. This is called the Mannheim-effect.

To prevent this from happening, a circuit called Mannheim-circuit is added. This consists of C2415, R3404, R3417 and D6406. During the scan, C2415 is charged via R3417. During the flyback, the S-correction parabola across the S-Cap C2417/C2418 is in its most negative, and D6406 conducts. Thus, C2415 is switched in parallel to C2417/C2418 during flyback. As C2415 is much larger than C2417/C2418, the voltage across C2415 reduces the Mannheim-effect oscillation.

Class D East-West Driver

To reduce the power loss of the normal used linear East-West amplifier, a class-D East-West circuit is used. To achieve this, the East-West parabola waveform EW_DRIVE from the Hercules (frame frequency) is sampled with a saw tooth (line frequency) taken from the line aux output. Then a series of width-modulated pulses is formed via two inverted phase amplifiers, filtered by an inductor, which then directly drive the diode modulated line circuit.

East-West Correction

To achieve a good geometry, **dynamic** S-correction is needed. The design is such that the tube/yoke needs East-West correction. Besides that, an inner pincushion is present after East-West correction. The line deflection is modulated with a parabolic voltage (frame frequency). In this way it is not so much at top and bottom, and much more in the middle.

Upon entering the picture geometry menu in the SAM mode, the following corrections will be displayed.

- EWW: East West Width.
- EWP: East West Parabola.
- UCP: Upper Corner Parabola.
- LCP: Lower Corner Parabola.
- EWT: East West Trapezium.

The East-West drive circuit realizes them all. The settings can be changed by a remote control. All changed data will be stored into the NVM after the geometry alignment.

Panorama

For Wide Screen sets, the S-correction of the picture has to adapt between the different picture modes. In particular, between 16:9 Wide Screen and 4:3 picture modes. This is achieved with the (separate) Panorama circuit (see diagram “G”). A signal (I2SDI1) from the UOC controls the state of TS7463. When in the normal 16:9 Wide Screen mode, the signal is “low” and therefore TS7463 is switched “off”.
When the 4:3 mode is selected, this signal from the UOC is pulled “high”, switching TS7463 “on”. The relay 1463 on the Panorama panel is subsequently turned “on” and, in effect, paralleling capacitor C2475/C2474 to the S-Cap C2469/C2470. This changes the overall effective S-correction. The relay is switched “on” in 4:3 and Superwide picture modes.

Auxiliary Voltages

The horizontal deflection provides various auxiliary voltages derived either directly or indirectly from the secondary pins of the LOT:

- +9V: This supplies the Hercules's flyback driver.
- +11V: This supplies the frame amplifier.
- -12V: This supplies the frame amplifier.
- 50V: This supplies the frame amplifier.
- Filament: This supplies the heater pins of the picture tube.
- VideoSupply (+200V from primary side of LOT): This supplies the RGB amplifier and Scavem circuit at the CRT panel.

Notes:

- The V_T voltage (to tuner) is drawn from V_batt.
- The EHT voltage is generated by the Line Output Transformer (LOT). The Focus and Vg2 voltages are created with two potentiometers integrated in the transformer.

Beam Current

The beam current is adjusted with R3451 and R3452. The components R3473, R3453 and C2451 determine the EHT_info characteristic. The voltage across C2412 varies when the beam current changes. This EHT_info is used to compensate the picture geometry via pin 97 of the Hercules when the picture changes rapidly, and compensate the phase 2 loop via pin 113 of the Hercules. Also from the EHT_info line, a BCL signal is derived and sent to the Hercules for controlling the picture's contrast and brightness.

When the picture content becomes brighter, it will introduce:

- Geometry distortion due to the impedance of the LOT causing the EHT to drop.
- Picture blooming due to the picture characteristics

Because of the above mentioned, we will need a circuit for Beam Current Limiter (BCL) and EHT compensation (EHT_info). These two circuits derive the signal from the picture tube current info through LOT pin 10.

BCL

- When the BCL pin voltage goes to 2.8 V, the Hercules will start to limit CONTRAST gain.
- When it reaches 1.7 V, then the BRIGHTNESS gain limit will start to react.
- When BCL pin voltage goes to 0.8 V, the RGB will be blanked.

Components TS7483, R3490, R3491, R3492, and C2483 are for fast beam current limiting (e.g. with a Black-to-White pattern).

Components R3454, D6451, D6450, C2453, R3493, and C2230 are for average beam current limiting. C2453 and R3493 also control the timing where average beam current limiting is more active or less active.

EHT_info

The “PHI2 correction” is to correct the storage time deviation of the Line Output Transistor, which is causing geometry distortion due to brightness change.
Line EHT_info is to correct the geometry distortion due to EHT deviation.
Both of them feedback through the EHTO and PH2LF pin, and correct the geometry through the East-West circuit.

Power Down

The power down connection is for EHT discharge during AC Power “Off” state. In the Hercules, if EHT_info > 3.9 V, it will trigger the X-ray protection circuit via a 2fH soft stop sequence. The Hercules bits OSO (Switch Off in Vertical Over scan) and FBC (Fixed Beam Current Switch Off) will discharge the EHT with 1mA cathode current at over-scan position.
During switch-off, the H_out frequency is doubled immediately and the duty cycle is set to 25% fixed, during 43 ms. The RGB outputs are driven “high” to get a controlled discharge of the picture tube with 1 mA during 38 ms. This will decrease the EHT to about half the nominal value (= safety requirement). When bit OSO is set, the white spot/flash during switch-off will be written in overscan and thus will not be visible on the screen. Careful application must guarantee that the vertical deflection stays operational until the end of the discharge period.

DAF

The Dynamic Astigmatic Focus (DAF) circuit is required by 34RF sets only. It provides vertical DAF and horizontal DAF. Both of the parabola signals are derived through integration by using chassis available signals:

- The vertical parabola is using RC integration (via R3403 and C2401) on the Frame sensing resistor saw tooth (Frame_FB).
- The horizontal parabola is obtained by 2 RC integration (R3409, R3410, C2402, C2403) on the +9V LOT output.

Both of the parabolas are added on the output stage through adder TS7402 and TS7403. The collector of TS7402 emitter-drives TS7401 and is amplified by pull up resistor R3411. D6401 and C2405 provide the rectified supply voltage.

X-ray Protection

The X-ray protection circuit rectifies the filament voltage and uses it to trigger TS7481 when the EHT is too high. TS7481 is biased at “off” condition by D6480, R3482, and R3483 during normal

operation. When the EHT goes too high, the voltage across R3482 will tend to increase as well, while the voltage across D6481 is fixed. Up to certain level (triggering point), TS7481 will be “on” and will force the EHT_info > 3.9 V. The chassis will be shut down through a soft stop sequence.

Vertical Deflection

The Frame stage consists fully of discrete components. This has the advantage for better flash behavior than when an IC was used.

The Frame differential drive signal from the Hercules comes from a current source. Resistors R3460 and R3461 convert them into a voltage, and feed them into the differential amplifier TS7455 and TS7456. The output of TS7456 is input to the next amplification stage of TS7452. Finally, TS7451 and TS7453 deliver the Vertical yoke current to the coil and feedback through the sensing resistors R3471 and R3472.
D6458 and TS7454 are used to bias TS7451 and TS7453, to get rid of zero crossovers, which can cause horizontal lines at the screen center.
The negative supply is from -12V and the positive scanning supply is from +12V through D6459. The flyback supply is derived from D6455, D6456 and C2456. This circuit is a voltage doubler, which stores energy in C2456 during the Line flyback period and delivers the energy to C2465 during the Line scanning period. Throughout the Frame period, the charging and discharging of C2456 works alternatively. However, at the first half of the Frame scanning, TS7451 is “on” and consumes all the charge from C2456. When entering 2nd half Frame period, TS7451 is “off”, so C2456 will gradually charge up to the required flyback supply.

C2463, R3464 and D6457 are for boosting the base voltage of TS7451 during the flyback period and the 1st half Frame period as well. C2463 is charged by D6457 during the 2nd half scanning. R3467 and R3468 are for oscillation damping.

The V_guard protection is to protect the Frame stage if a fault condition happens. The V_guard will sense the pulse with voltage > 3.8 V and period < 900 us. Any signal out of this range will be considered as fault, and the chassis will be shut down.

Tilt and Rotation

The rotation control signal is a PWM output from the UOC. It is filtered by R3252, R3246, R3259 and C2259. The DC voltage after filtering at C2259 will be amplified by R3245 (Main Board) and R3390 (CRT panel).
The output stage functions similarly as in M8/L01.1 with rotation IC TDA8941P. TS7331/TS7382 and TS7332/TS7381 will function alternatively corresponding to the rotation setting.

CRT panel

The RGB amplifier stage is exactly the same as in M8/L01.1. However, the RGB amplifier IC has been changed to TDA6107AJF or TDA6108AJF. The “A” indication is with gain of “80” rather than “50” in M8/L01.1. The diode D6332 used in the former chassis, to solve the bright screen during start up, is not required because this IC has the error correction implemented.

Scavem

In certain versions, the Scavem feature is used to enhance the sharpness of the picture. The RGB signals are first differentiated and subsequently amplified before feeding to an auxiliary coil known as the SVM coil. The current, flowing through the SVM coil during the picture intensity transients, modulates the deflection field and thus the scan velocity.

During the first half of the intensity increase, the scan velocity is increased (thus decreasing the current density by spreading it on a wider area). During the second half of the intensity increase, the scan velocity is decreased (increasing the current density by concentrating it on a smaller area). The increasing current density transition is sharpened. A decreasing current density transition is processed in a similar way and is also sharpened.

In this chassis the SCAVEM signal is different from its predecessor because the Hercules generates the differential SCAVEM signal inside the IC.
The supply of the SCAVEM is taken from V_bat through a 1k5 / 5 W resistor. Compared with the M8/L01.1, this has the advantage of getting better performance for the pattern with tremendous SCAVEM current (like V_sweep). In this former chassis, because the supply was taken from the 200 V through a 8k2 / 5 W resistor, the supply dropped significantly during a large SCAVEM current. In this chassis, the drop due to the pattern will be less because of the lower supply voltage impedance.
In the Main Board, 1st stage amplification is taken care by 7208 with the pull up resistors (3361, 3387) located in the CRT panel.

TS7361 and TS7362 is the current buffer delivering the current to the output stage. The diode D6361 is to lightly bias these transistors, to get rid of the zero crossover of the stage.
After that, the signal is ac-coupled to TS7363 and TS7364 where the emitter resistors (R3364 and R3370) will determine the final SCAVEM current. TS7363 and TS7364 are biased by R3363, R3366, R3367 and R3368.
C2387, R3388, R3389, R3365, R3369, C2384, and C2385 are used for suppressing unwanted oscillations.
The function of TS7376 is to limit the SCAVEM current from going too high. It basically senses the voltage after R3373 and clamps the SCAVEM signal through D6367 and C2376.

Control

The Micro Controller is integrated with the Video Processor, and is called the Hercules. For dynamic data storage, such as SMART PICTURE and SMART SOUND settings, an external NVM IC is being used.
Another feature includes an optional Teletext/Closed Caption decoder with the possibility of different page storage depending on the Hercules type number.

The Micro Controller ranges in ROM from 128 kB with no TXT-decoder to 128 kB with a 10 page Teletext or with Closed Caption.

Block Diagram

The block diagram of the Micro Controller application is shown below.

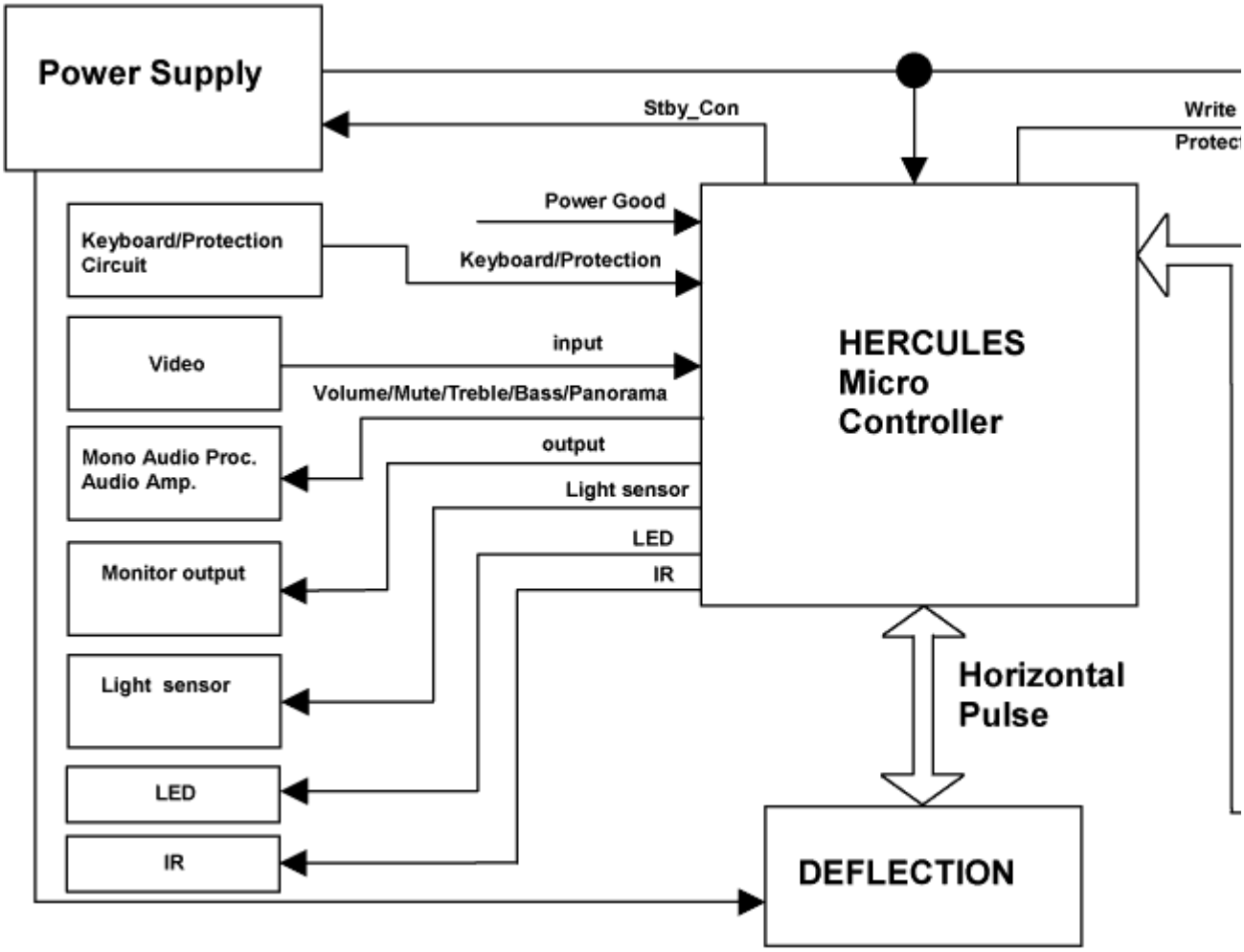


Figure: Micro Controller block diagram

Basic Specification

The Micro Controller operates at the following supply voltages:

- +3.3 V_dc at pins 33, 125, and 19.
- +1.8 V_dc at pins 126, 36, and 33.
- I2C pull up supply: +3.3V_dc.

Pin Configuration and Functionality

The ports of the Micro Controller can be configured as follows:

- A normal input port.
- An input ADC port.
- An output Open Drain port.
- An output Push-Pull port.
- An output PWM port.
- Input/Output Port

The following table shows the ports used for the L04 control:

Table: Micro Controller ports overview

Pin	Name	Description	Configuration
32	INT0/ P0.5	IR	INT0
31	P1.0/ INT1	PWRDOWN	INT1
30	P1.1/ T0	LED	P1.1
27	P0.4/ I2SWS	(for future use)	-
26	P0.3/ I2SCLK	(for future use)	-
25	P0.2/ I2SDO2	SEL_SC2_INTERFACE/ SDM	P0.2
24	P0.1/ I2SDO1	(for future use)	P0.1
23	P0.0/ I2SDI/O	Panorama	P0.0
22	P1.3/ T1	Write Protect	P1.3
21	P1.6/ SCL	SCL	SCL
20	P1.7/ SDA	SDA	SDA
18	P2.0/ TPWM	VOL_MUTE	P2.0
17	P2.1/ PWM0	ROTATION	PWM0
16	P2.2/ PWM1	SEL_LL'/M	P2.2
15	P2.3/ PWM2	STANDBY_CON	P2.3
14	P3.0/ ADC0	Light Sensor	ADC0
13	P3.1/ ADC1	(for future use)	-
10	P3.2/ ADC2	(for future use)	-
9	P3.3/ ADC3	KEYBOARD	ADC3
7	P2.4/ PWM3	A (for future use)	P2.4
6	P2.5/ PWM4	B (for future use)	P2.5
3	P1.2/ INT2	C (for future use)	INT2
2	P1.4/ RX	E (for future use)	-
1	P1.5/ TX	D (for future use)	-

The description of each functional pin is explained below:

- **LED.** This signal is used as an indication for the Standby, Remote and Error Indicator. Region diversity:
  - During protection mode, the LED blinks and the set is in standby mode.
  - During error conditions it blinks at a predefined rate.
  - After receiving a valid RC-5 or local keyboard command it flashes once.
  - For sets with error message indication, the LED blinks when message is active and the set is in standby mode.

Table: LED signal diversity

LED	Europe	AP/ LATAM	NAFTA			
0	LED brighter	Standby	LED lighted	Standby	LED lighted	Normal
1	LED dimmer	Normal	LED 'off'	Normal	LED 'off'	Standby

- **SCL.** This is the clock wire of the two-wire single master bi-directional I2C bus.
- **SDA.** This is the data wire of the two-wire single master bi-directional I2C bus.
- **STDBY_CON.** The Hercules generates this signal. This can enable the MAIN SMPS in normal operation and disable it during Standby. It is of logic “low” (0 V) under normal operation and “high” (3.3 V) during Standby.
- **IR.** This input pin is connected to an RC5 remote control receiver.
- **SEL-IF-LL'/ M-TRAP.** For AP: All L04 AP sets are Multi System QSS set. This is an output pin to switch the Video SAW filter between M system and other systems.
  - 0: NTSC M (default)
  - 1: PAL B/G, DK, I, L
- **Write Protect.** The global protection line is used to enable and disable write protection to the NVM. When write to the NVM is required, pin 7 of the NVM must be pulled to logic '0' first (via Write_Protect of the micro-controller pin) before a write is performed. Otherwise pin 7 of NVM must always be at logic “1”
  - 0: Disabled
  - 1: Enabled (default)
- **Mute.** This pin is use to MUTE the audio amplifier. It is configured as push pull.
- **Rotation.** This pin is configured as PWM for the Rotation feature. The output of the PWM is proportional to the feature control.
- **Light Sensor.** This pin is configured as ADC input for the Light Sensor.
- **Sel_SC2_Interface.** This pin is use to switch between the SC2_CVBS_OUT and the INTF_CVBS_OUT for the SCART_2_CVBS_OUT/ MONITOR_OUT signal.
  - 0: Hercules CVBS Output (default)
  - 1: Interface CVBS Output
- **PWRDOWN.** The AUX SMPS generates this signal. Logic “high” (3.3 V) under normal operation of the TV and goes “low” (0 V) when the Mains input voltage supply goes below 70 V_ac.
- **Keyboard.** Following are the Keyboard functions and the step values (8 bit) for it.

Table: Local keyboard values

Function	Voltage (V_dc)	Step values (8 bit)
NAFTA Standby	0	0 - 6
Ch +	0.43	7 - 33
Exit Factory (Ch- and Vol-)	0.69	34 - 53
Ch -	0.93	54 - 73
Menu (Vol - and Vol +)	1.19	74 - 96
Vol -	1.49	97 - 121

DVD Eject	1.8	122 - 147
Vol +	2.12	148 - 169

- **SDM.** This pin is configured as Open Drain during the cold start only. If this pin is shorted to ground during cold start, it will enter the SDM mode (for Service use).
- **ISP.** This pin is configured as Open Drain during the cold start only. If this pin is shorted to ground during cold start, it will enter the ISP mode (for Service use).
- **PANEL.** This pin is configured as Open Drain during the cold start only. If this pin is shorted to ground during that, then it will enter to the PANEL mode.
- **ResetEnabled.** This is an output pin to switch the control transistor (pos. TS7202) “high” or “low” for the reset of 1.8 V in case there is a corruption in the Hercules.

Tuner and IF

The tuner used in this chassis comes from two sources, from Philips and from Alps. Both tuner sources have the same pin configuration so they are 1 to 1 compatible except for the software, which will be selected by means of Option Settings.

Some features:

- Multi-Standard alignment free PLL-IF, including SECAM L/L'.
- Integrated IF-AGC time constant.
- Integrated sound band-passes and traps (4.5 / 5.5 / 6.0 / 6.5 MHz).
- Group delay compensation (for NTSC and for PAL).
- QSS versions with digital Second-Sound-IF SSIF (AM demodulator for free).
- FM mono operation possible: Inter-Carrier or QSS.

Diversity

The following Tuners can be present (depending on the region and the set execution):

- Normal tuner without PIP.
- FM radio tuner without PIP.
- Normal tuner with PIP (main tuner with splitter).
- FM radio set with PIP (PIP tuner with splitter).

The SAW filter used, depends on the application concept (whether it is a QSS concept or an Intercarrier):

- OFWM3953M for QSS Video.
- OFWK9656M for QSS Audio.
- OFWM1971M for Intercarrier.

Pin Assignments and Functionality

Pin assignment of the Tuner:

Table: Pinning Tuner

Pin	Pin Description	DC Voltages
1	RF-AGC	4V for Maximum Gain < 4V for Strong Signal Condition
2	FM Radio Input or N.C	-
3	NC (Address Pin)	-
4	SCL	0 to 3.3 V_dc
5	SDA	0 to 3.3 V_dc
6/7	Supply Voltage	5 V_dc +/- 0.25 V
8	N.C	-
9	Tuning Supply Voltage	30 to 35 V_dc
10	FM Radio IF Output/Ground	-
11	TV IF Output	-

Pin assignment of the several SAW filters (depends on region/execution):

Table: Pinning SAW filters

Pin	QSS Video (item 1002)	QSS Video (item 1003)	QSS Audio (item 1001)	Intercarrier (item 1002)
1	Input	Input	Input	Input
2	Input Ground	Input Ground	Switching Input	Input Ground
3	Ground	Ground	Ground	Ground
4	Output	Output	Output	Output
5	Output	Output	Output	Output
6	-	n.c.	-	-
7	-	n.c.	-	-
8	-	Ground	-	-
9	-	Free	-	-
10	-	Switching input	-	-

The table below shows the switching behavior of SAW filter.

Table: Switching behavior SAW filter

	Condition	

	High	Low
System	M	BG/DK/I/L

Note: The logic level is measured at the base of transistor 7001.

Option Settings

The option settings for the Tuner type can be found in Option setting 1 of the SAM mode. The Option settings for Option 1 are as follows:

- Option Byte 1
  - Bit 7: OP_PHILIPS_TUNER
  - Bit 6: OP_FM_RADIO
  - Bit 5: OP_LNA
  - Bit 4: OP_ATS
  - Bit 3: OP_ACI
  - Bit 2: OP_UK_PNP
  - Bit 1: OP_VIRGIN_MODE
  - Bit 0: OP_CHINA

For more details on the option settings, please refer to the chapter 8 “Alignments”.

Source Select

For this chassis, the audio/video source selection is controlled via the Hercules.
The Audio/Video Source Select is one of the more complex functions due to its diversity and complex switching. The Audio/Video Source Select comprises of the following components:

- The Hercules itself for Mono Audio and Video Source Selection.
- The HEF switch for Stereo Audio as well as Video Selection.

Options

The option settings for the Source Selection can be found in Option settings of the SAM mode. The Option settings for Option 5 are as follows:

- Option Byte 5
  - Bit 7: AV1
  - Bit 6: AV2
  - Bit 5: AV3
  - Bit 4: CVI
  - Bit 3: SVHS2
  - Bit 2: SVHS3
  - Bit 1: HOTEL MODE
  - Bit 0:

For more detail on the option settings, please refer to the chapter 8 “Alignments”.

Diversity

The basic diversity of the Audio/Video Source Select is between the Mono and the Stereo sets and the number of Cinch/SCART's as specified in the product specification. The table below shows the Audio/Video Source Select diversity for all regions:

Table: AV Source Select diversity

Pin	Symbol	Remark
51	R/Pr IN3	AV1 (CVI)
50	G/Y IN3	
49	B/Pb IN3	
52	INSSW3	
74	CVBS2/Y2	
95	AUDIO IN5 L	
94	AUDIO IN5 R	
73	AUDIO IN3 L	AV2 (SVHS)
72	AUDIO IN3 R	
71	CVBS3/Y3	
70	C2/C3	
80	AUDIO IN4 L	Side (SHVS)
79	AUDIO IN4 R	
78	CVBS4/Y4	
77	C4	
81	IFVO/SVO/CVBSI	Monitor Out
67	AUD OUT HP L	
66	AUD OUT HP R	
69	AUD OUT LS L (AUD OUT/AM OUT)	HP/ LS Out
68	AUD OUT LS R	
59	V IN (R/Pr IN2/CX)	Interface
58	U IN (B/Pb IN2)	
57	Y IN (G/Y IN2/CVBS-Yx)	
54	U OUT (INSSW2)	
76	AUDIO IN2 L	

75	AUDIO IN2 R	
86	DVBO/IFVO/FMRO	N.C.
65	CVBSO/PIP	PIP application
56	Y SYNC	100 nF
55	Y OUT	100 nF
53	V OUT (SWO)	N.C.
93	AUD OUT S L	N.C.
92	AUD OUT S R	N.C.

Table: SCART Source Select diversity

Pin	Symbol	Remark
51	R/Pr IN3	SCART 1
50	G/Y IN3	
49	B/Pb IN3	
52	INSSW3	
74	CVBS2/Y2	
86	DVBO/IFVO/FMRO	
95	AUDIO IN5 L	
94	AUDIO IN5 R	
93	AUD OUT S L	
92	AUD OUT S R	
71	CVBS3/Y3	SCART 2
70	C2/C3	
81	IFVO/SVO/CVBSI	
73	AUDIO IN3 L	
72	AUDIO IN3 R	
67	AUD OUT HP L	
66	AUD OUT HP R	
80	AUDIO IN4 L	Side I/O
79	AUDIO IN4 R	
78	CVBS4/Y4	
77	C4	
69	AUD OUT LS L (AUD OUT/AM OUT)	LS/ HP/ MON OUT
68	AUD OUT LS R	
59	V IN (R/Pr IN2/CX)	Interface
58	U IN (B/Pb IN2)	
57	Y IN (G/Y IN2/CVBS-Yx)	

54	U OUT(INSSW2)	
76	AUDIO IN2 L	
75	AUDIO IN2 R	
65	CVBSO/PIP	for PIP
56	YSYNC	100 nF
55	YOUT	100 nF
53	VOUT(SWO)	N.C.

Audio Source Selection

The signals coming out of the DEMDEC (internal demodulator/decoder block of the Hercules) are selectable and consist of the following (depending on the transmission):

- DEC L/R (Can be NICAM, FM 2CS, or BTSC Stereo).
- Mono (Refers to fallback/forced Mono in Stereo Transmission).
- SAP.

For L04, the assigned I/O with respect to the Hercules is as follows:

- SCART1 or AV1 Input assigned to **Audio In 5** .
- SCART2 or AV2 Input assigned to **Audio In 3** .
- Side AV Input assigned to **Audio In 4** .
- External Interface Input assigned **to Audio In 2** .
- SCART1 Output assigned to **SCART Output** .
- SCART2 Output (EU) or Monitor Output (LA/NA/AP) assigned to **Headphone Output** .
- Constant Level Output assigned to **Loudspeaker Output** .

Video Source Selection

Video source selection is done inside the Hercules. Therefore it provides a video switch with 3 external CVBS inputs and a CVBS output. All CVBS inputs can be used as Y-input for Y/C signals. However, only 2 Y/C sources can be selected because the circuit has 2 chroma inputs.
All input signals are converted to YUV, and looped through an external interface. This to enable picture improvement features (like LTI/CTI) or PIP.

Video Processing

The Video Processor is basically the Hercules and the TDA9178 (CTI/LTI). Video processing is done in these two chips such as the Brightness Control, Contrast Control and so on.

Some features:

- Full YUV-loop interface (alternative functions: DVD, RGB or Y/C).
- Internal OSD insertion (not Saturation or Contrast controlled).
- Double window implementation.
- Linear / non linear scaling for 16:9 sets.

- Tint (hue) on UV signals (including DVD).
- Peaking, Coring, Black \ Blue \ White-stretch.
- Transfer-Ratio and Scavem (also on TXT).

Features

The features included in the Hercules are as follows:

- Brightness Control.
- Contrast Control.
- Saturation Control.
- Sharpness Control.
- Peak White Limiter.
- Beam Current Limiter.
- Black Stretch (Contrast Plus).

For sets with the TDA9178, there are two extra features:

- Luminance Transient Improvement (LTI).
- Color Transient Improvement (CTI).

Block Diagram

Following diagram is the block diagram of the video processing part:

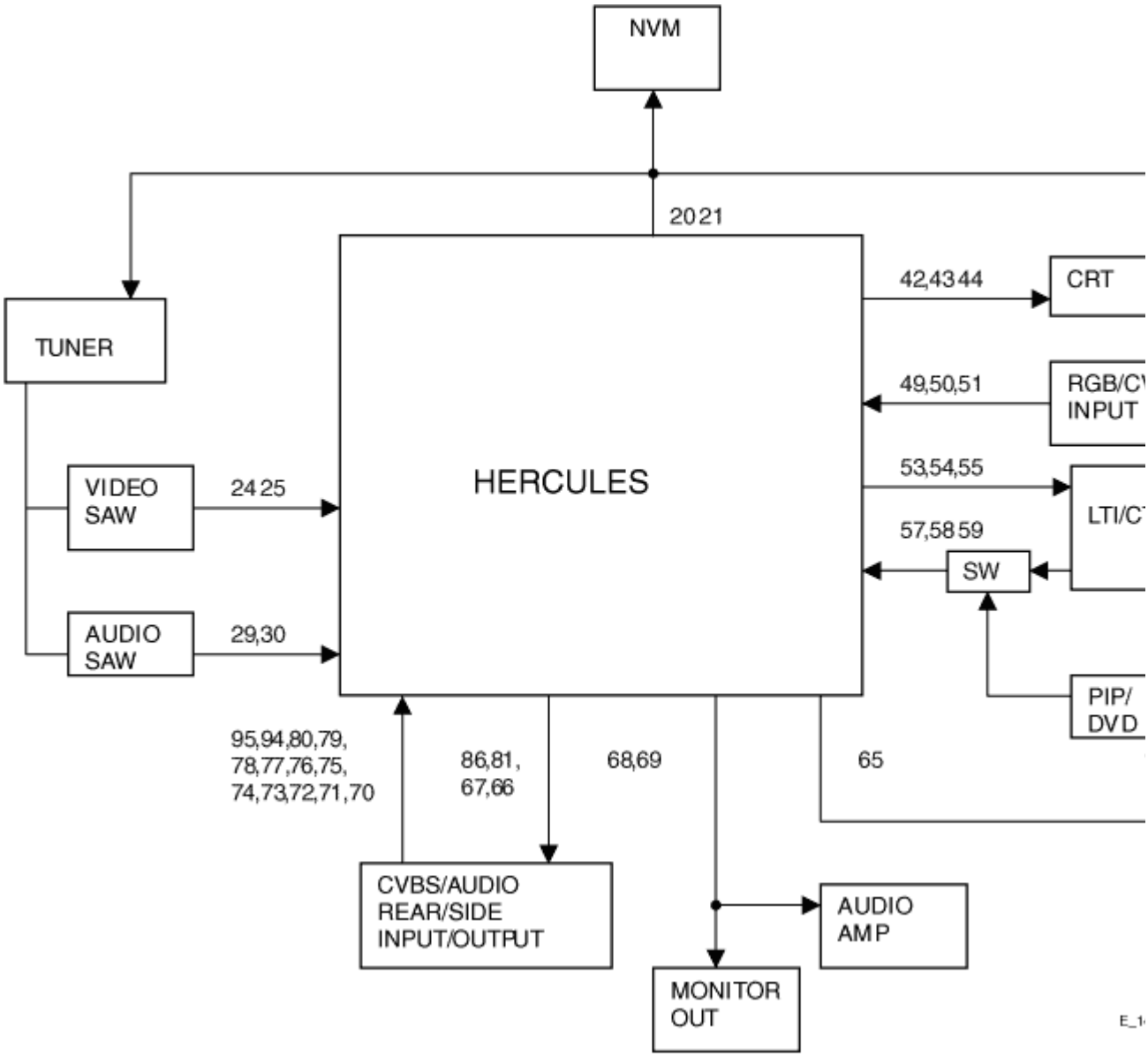


Figure: Video processing block diagram

LTI/CTI

The TDA9178 is an I2C-bus controlled IC (INCREDIBLE chip) with YUV interface. This IC can do mainly histogram processing, color transient improvement (CTI) and line transient improvement (LTI).

- Luminance Vector Processing involves histogram function, which provides scene dependent contrast improvement, adaptive black and white point stretching.
- Color Vector Processing involves skin tone correction, green enhancement and blue stretch.
- Spectral Processor involves step improvement processing, contour processing, smart sharpness control, color dependant sharpness and Color Transient Improvement.
- Noise detector, feature mode detector and cue flash functions.
- Demonstration mode shows all the improvement features in one picture.

Table: Pinning overview TDA9178

Pin	Symbol	Description
1	SC	Sandcastle input pin
2	n.c.	Not connected pin
3	ADEXT1	External AD-conversion #1 input pin
4	ADEXT2	External AD-conversion #2 input pin
5	ADEXT3	External AD-conversion #3 input pin
6	Y in	Luminance input pin
7	ADR	Address selection input pin
8	U in	-(B-Y) signal input pin
9	V in	-(R-Y) signal input pin
10	TP	Testpin, connected to ground
11	SCL	I2C-bus: clock input pin
12	n.c.	Not connected pin
13	n.c.	Not connected pin
14	SDA	I2C-bus: data input pin
15	DECDIG	Decoupling digital supply
16	V out	-(R-Y) signal output pin
17	U out	-(B-Y) signal output pin
18	V ee	Ground pin
19	Y out	Luminance output pin
20	V cc	Supply-voltage pin
21	S out	Luminance output for SCAVEM
22	CF	Cue-flash output pin
23	n.c.	Not connected pin
24	n.c.	Not connected pin

Options

The option settings allow for process of the video as per set specification. The option settings can be found in “Option 2” and “Option 6” in the SAM mode. The option settings are as follows:

- Option Byte 2
  - Bit 7:
  - Bit 6 :OP_GREEN_UI
  - Bit 5: OP_CHANNEL_NAMING,
  - Bit 4: OP_LTI,
  - Bit 3: OP_TILT,
  - Bit 2: OP_FINE_TUNING
  - Bit 1: OP_PIP_PHILIPS_TUNER,
  - Bit 0: OP_HUE,

- Option Byte 6
  - Bit 7: OP_PERSONAL_ZAPPING,
  - Bit 6:
  - Bit 5: OP_FMTRAP
  - Bit 4: OP_COMBFILTER
  - Bit 3: OP_ACTIVE_CONTROL
  - Bit 2: OP_VIDEO_TEXT
  - Bit 1 :OP_LIGHT_SENSOR,
  - Bit 0: OP_DUAL_TEXT

For more details on the option settings, please refer to the chapter 8 “Alignments”.

Audio Processing

The audio decoding is done entirely via the Hercules. The IF output from the Tuner is fed directly to either the Video-IF or the Sound-IF input depending on the type of concept chosen. There are mainly two types of decoder in the Hercules, an analog decoder that decodes only Mono, regardless of any standards, and a digital decoder (or DEMDEC) that can decode both Mono as well as Stereo, again regardless of any standards.

In this chassis, the analog decoder is used in two cases:

- It is used for AM Sound demodulation in the Europe SECAM LL' transmission.
- It is used for all FM demodulation in AP AV-Stereo sets.

Diversity

The diversity for the Audio decoding can be broken up into two main concepts:

- The Quasi Split Sound concept used in Europe and some AP sets.
- The Inter Carrier concept, used in NAFTA and LATAM.

The UOC-III family makes no difference anymore between QSS- and Intercarrier IF, nearly all types are software-switchable between the two SAW-filter constructions.

Simple data settings are required for the set to determine whether it is using the Inter Carrier or the QSS concept. These settings are done via the “QSS” and “FMI” bit found in SAM mode. Due to the diversity involved, the data for the 2 bits are being placed in the NVM location and it is required to write once during startup.

On top of that, it can be further broken down into various systems depending on the region. The systems or region chosen, will in turn affect the type of sound standard that is/are allowed to be decoded.

- For the case of **Europe** , the standard consists of BG/DK/I/LL' for a Multi-System set. There are also versions of Eastern Europe and Western Europe set and the standard for decoding will be BG/DK and I/DK respectively. FM Radio is a feature diversity for the Europe sets. The same version can have either FM Radio or not, independent of the system (e.g. sets with BG/DK/I/LL' can have or not have FM radio).
- For the case of **NAFTA** and **LATAM** , there is only one transmission standard, which is the M standard. The diversity then will be based on whether it has a dBx noise reduction or a Non-

dBx (no dBx noise reduction).
- For the case of **AP** , the standard consists of BG/DK/I/M for a Multi-System set. The diversity here will then depends on the region. AP China can have a Multi-System and I/DK version. For India, it might only be BG standard.

Functionality

The features available in the Hercules are as follows:

- Treble and Bass Control.
- Surround Sound Effect that includes:
  - Incredible Stereo.
  - Incredible Mono.
  - 3D Sound (not for AV Stereo).
  - TruSurround (not for AV Stereo).
  - Virtual Dolby Surround, VDS422 (not for AV Stereo).
  - Virtual Dolby Surround, VDS423 (not for AV Stereo).
  - Dolby Pro-Logic (not for AV Stereo).
- Bass Feature that includes:
  - Dynamic Ultra-Bass.
  - Dynamic Bass Enhancement.
  - BBE (not for AV Stereo).
- Auto-Volume Leveler.
- 5 Band Equalizer.
- Loudness Control.

All the features stated are available for the Full Stereo versions and limited features for the AV Stereo

Audio Amplifier

The audio amplifier part is very straightforward. It uses the integrated power amplifier TDA2616Q, and delivers a maximum output of 2 x 10 W_rms.
The maximum operating condition for this amplifier is 21 V unloaded. Normal operating supply is from 7.5 V to 16 V.
Muting is done via the VOLUME_MUTE line connected to pin 2 of the amplifier-IC and coming from the UOC.

The following table shows pin functionality of the Audio Amplifier:

Table: Pinning overview TDA2616

Pin	Pin Name	Normal Operation
1	Input Left	Input AC signal
2	Mute	16 V_dc
3	Ground	0 V
4	Output L Channel	AC waveform
5	Supply Voltage (negative)	-16 V_dc
6	Output R Channel	AC waveform

7	Supply Voltage (positive)	+ 16 V_dc
8	Inverting inputs L and R	0 V
9	Input Right	Input AC signal

Abbreviation list

Abbreviation	Description
2CS	2 Carrier (or Channel) Stereo
ACI	Automatic Channel Installation: algorithm that installs TV sets directly from cable network by means of a predefined TXT page
ADC	Analogue to Digital Converter
AFC	Automatic Frequency Control: control signal used to tune to the correct frequency
AFT	Automatic Fine Tuning
AGC	Automatic Gain Control: algorithm that controls the video input of the feature box
AM	Amplitude Modulation
AP	Asia Pacific region
AR	Aspect Ratio: 4 by 3 or 16 by 9
ATS	Automatic Tuning System
AV	External Audio Video
AVL	Automatic Volume Leveler
BCL	Beam Current Limitation
B/G	Monochrome TV system. Sound carrier distance is 5.5 MHz
BTSC	Broadcast Television Standard Committee. Multiplex FM stereo sound system, originating from the USA and used e.g. in LATAM and AP-NTSC countries
CC	Closed Caption
CCC	Continuous Cathode Calibration
ComPair	Computer aided rePair
CRT	Cathode Ray Tube or picture tube
CSM	Customer Service Mode
CTI	Color Transient Improvement: manipulates steepness of chroma transients
CVBS	Composite Video Blanking and Synchronization
CVI	

	Component Video Input
DAC	Digital to Analogue Converter
DBX	Dynamic Bass Expander or noise reduction system in BTSC
D/K	Monochrome TV system. Sound carrier distance is 6.5 MHz
DFU	Direction For Use: description for the end user
DNR	Dynamic Noise Reduction
DSP	Digital Signal Processing
DST	Dealer Service Tool: special remote control designed for dealers to enter e.g. service mode
DVD	Digital Versatile Disc
EEPROM	Electrically Erasable and Programmable Read Only Memory
EHT	Extra High Tension
EHT-INFO	Extra High Tension information
EPG	Electronic Programming Guide
EU	Europe
EW	East West, related to horizontal deflection of the set
EXT	External (source), entering the set via SCART or Cinch
FBL	Fast Blanking: DC signal accompanying RGB signals
FILAMENT	Filament of CRT
FM	Field Memory or Frequency Modulation
H	Horizontal sync signal
HP	Headphone
I	Monochrome TV system. Sound carrier distance is 6.0 MHz
I2C	Integrated IC bus
IF	Intermediate Frequency
IIC	Integrated IC bus
ITV	Institutional TV
LATAM	Latin American countries like Brazil, Argentina, etc.
LED	Light Emitting Diode
L/L'	Monochrome TV system. Sound carrier distance is 6.5 MHz. L' is Band I, L is all bands except for Band I
LS	Large Screen or Loudspeaker
M/N	Monochrome TV system. Sound carrier distance is 4.5 MHz
NC	Not Connected
NICAM	Near Instantaneous Compounded Audio Multiplexing. This is a digital sound system, mainly used in Europe.

NTSC	National Television Standard Committee. Color system mainly used in North America and Japan. Color carrier NTSC M/N = 3.579545 MHz, NTSC 4.43 = 4.433619 MHz (this is a VCR norm, it is not transmitted off-air)
NVM	Non Volatile Memory: IC containing TV related data e.g. alignments
OB	Option Bit
OC	Open Circuit
OP	Option Byte
OSD	On Screen Display
PAL	Phase Alternating Line. Color system mainly used in West Europe (color carrier = 4.433619 MHz) and South America (color carrier PAL M = 3.575612 MHz and PAL N = 3.582056 MHz)
PCB	Printed Circuit board
PLL	Phase Locked Loop. Used for e.g. FST tuning systems. The customer can give directly the desired frequency
POR	Power-On Reset
PTP	Picture Tube Panel (or CRT-panel)
RAM	Random Access Memory
RC	Remote Control handset
RGB	Red, Green, and Blue video signals
ROM	Read Only Memory
SDAM	Service Default / Alignment Mode
SAP	Second Audio Program
SC	Sandcastle: pulse derived from sync signals
S/C	Short Circuit
SCL	Serial Clock
SDA	Serial Data
SECAM	SEequence Couleur Avec Memoire. Color system mainly used in France and East Europe. Color carriers = 4.406250 MHz and 4.250000 MHz
SIF	Sound Intermediate Frequency
SS	Small Screen
STBY	Standby
SVHS	Super Video Home System
SW	Software
THD	Total Harmonic Distortion
TXT	

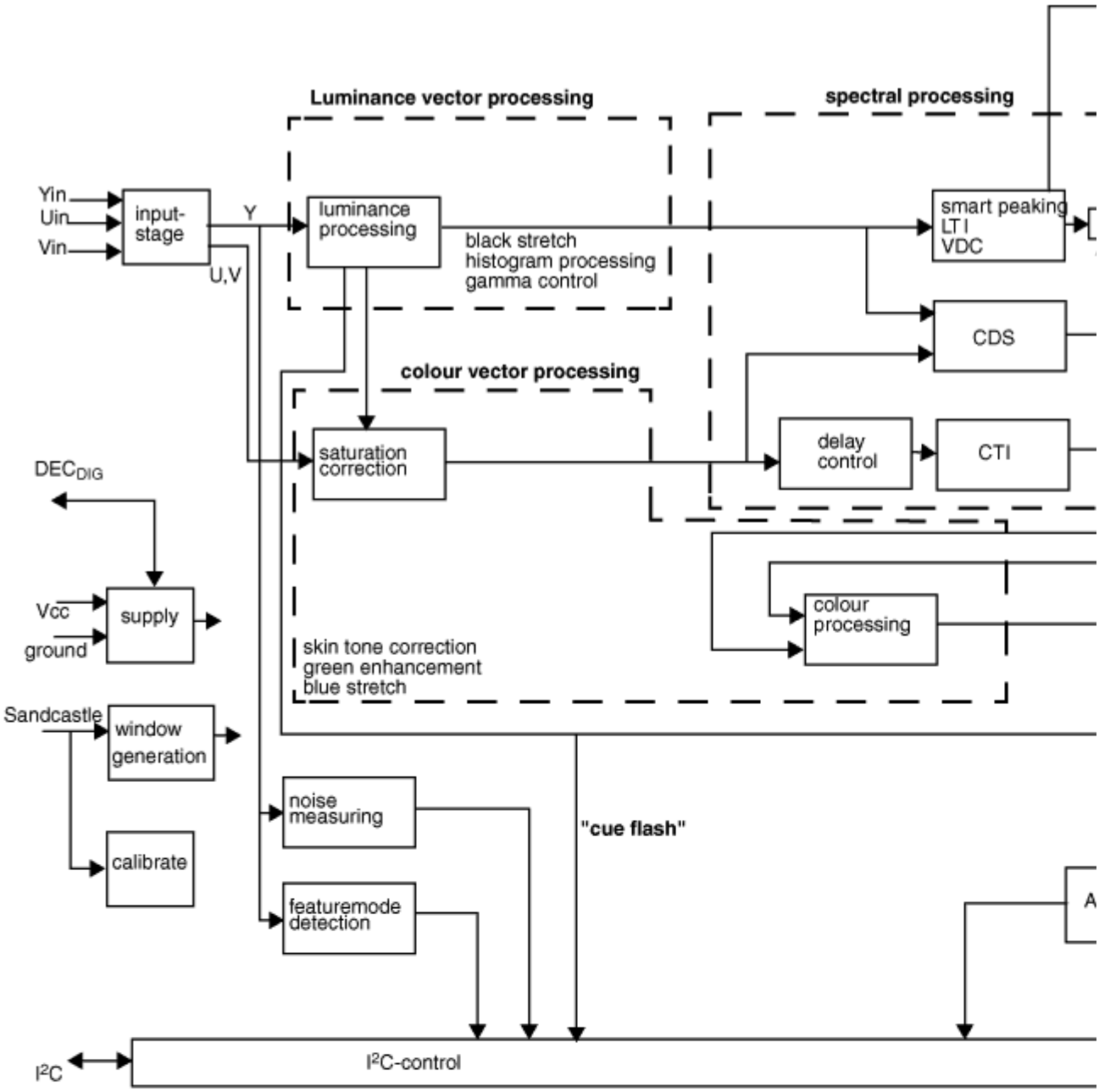
	Teletext
uP	Microprocessor
UOC	Ultimate One Chip
V	Vertical sync signal
V_BAT	Main supply voltage for the deflection stage (mostly 141 V)
V-chip	Violence Chip
VCR	Video Cassette Recorder
WYSIWYR	What You See Is What You Record: record selection that follows main picture and sound
XTAL	Quartz crystal
YC	Luminance (Y) and Chrominance (C) signal

IC Data Sheets

This section shows the internal block diagrams and pin layouts of ICs that are drawn as 'black boxes' in the electrical diagrams (with the exception of 'memory' and 'logic' ICs).

Diagram H, TDA9178 (IC7610)

BLOCK DIAGRAM



PIN CONFIGURATION

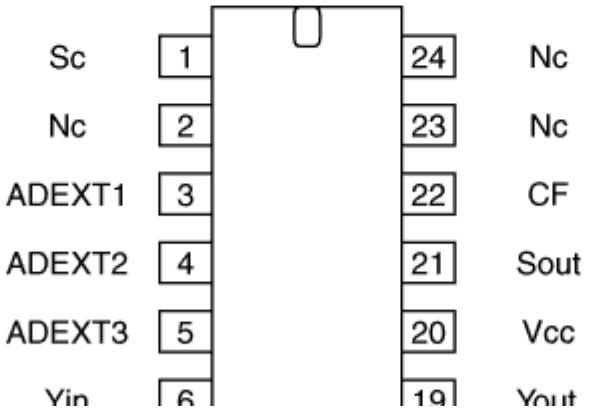


Figure: Internal Block Diagram and Pin Configuration