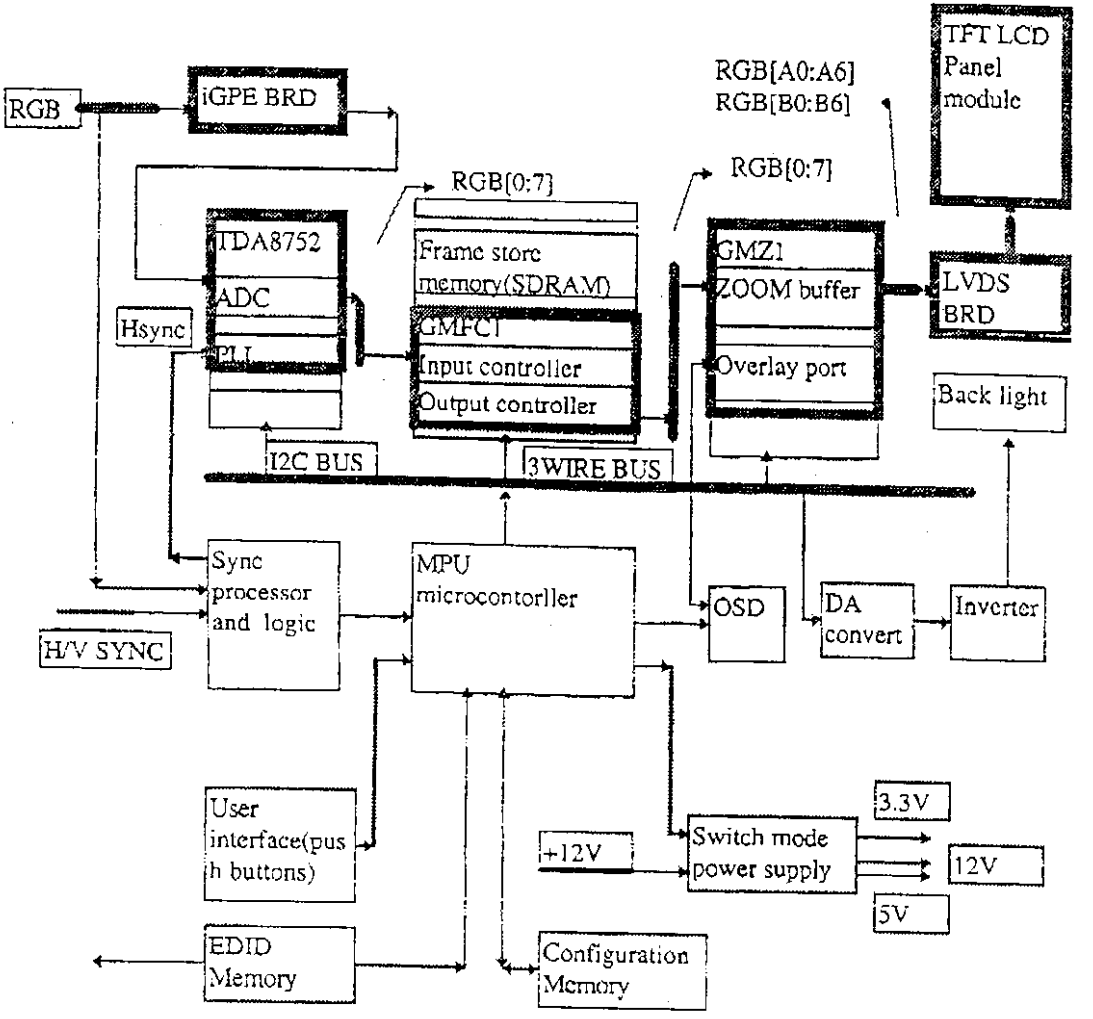
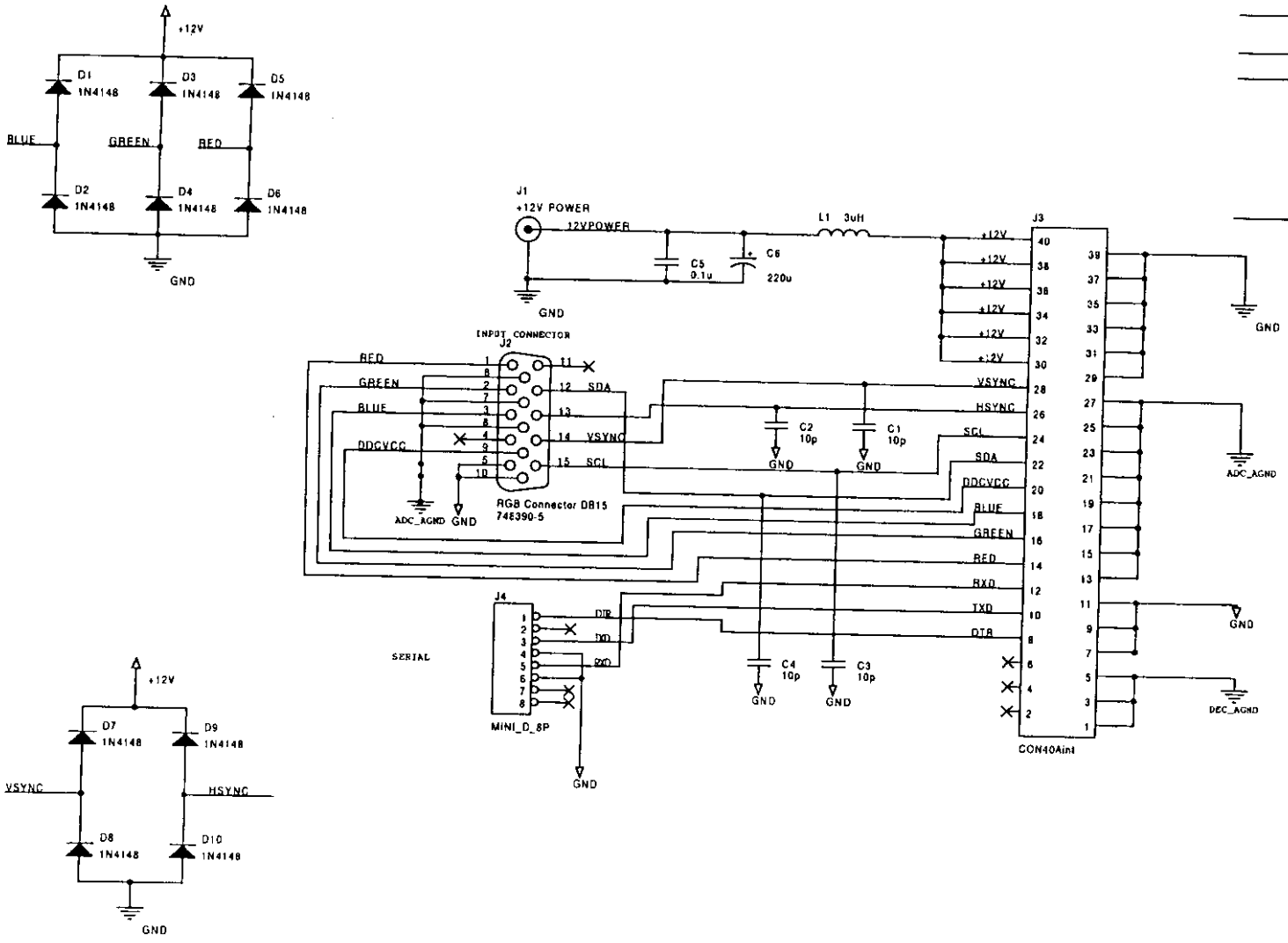
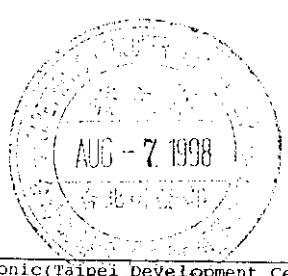
.Block diagram





Revision History

Rev	Description
0.0	original
1.0	updated for ESD and EMI 1. add L1, C5 for EMI 2. add D1 to D8 for ESD
2.0	add C6 for 12V.

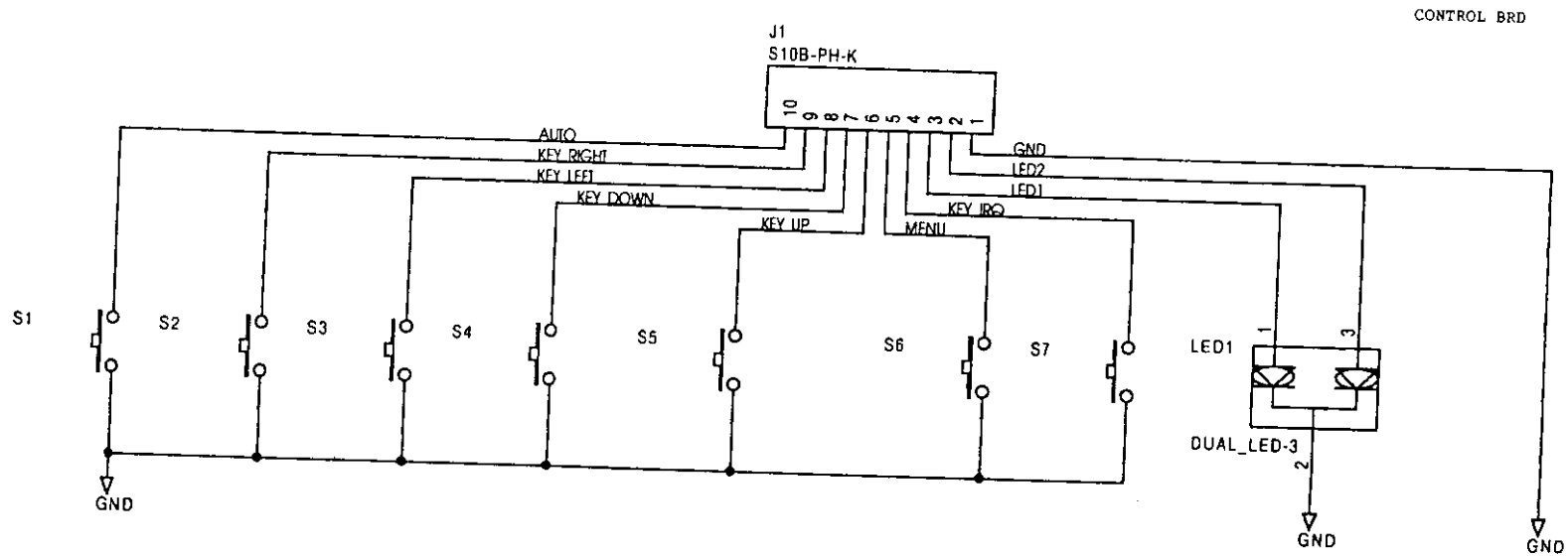


Capetronic(Taipei Development Center)

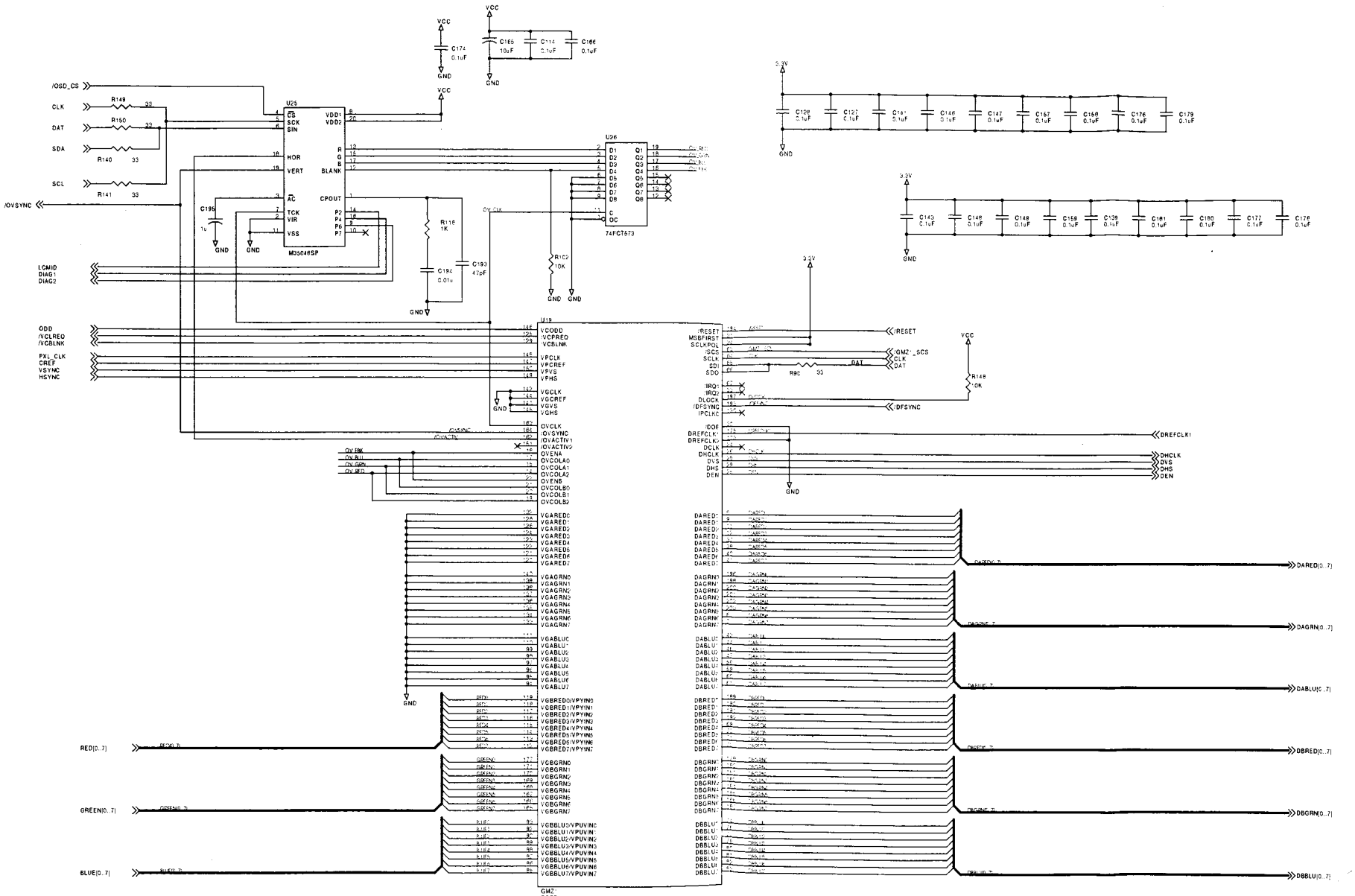
Title: CPD-L173

Size: B | Document Number: CONNECTOR BRD | Rev: 2

Date: Monday, July 20, 1998 | Sheet 1 of 1

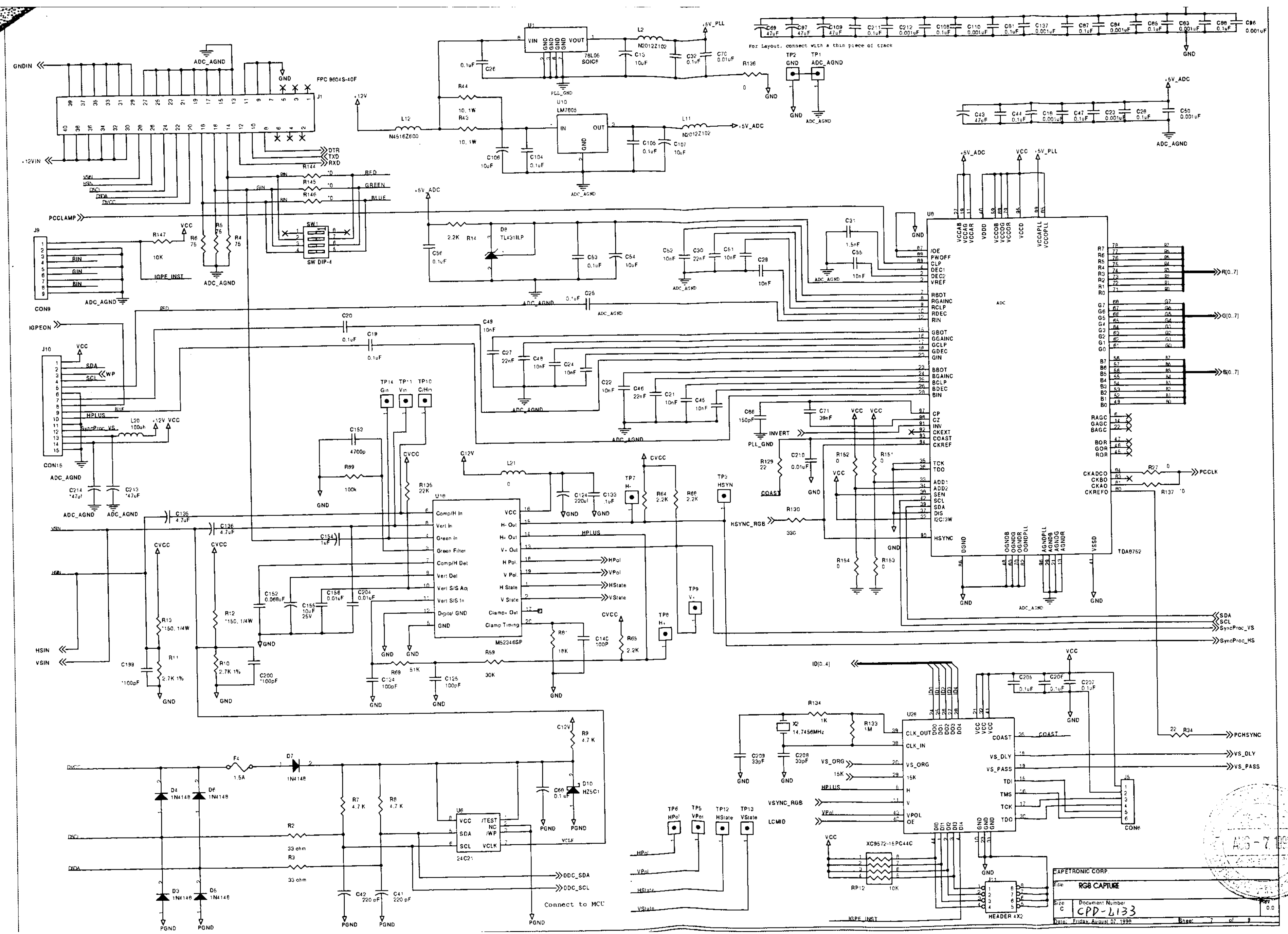


CAPETRONIC CORP.		
Title: CONTROL PANEL		
Size: A	Document Number: CPD-L133	Rev: 1.0
Date: Thursday, February 12, 1998	Sheet 1 of 1	

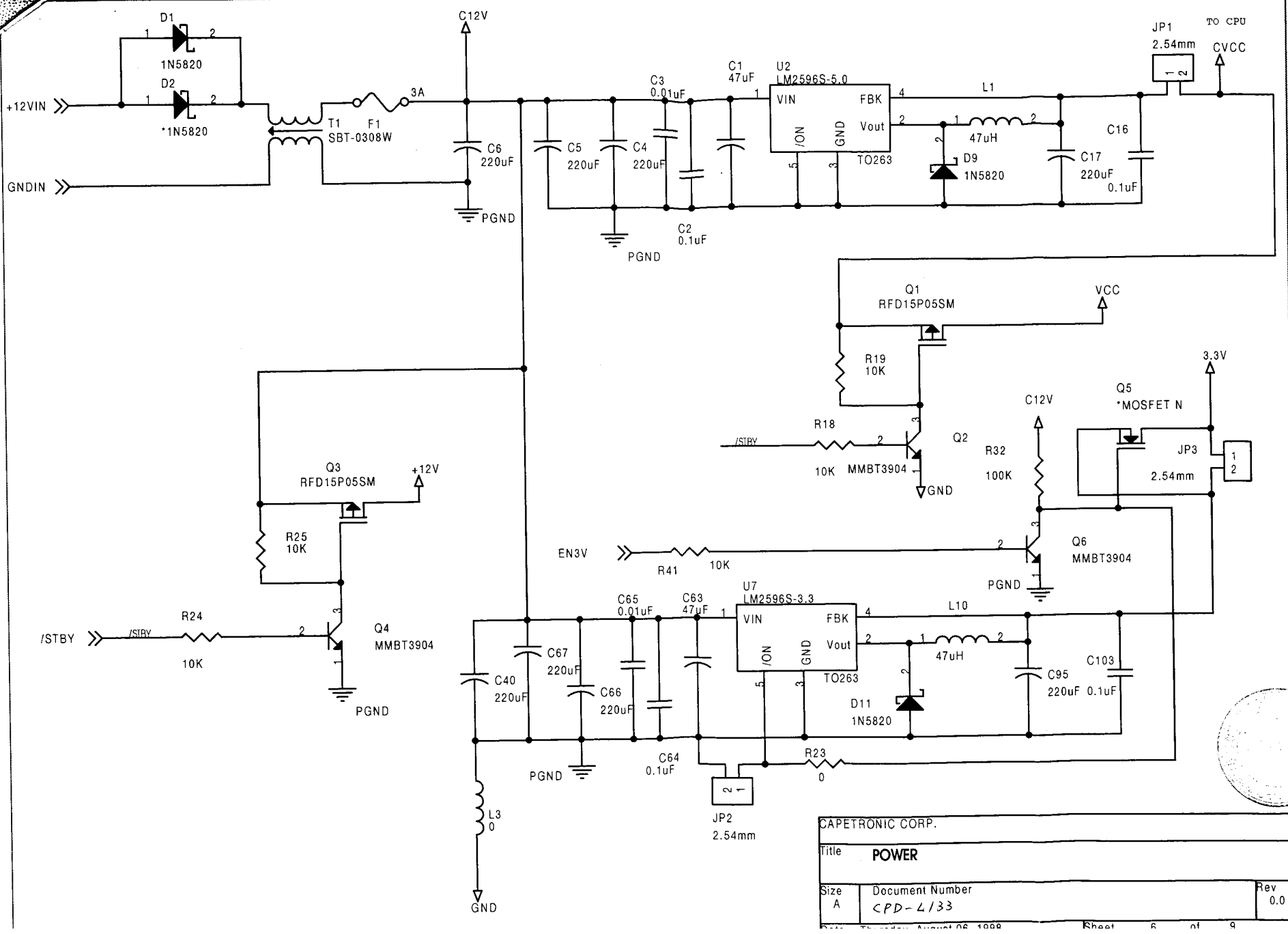


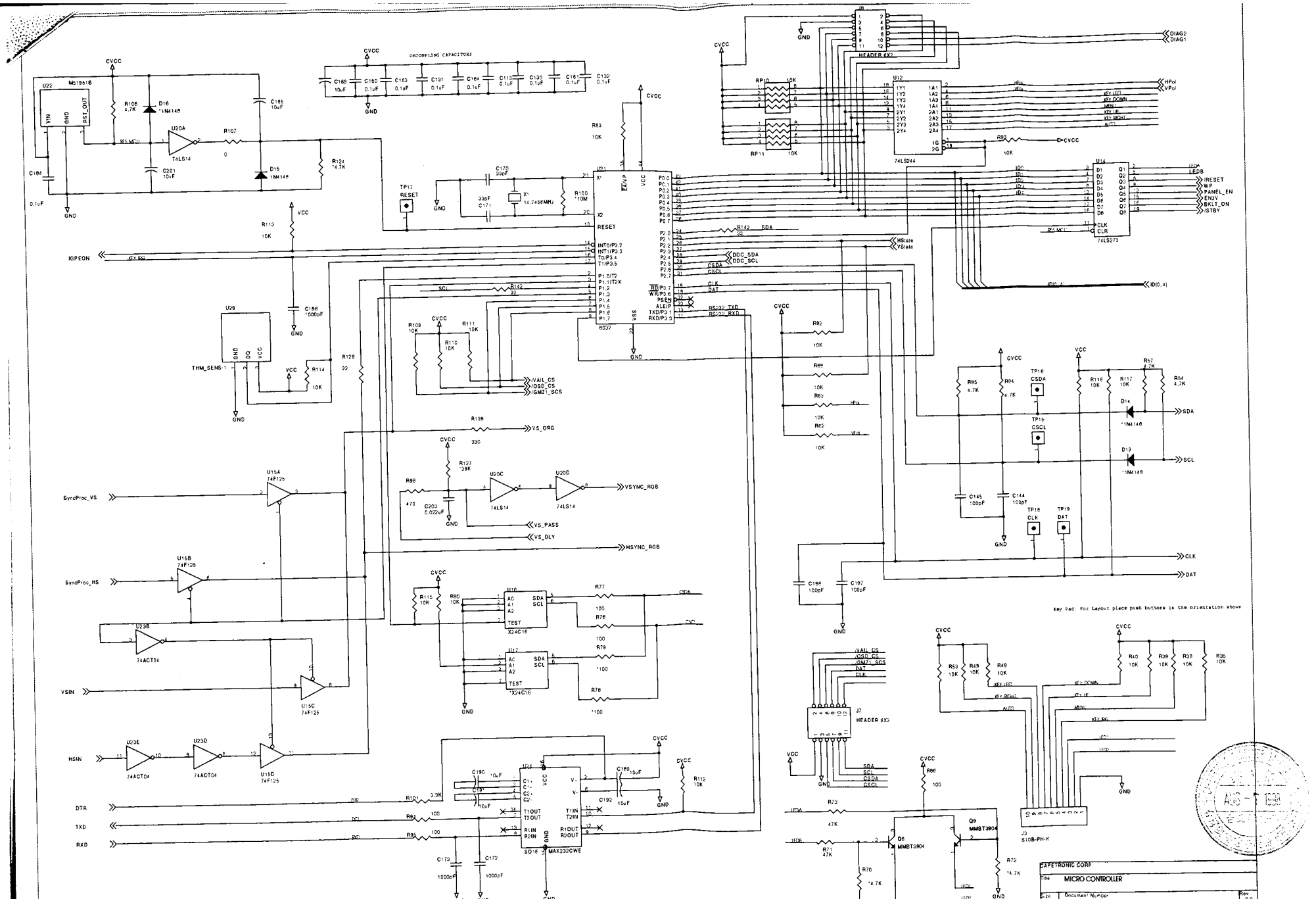
CAPETRONIC CORP.

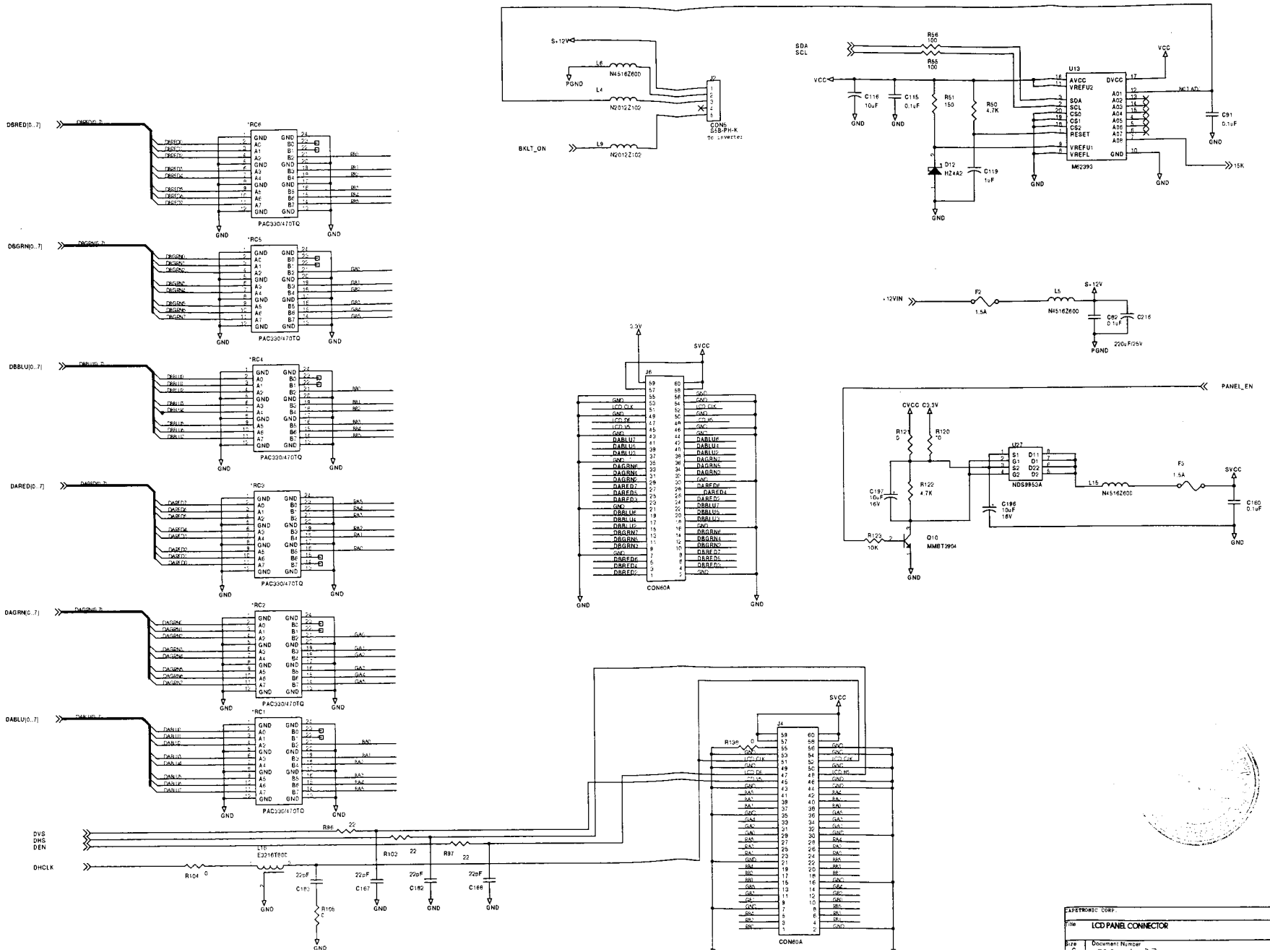
Title	ZOOM ENGINE	
Size C	Document Number CPD-L133	Rev 0.0
Date: Thursday, August 06, 1998	Sheet 8 of 8	



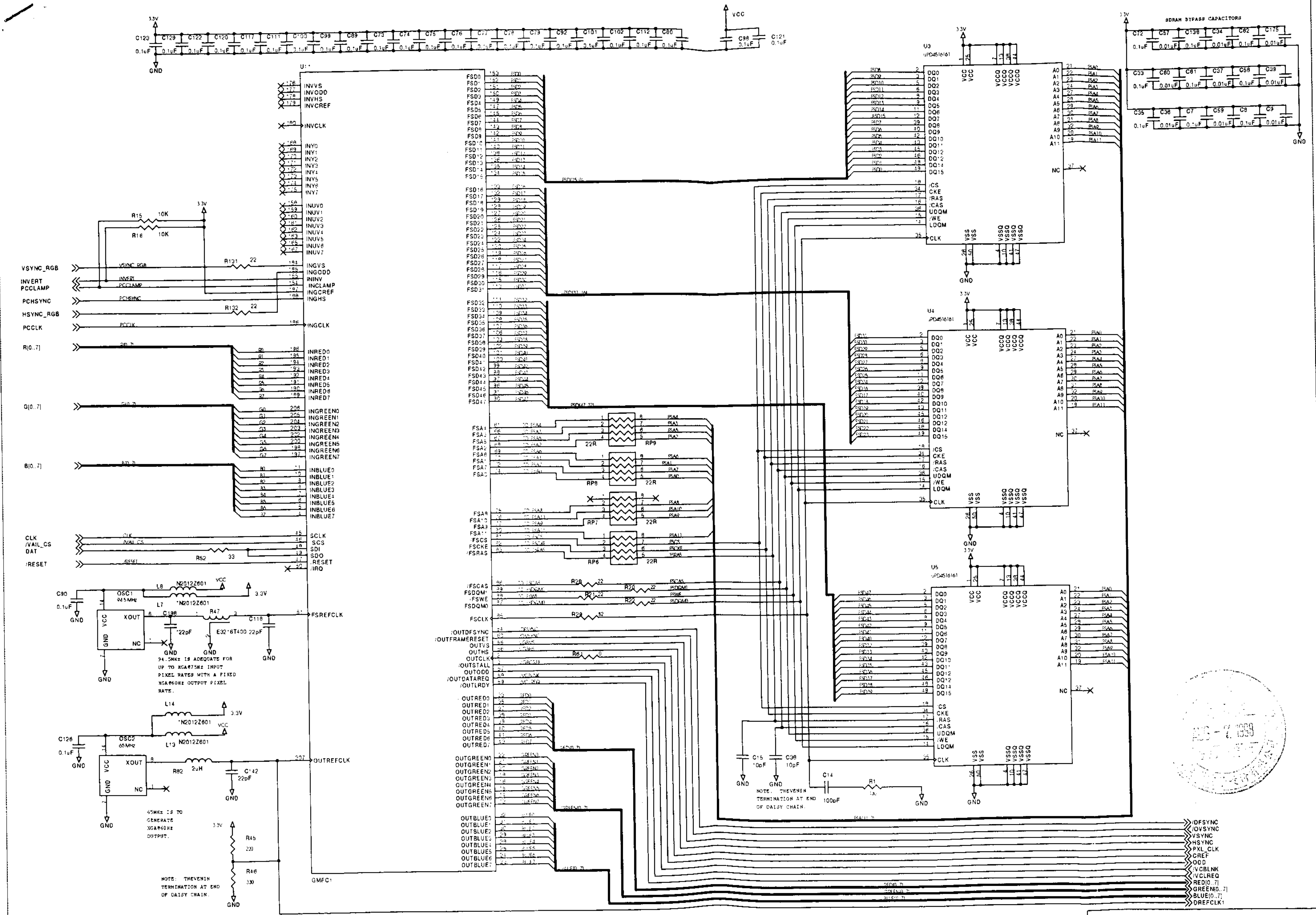
CAPETRONIC CORP.
Title RGB CAPTURE
Size C
Document Number CPD-2133
Rev 0.0
Date: Friday, August 07, 1998
Sheet 7 of 9
For Layout, connect with a thin piece of track
Connect to MCU
FPC 9604S-40F
J1
J9
J10
CON9
CON15
CON6
SW1
SW DIP-4
U1 78L05 SOIC8
U10 LM7805
U8 TDA8752
U18 M52346SP
U6 24C21
U26 XC9572-15PC44C
J1 HEADER 4X2
GNDIN
+12VIN
PCCLAMP
IGPEON
IGPE_INST
DTR
TXD
RXD
RED
GREEN
BLUE
HSIN
VSIN
DVCC
DSCL
DSDA
ADC_AGND
PLL_GND
PGND
+5V_PLL
+5V_ADC
CVCC
C12V
R[0..7]
G[0..7]
B[0..7]
PCCLK
SDA
SCL
SyncProc_VS
SyncProc_HS
PCHSYNC
VS_DLY
VS_PASS
HPol
VPol
HState
VState
HPLUS
HSYNC_RGB
VSYNC_RGB
LCMID
COAST
INVERT
ID[0..4]
DDC_SDA
DDC_SCL


D1
1N5820
D2
*1N5820
+12VIN
GNDIN
T1
F1
SBT-0308W
3A
C12V
C6
220uF
PGND
C5
220uF
C4
220uF
C3
0.01uF
C2
0.1uF
C1
47uF
U2
LM2596S-5.0
VIN
FBK
/ON
GND
Vout
TO263
L1
47uH
D9
1N5820
C16
C17
220uF
0.1uF
JP1
2.54mm
TO CPU
CVCC
Q1
RFD15P05SM
VCC
R19
10K
R18
10K
/STBY
Q2
MMBT3904
GND
R32
100K
C12V
Q5
*MOSFET N
3.3V
JP3
2.54mm
Q3
RFD15P05SM
+12V
R25
10K
R24
10K
/STBY
Q4
MMBT3904
PGND
EN3V
R41
10K
Q6
MMBT3904
PGND
U7
LM2596S-3.3
VIN
FBK
/ON
GND
Vout
TO263
C65
0.01uF
C63
47uF
L10
47uH
C67
220uF
C66
220uF
C40
220uF
C64
0.1uF
D11
1N5820
C95
220uF
0.1uF
C103
R23
0
JP2
2.54mm
L3
0
GND
CAPETRONIC CORP.
Title
POWER
Size
A
Document Number
CPD-4133
Rev
0.0
Sheet 6 of 9


DECOUPLING CAPACITORS
HEADER 6X2
Key Pad: For Layout place push buttons in the orientation shown
EAPETRONIC CORP
MICRO CONTROLLER



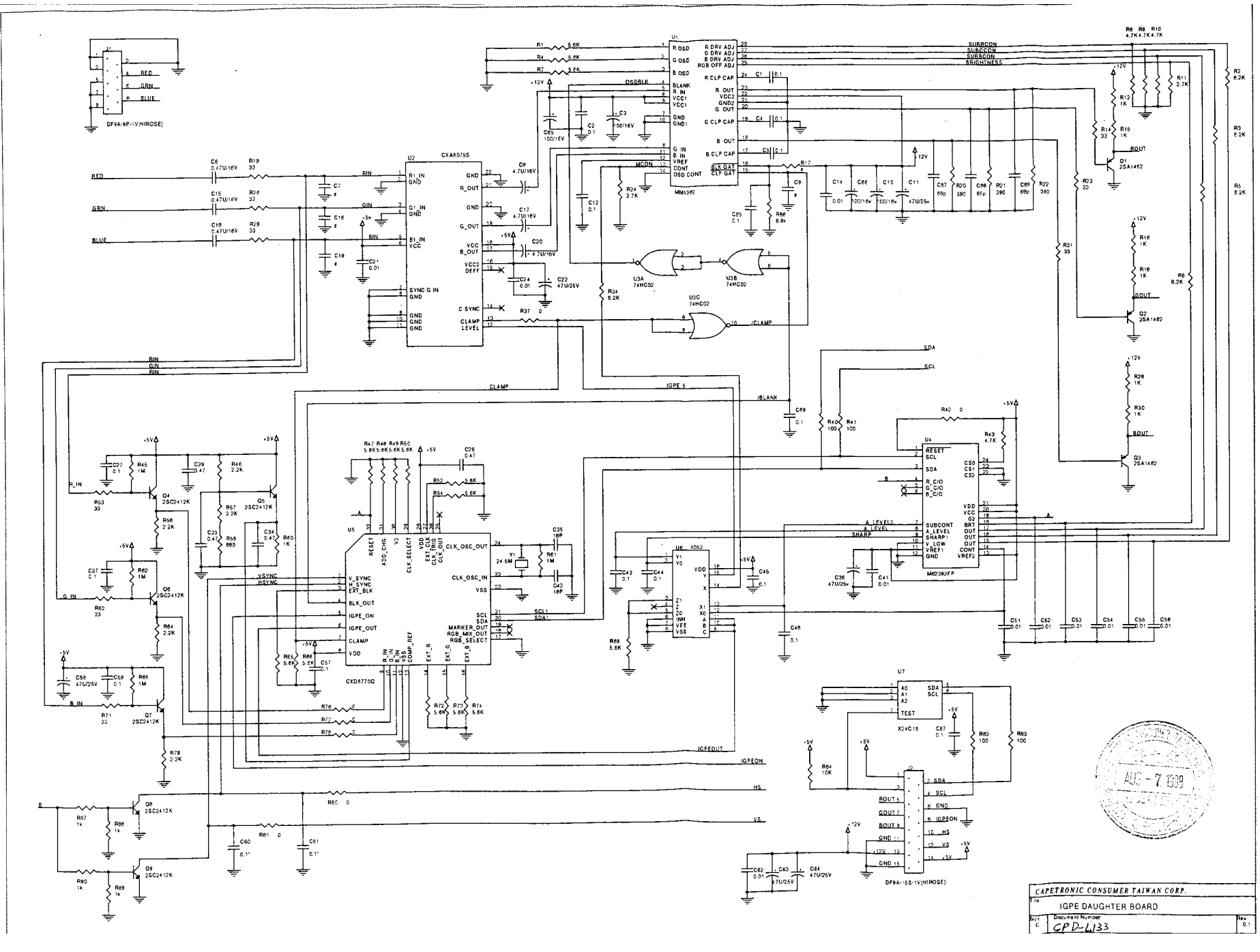
CAPETRONIC CORP.		
Title	LCD PANEL CONNECTOR	
Size	Document Number	Rev



CAPETRONIC CORP.

Title GMFC1 FRAME CONVERTER

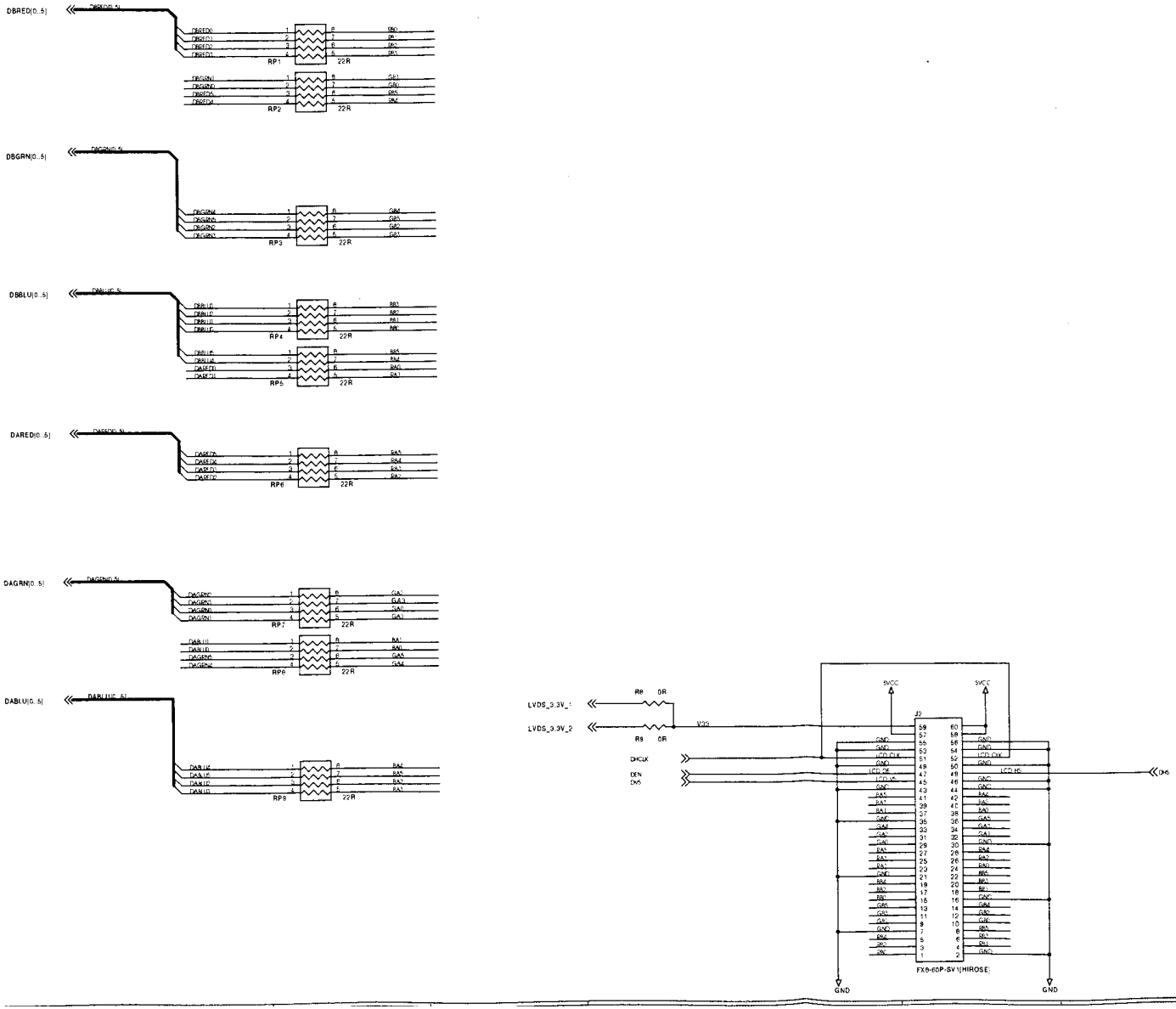
Size C | Document Number | Rev 0.0



CAPETRONIC CONSUMER TAIWAN CORP.

Title: IGPE DAUGHTER BOARD

Size: C | Document Number: CPD-L133 | Rev: 0.1

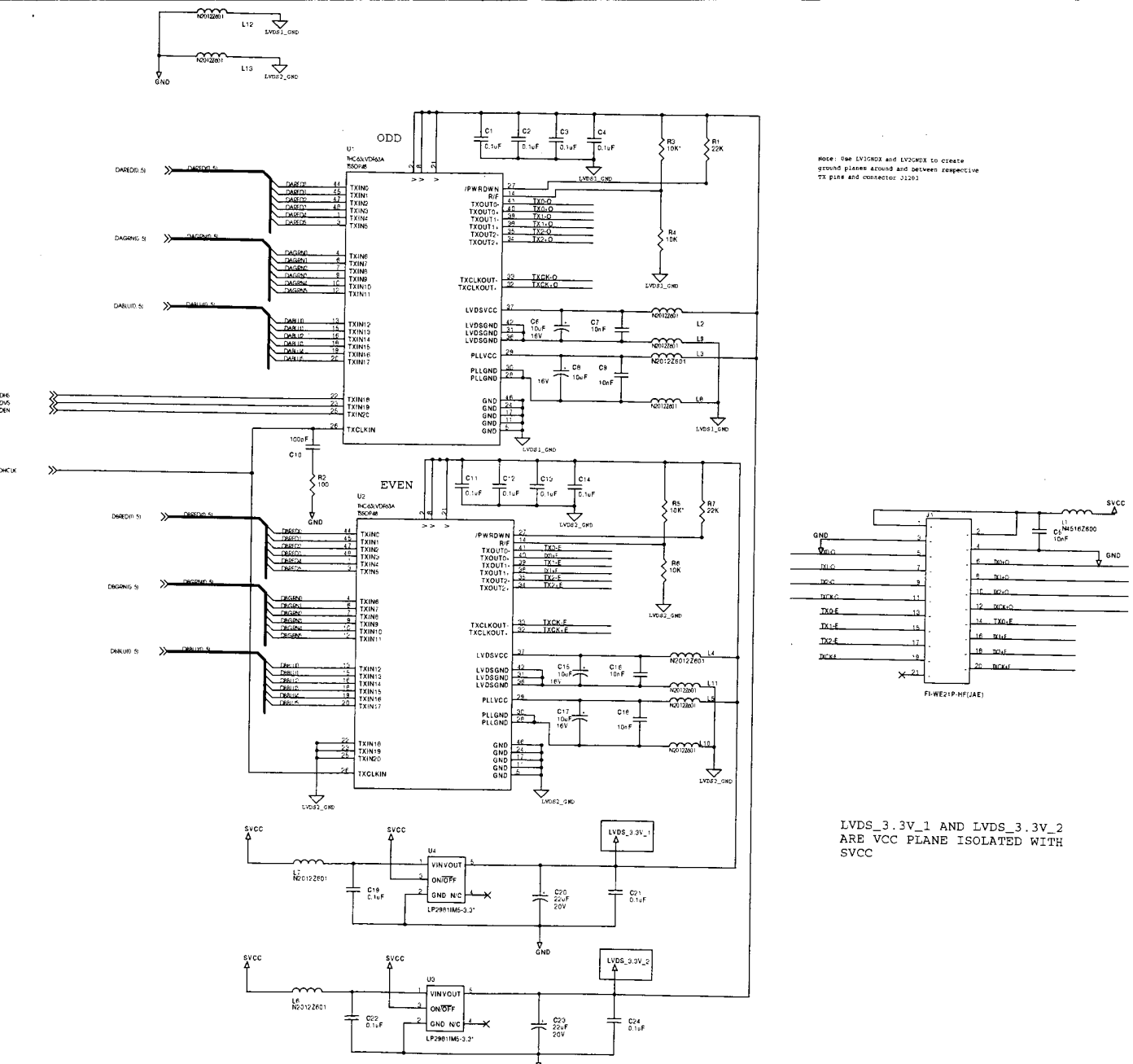


CAPETRONIC CONSUMER TAIWAN CORP.

Title: LVDS DAUGHTER CONNECTOR

Size: C | Document Number: CPD-4133 | Rev:

Date: Thursday, August 06, 1998 | Sheet 2 of 2


ODD
EVEN
Note: Use LV1GNDX and LV2GNDX to create ground planes around and between respective TX pins and connector J1201
LVDS_3.3V_1 AND LVDS_3.3V_2 ARE VCC PLANE ISOLATED WITH SVCC
FI-WE21P-HF(JAE)
AUG - 7 1998
CAPETRONIC CONSUMER TAIWAN CORP.