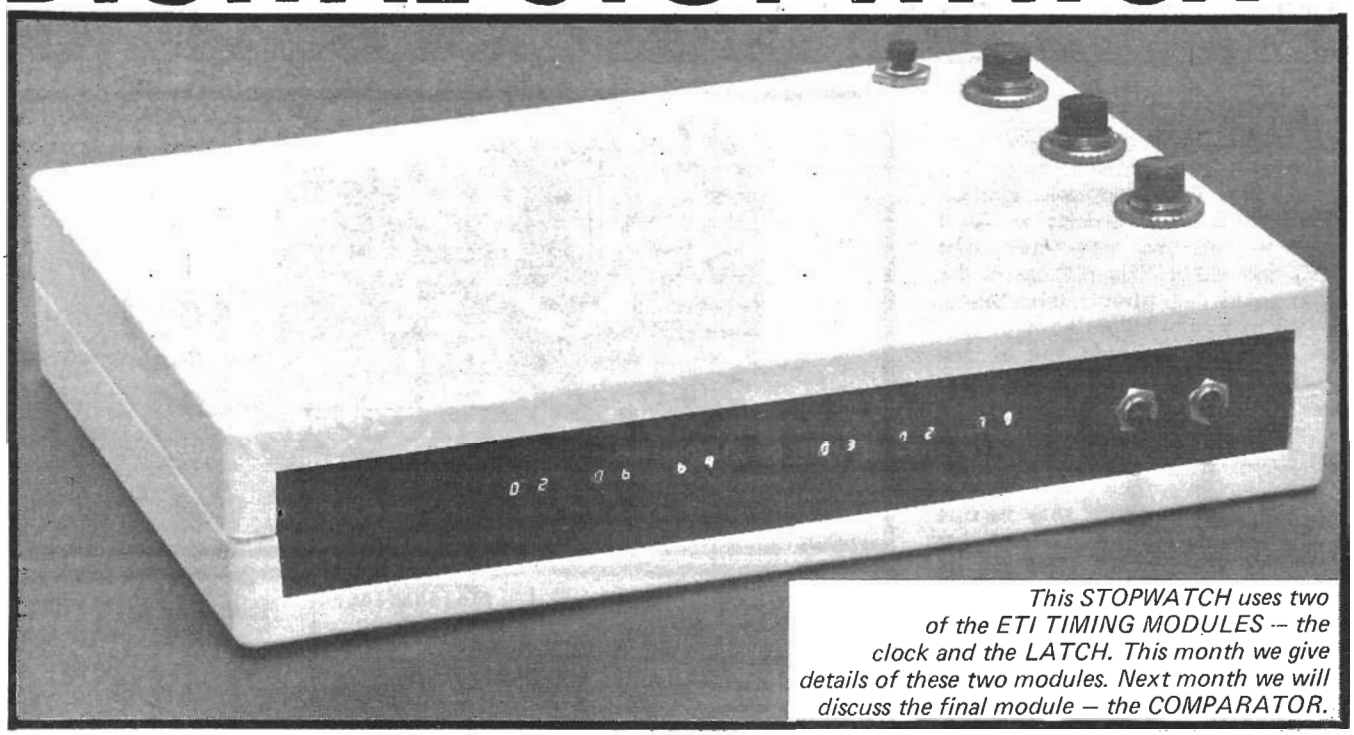
Use ETI TIMING MODULES to build this

DIGITAL STOPWATCH



This STOPWATCH uses two of the ETI TIMING MODULES -- the clock and the LATCH. This month we give details of these two modules. Next month we will discuss the final module – the COMPARATOR.

CLOCK MODULE ETI 551

The main module is a nine digit crystal-controlled clock with an easily varied counting format — it can count in ''hrs hrs, mins mins secs secs, 1/10th, 1/100ths, 1/1000ths,'' or in 000,000.000 secs, or, with slight modifications, in some other formats such as hours, minutes and fractions of minutes, or in 00.0000000 hrs.

LATCH MODULE ETI 552

The second module of which any number may be added to one basic clock module, is a nine digit latch which can either contain the same data as the clock module, or can store the number in the latter when a switch is pressed or a control pulse received. This enables one to 'freeze' the time in the clock module without interrupting counting — a stopwatch 'split' facility.

COMPARATOR MODULE ETI 553

The third module can give out a pulse, set a Flip-Flop or reset the clock module to zero. Any number of these modules may be connected to one basic clock module. One comparator could be used to sound an alarm after a preset time, or several could be connected together to switch a video tape recorder on and off at preset times, or to control some machine or an industrial process. (This will be described next month.

WHAT IF NINE DIGITS IS TOO MANY?

Although the counter, latches and comparators can all accommodate nine digits, those who only need to 'see' a few digits should not be put off. Because of the elegance of the SR (shift register) counting system used a nine digit counter requires nearly the same number of components as a six digit counter. In fact, on the PCB layouts we have only provided sufficient components to drive 6-digit displays. Those who require more will have to use a few additional components.

The 6 digits to be displayed can be chosen from any of the 9 digits: laboratory timers usually display minutes down to milliseconds; stop-watches can display hours to tenths of seconds, or tens of minutes to hundredths of seconds, whilst owners of video and other tape recorders could choose tens of hours to seconds. As yet we know no perfectionist who wants tens of hours to milliseconds!

COUNTING WITH A SHIFT REGISTER

The conventional design for a multi-digit counter used to be a chain of BCD counters, and a large arrangement of switches which sequentially feed the data from each stage of the counter to a single 'multiplexed' BCD output, suitable for driving the displays. This is the system found in most clock ICs, in some watch ICs and in nearly all circuits for clocks which used TTL.

However, as first realised three years ago, it is more efficient to make multi-digit counters by storing a number in a shift register and 'circulating' it through a binary adder adding one to a digit or setting it to zero at the required times. This system is found in most timing ICs designed in the last few years (e.g. the Mostek MK5030).

Figure 1 shows a block diagram of an SR counting system. The main advantages of the system are that as the data is handled sequentially (digit by digit) it is already in a format suitable for interfacing to multiplexed displays, and that increasing the size of the counter only requires increasing the shift register capacity and slightly modifying the control circuitry.

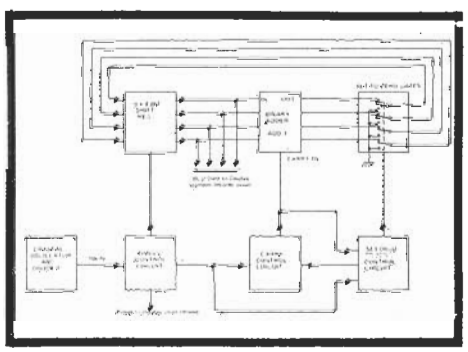


Fig. 1. An SR counter.

THE CLOCK MODULE

Figure 2 is identical to Fig 1 but the circuit blocks are filled in with actual components. For simplicity we will first discuss a clock using the "hrs hrs, mins mins, secs secs, 1/10th, 1/100th, 1/1000ths" format. This project does not have a separate "How it works" section; rather this is explained as we cover the various design options. The number in the counter is stored in a 9 x 4 bit shift register (4006 (1) and (2)). The output of the SR is returned to its input via a 2 digit and carry, 4 bit, binary adder (4008 (1)), and a set of 4 AND gates (4081 (1)). In one pass around the loop any digit may be left unchanged, incremented by one, or reset to zero. All that needs changing is the carry input to the adder and the common control to the 4 AND gates.

A 10kHz signal goes to the clock input of a 4017 decade counter and the 4017 produces 10 consecutive output pulses on its 10 output pins, Q0 to Q9, such that only one output is 'high' at any one time. One in ten of the 10kHz pulses which clock the 4017 is blanked by the Q9 output using a two input NOR gate (¼ of 4001 (1)). This signal is used to clock the shift register.

Thus in one millisecond the number in the SR is circulated once, and the 4017 goes through a complete cycle. The clock polarities are such that the SR is clocked (that is, new data is latched into its first stage, and new data appears at its output) at the same instant as a change occurs in the 4017 outputs.

The data present at SR outputs during the time in which Q0 is high is defined as the value of the least significant digit, called D0, that present while Q1 is high defines the value of D1, and so on. Q0 to Q8 can be used to drive display "digit drivers", and the SR outputs drive the display segments via a 4511 BCD-to-seven-segment decoder-driver.

"SET DIGIT TO ZERO"

A digit is recirculated unchanged until there is a 'carry' from the previous (less significant) digit. At this point it is incremented by '1' by the adder, and the new value recirculated. If however the digit in

PARTS LIST

CLOCK MODULE ETI551

CAPACITORS
Sixteen 10nF All ceramic
One each 27pF, 47pF, 68pF
one trimmer 2-22pF
two 100µF 2V electrolytics

RESISTORS
Nine 150Ω All 1/8th W
Five 120k
One each 560 ohm, 1k, 8.2k, 15k

DIODES
Seven 1N914 1N4001

CMOS
4000 4006 4017 4050 4511
4001 4008 4020 4081 75492
4006 4008 4027 4081
BC184 transistor
2N3704 "
5.12MHz crystal
ETI551 pcb
Seven 16 pin DIL sockets
Ten 14 pin DIL sockets*
(One 24 pin LSI socket)*
Two soldercon pins for Xtal socket
DIL Pin Header

DISPLAY MODULE ETI551D
Three DL33 3-Digit packs
One ETI551D pcb
6" 14 way flat cable
(14 pin DIL plug)*

LATCH MODULE ETI552

RESISTORS
Eight 150Ω Five 120k

CAPACITORS
Eight 10nF

DIODES
Four diodes (1N914)

CMOS 4006 4019 4050 75492
4006 4011 4027 4511
2N3704 transistor
ETI552 pcb
Five 16 pin DIL sockets
Five 14 pin DIL sockets*
(One 24 pin LSI socket)*
DIL Pin Header

DIGITAL STOPWATCH
One ETI551 One ETI552 Two ETI551D
One connector (6" of 24 way flat cable; with optional LSI plugs)*
Two miniature toggle switches
Three microswitches
One push-to-make switch
Battery connector
3 PCB mounting pillars
193x29x2.5mm red perspex
Verocase 751410J

* A couple of pounds can be saved if the connections are soldered in rather than using plugs and sockets.

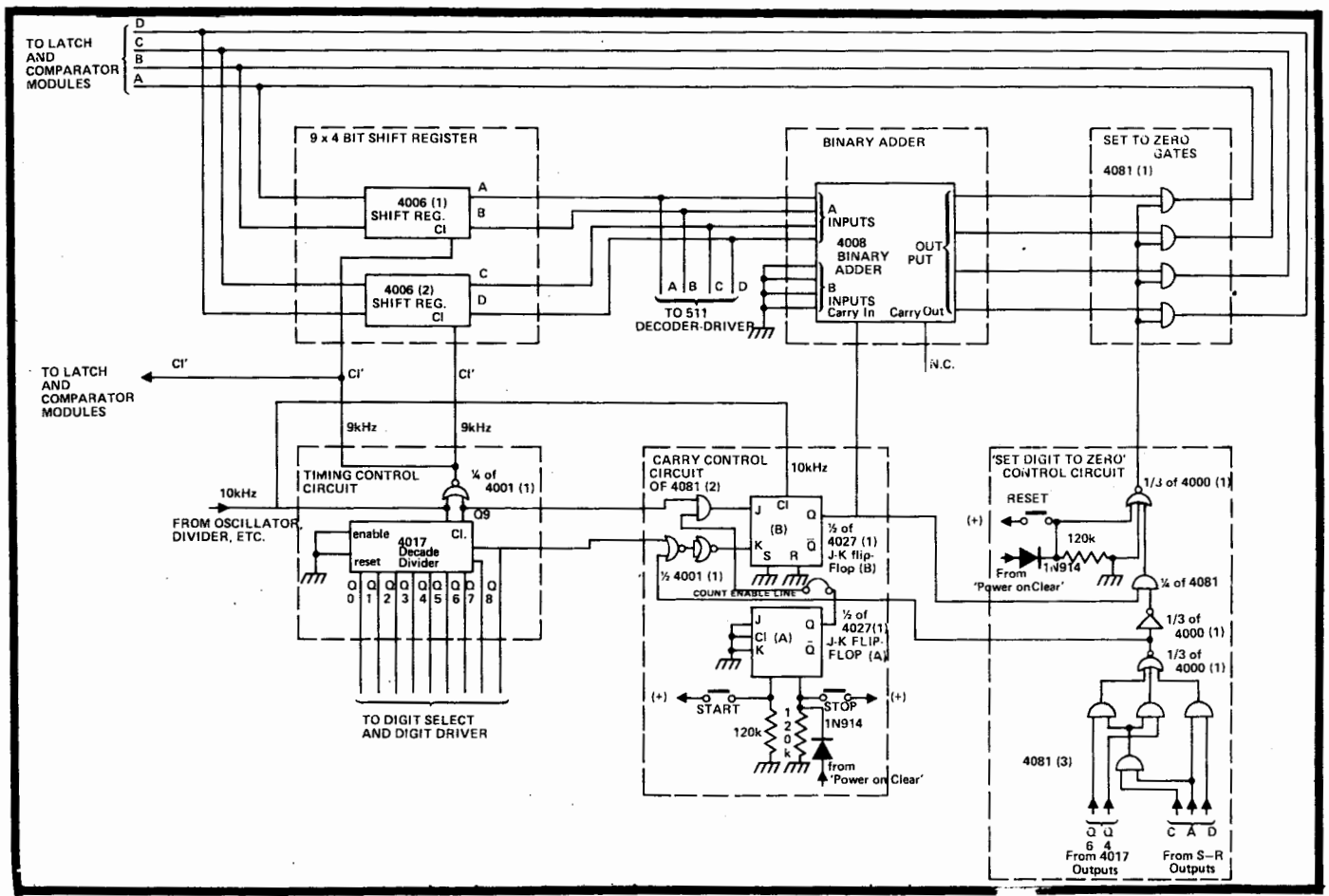
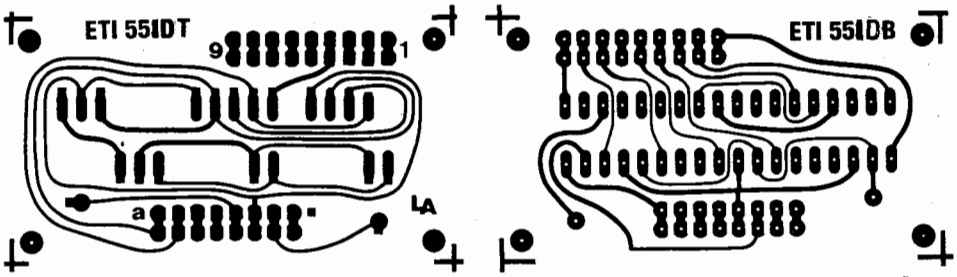


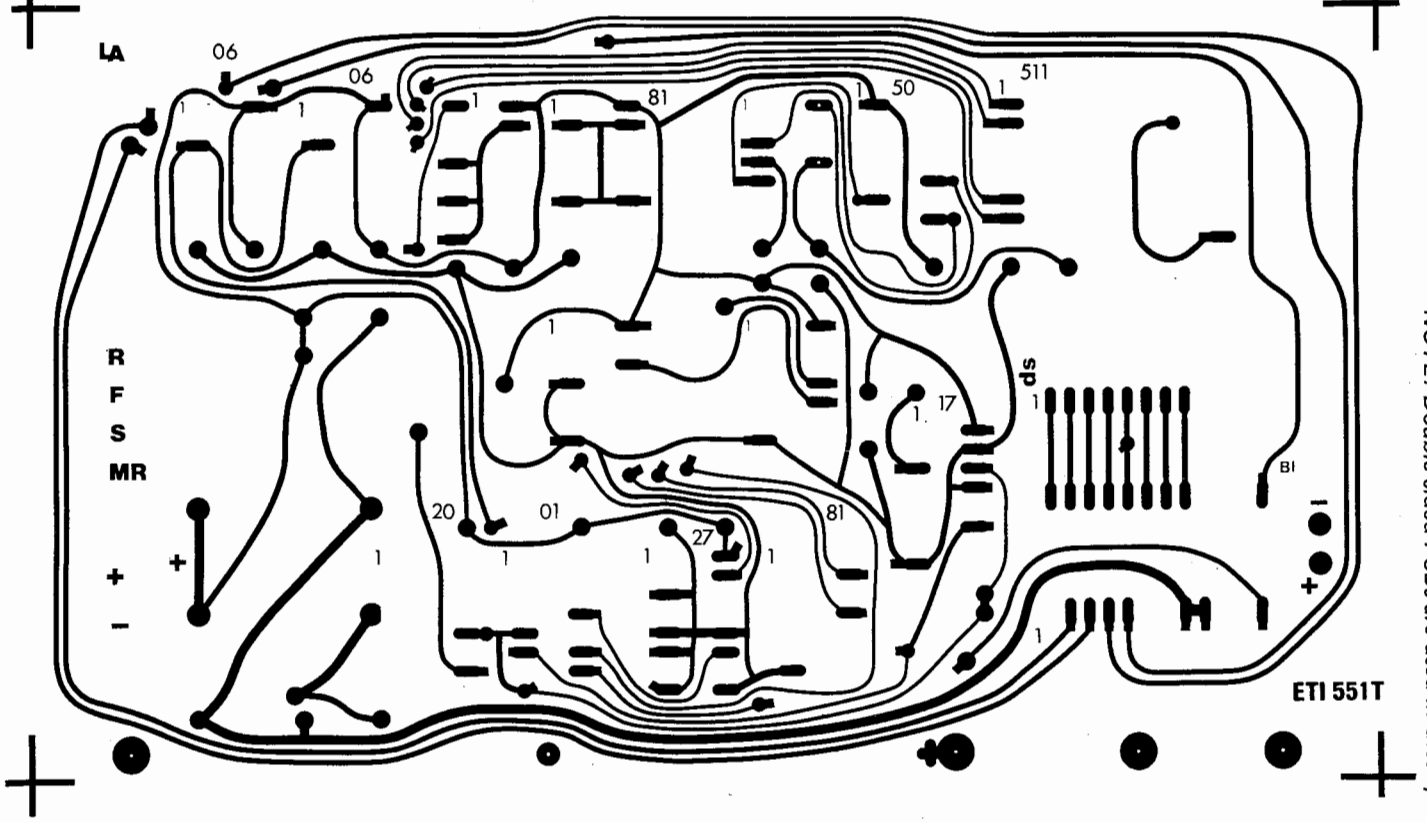
Fig. 2. Circuit diagram of the clock. Figs. 3,4,5,6 and 7 show other circuitry on the clock board.

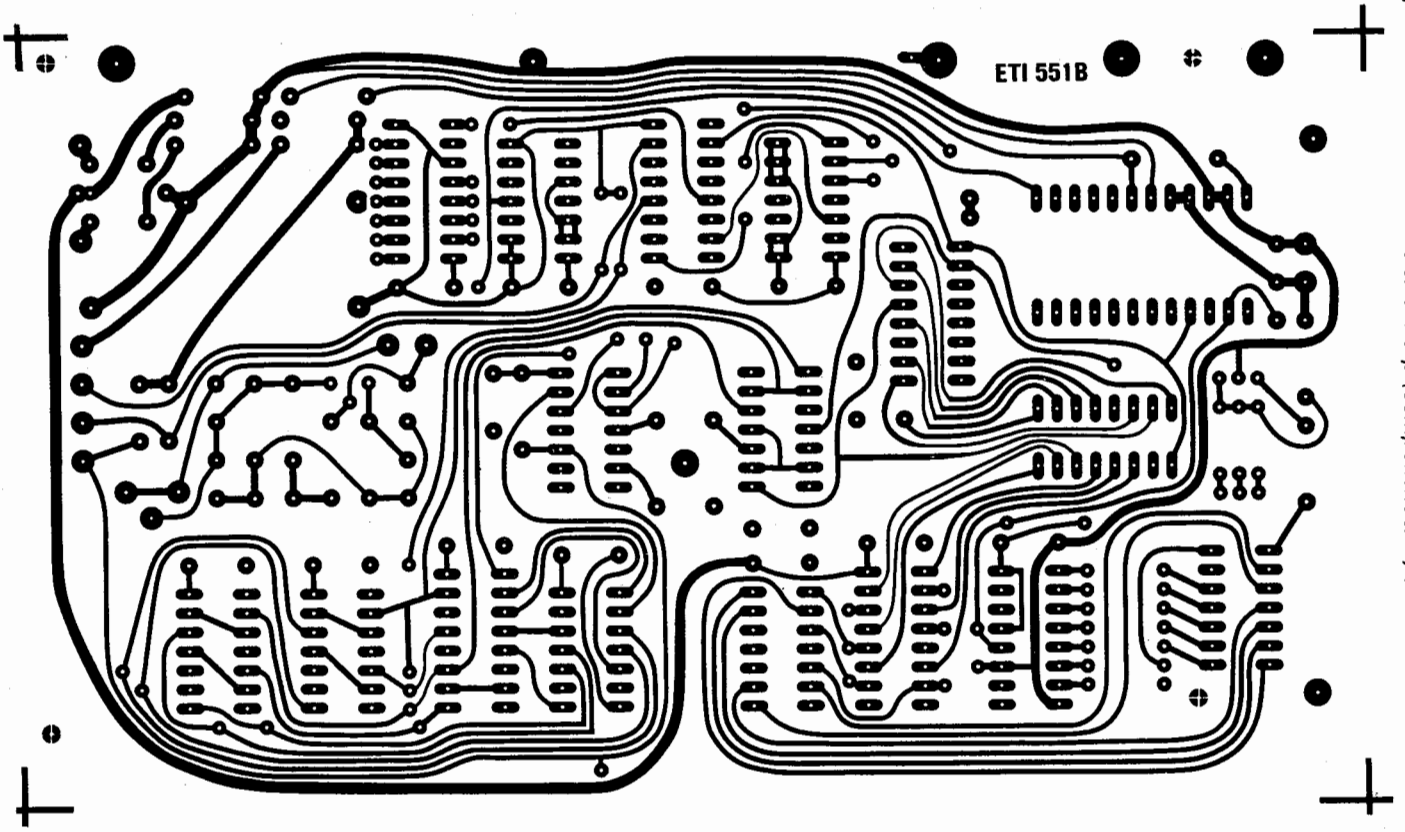
ETI TIMING MODULES

DIGITAL STOPWATCH

Main text continues on page 24







NOTE: Double sided PCBs are used in these projects. The suffix T refers to the top (component side) and B to the bottom.

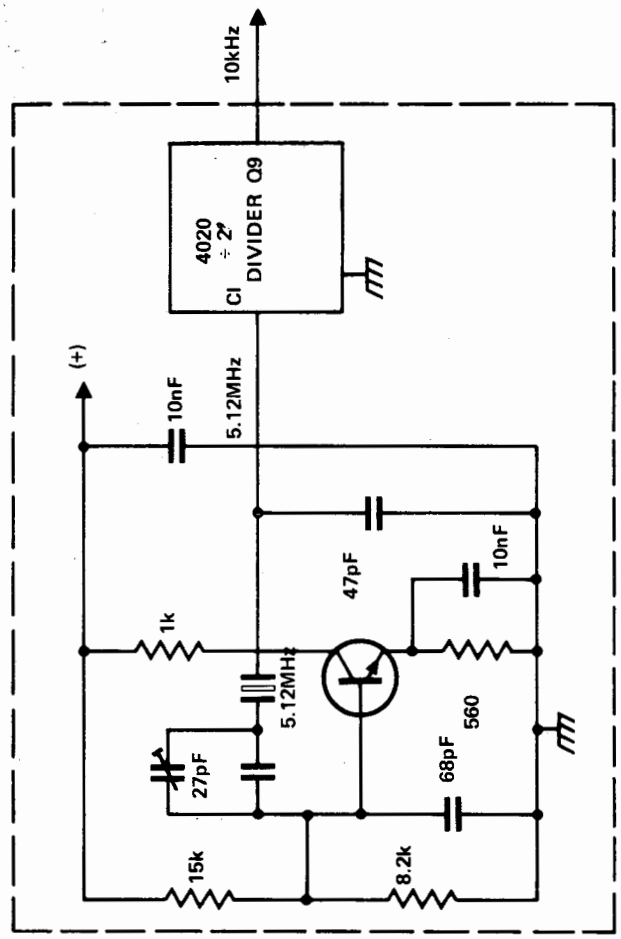


Fig. 3. Crystal oscillator and divider.

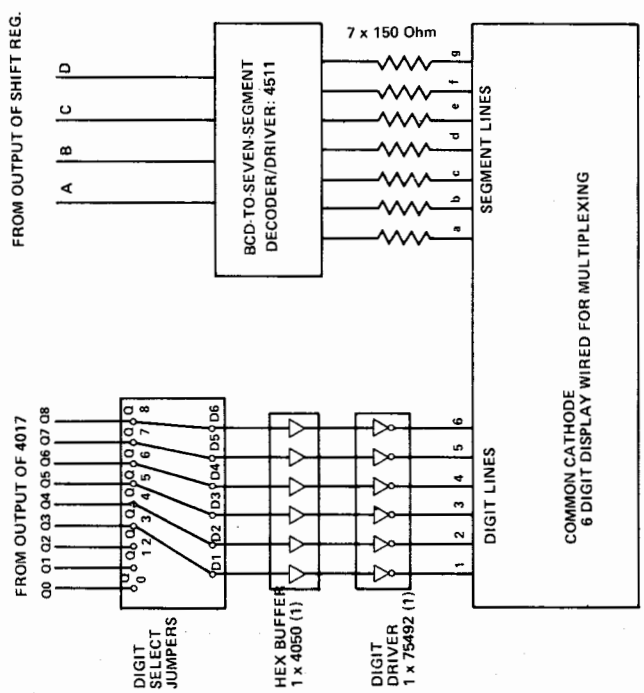


Fig. 4. Display Driving Circuitry.

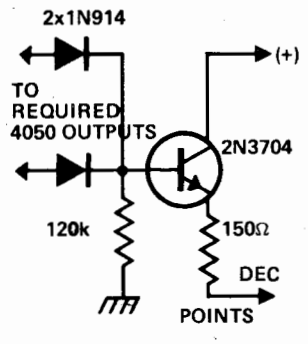


Fig. 5. Decimal Point Driver.

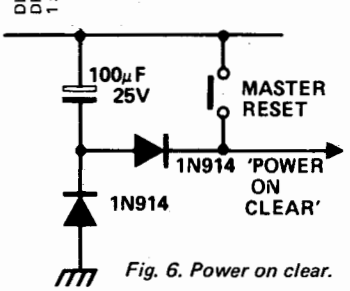


Fig. 6. Power on clear.

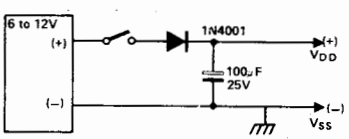
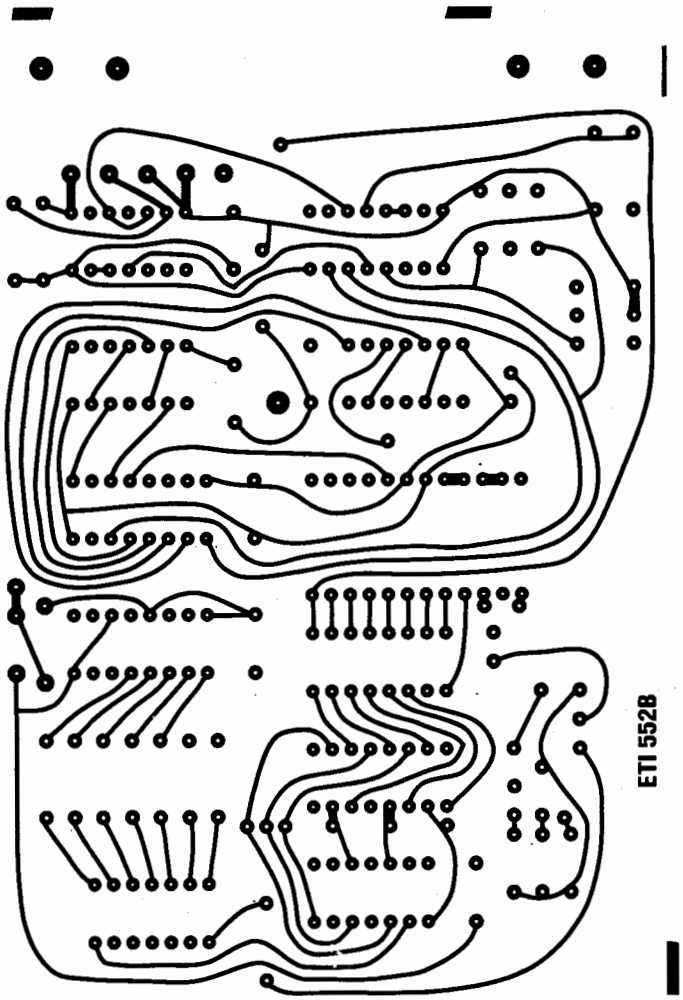
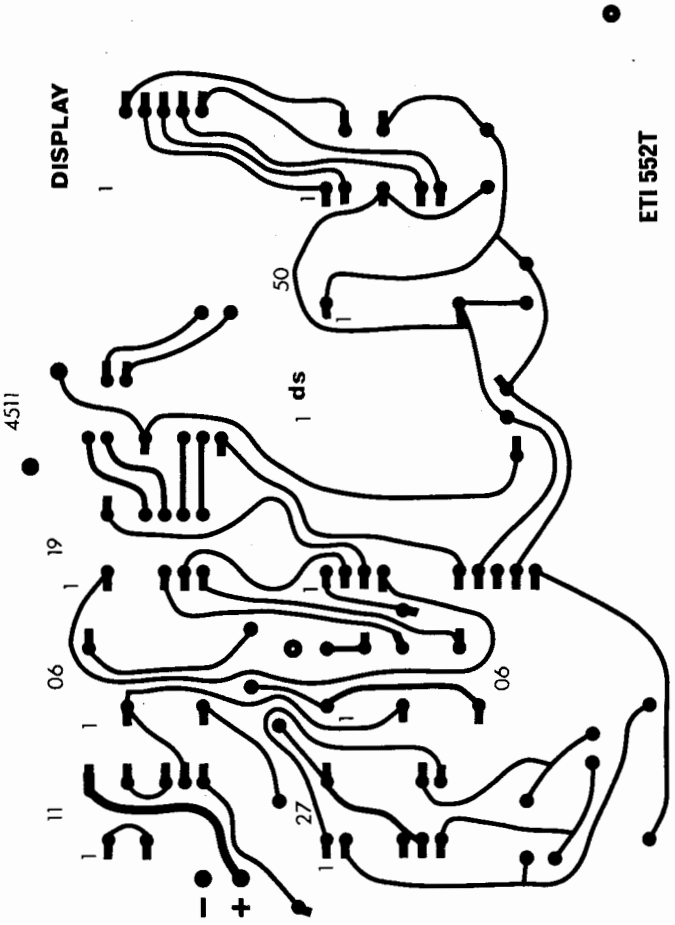


Fig. 7. Battery Power Supply.





DIGITAL STOPWATCH

question had already reached its maximum value ('5' for the tens mins and tens secs digits, '9' for all the others), instead of the value being incremented, it should go to zero, and a carry be transmitted to the next digit. This "Set to Zero" signal is derived from various gates as shown. In addition, pushing the Reset button for more than one millisecond sets all digits to zero.

"CARRY"

Before describing this part of the circuit it is worth looking at the operation of the 4027 J-K Flip-Flop. The J and K inputs are used to set (logical '1') or clear (logical '0') the Q output as follows:

If Q is '0', and J is '1', Q will go to '1' a few nanoseconds after the clock input goes from '0' to '1'. This occurs whether the K input is '1' or '0'.

If Q is '1', and K is '1', Q will go to '0' just after the clock input goes from '0' to '1' (irrespective of the state of the J input.) This a '1' on the J input will set the Q output on the positive edge of the clock pulse; a '1' on K will similarly clear it. If J and K are both '1', Q will toggle between '1' and '0', changing at every positive transition of the clock pulse. Q can be independently set or cleared by a '1' on the set or reset inputs.

The Q output of Flip-Flop A (½ of 4027 (1)) is set to '1' by pressing the Start button. This '1' is then used to set the Q output of Flip-Flop B (½ of 4027 (2)) to '1' at the start of Q0 time (the period during which Q0 of the 4017 is high). This Q output is the 'carry' signal, and when D0 (the digit whose value is present at the SR outputs during Q0 time) is clocked back into the SR at the end of Q0, it is incremented by 1 once every loop of the SR, i.e. once every milisecond.

Until D0 has reached its maximum value, D1 must not be incremented, and the carry must be 0, every time D1 is clocked back into the SR (at the end of Q0 time.) The condition that D0 is not at its maximum value is indicated by a '1' on the MAX output of the "Set to Zero" circuit, which goes to the K input of Flip-Flop B and cancels the carry at the beginning of Q1 time. If D0 has reached its maximum value, then MAX is low during Q0 time, the carry is not cancelled and increments D1 at the end of Q1 time.

If both D0 and D1 have their maximum values, the carry will propagate to Q2 time, etc. Thus if the counter is counting, the carry is set during Q0 time, and propagates 'down' the number until cancelled. It is also cancelled by Q8 at the beginning of Q9 time so that the counter behaves itself if it overflows.

10 kHz SOURCE

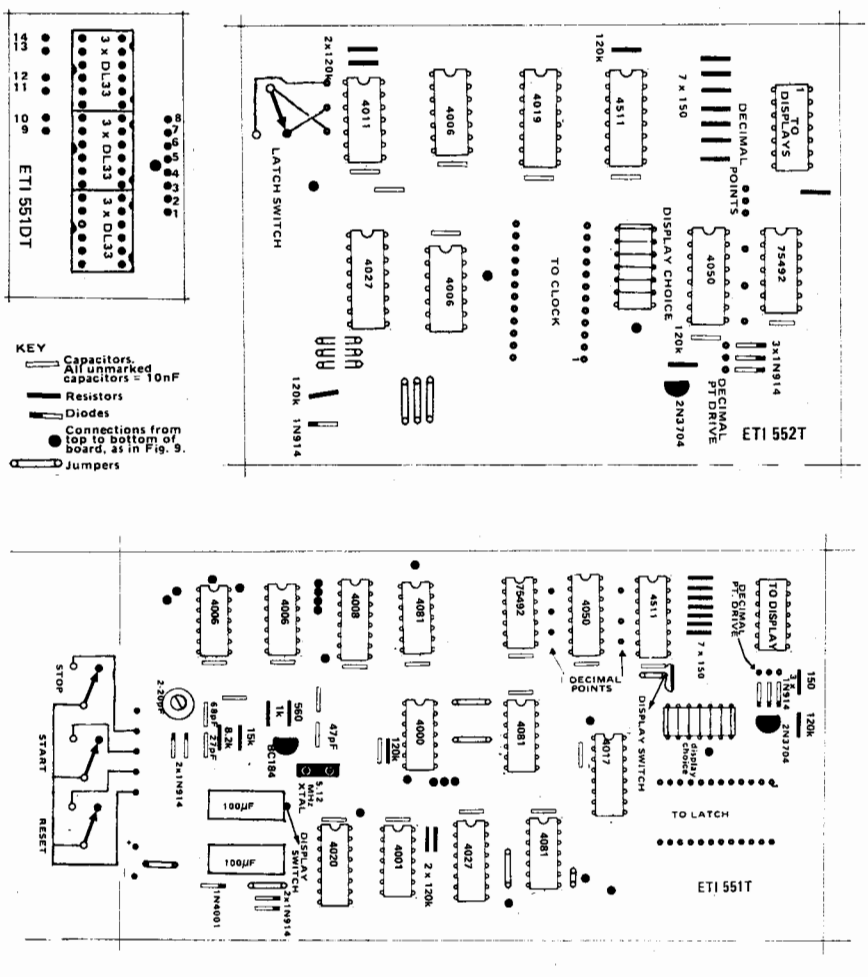
The 10 kHz signal is obtained by dividing the output of a 5.12 MHz crystal oscillator by 512 (2^9) using the first nine stages of a 4020 14 stage binary counter (see Fig 3.) The disadvantage of using a crystal of this frequency is that a transistor oscillator has to be used rather than a CMOS inverter oscillator (which doesn't have enough gain at this frequency to sustain oscillation). The advantages are that crystals over 5 MHz are cheaper, inherently more stable, and physically smaller than lower frequency crystals.

DISPLAY DRIVING

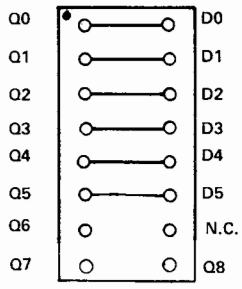
The digit and segment driving circuits are straightforward (Fig. 4). The SR outputs are fed to a 4511 BCD-to-seven-segment decoder-driver, which drives the display segment lines through current-limiting resistors. The maximum recommended continuous output current per segment on the 4511 is 25 mA, and with a 8V supply (typical output voltage of a 9V battery) the resistor value required is 150 Ohm.

The digit driver as shown will drive 6 digits. The digits required are selected by wiring jumpers between six of the nine Q0 to Q8 outputs and the six 4050 hex buffer inputs. For convenience on the PCBs these connections have been laid out in a standard DIL format so that the jumpers can be wired onto a pin-header and the required selection 'plugged in'. Q0 corresponds to the least significant digit, i.e. milliseconds, and Q8 to the most significant, i.e. tens of hours.

The component layouts for the clock, latch and display boards.

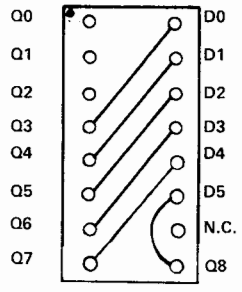


Here are three examples:



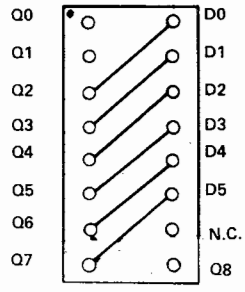
(a) is wired to display

mins	D5
secs	D4
secs	D3
1/10	D2
1/100	D1
1/1000	D0



(b) is wired to display

hrs	D5
hrs	D4
mins	D3
mins	D2
secs	D1
secs	D0



(c) is wired to display

hrs	D5
mins	D4
mins	D3
secs	D2
secs	D1
1/10	D0

The 4050 buffers are needed to drive the 75492 hex digit driver. The latter contains six Darlington Pair NPN transistors with the required resistors and can supply digit currents up to 250mA per digit.

Decimal points may be lit if required by wiring jumpers from the required 4050 buffer output to the decimal point driving circuit (Fig. 5). Thus decimal points are wanted after hrs and mins on a display (hrs hrs . mins mins . secs secs) for right-hand decimal point digits, the Q5 and Q7 time dec pts have to be lit, and jumpers are connected from the outputs of the 4050 buffers corresponding to Q5 and Q7 (D2 and D4) to two of the diodes in the dec pt driving circuit.

DISPLAYS

The driving circuitry will drive any common cathode LED displays, such as the DL33MMB (0.08in), DL704 or DL704E (0.3in) and FND500 or DL750 (0.5in and 0.6in).

POWER ON CLEAR

A simple circuit is provided which sets the counter to '0' and puts it into the stop mode when power is turned on (Fig. 6).

THE LATCH MODULE

The essence of the latch module is that it contains a shift register and display driving circuitry identical to that of the clock module. There is also switching circuitry to enter into the latch SRs the same data as is entered into the clock SRs, or to circulate the data unchanged. Finally there is circuitry to time the change between these two states. The data routing is accomplished by a 4019 Quad AND-OR gate which is basically a 4 pole 2-way switch which routes data from the inputs of the clock SR to the inputs of the latch SR when KA is '1' and KB is '0'. It connects the latch SR input to its output when KA is '0' and KB is '1'.

The 4027 J-K Flip-Flops time the changeover of the 4019 switch. These Flip-Flops can be wired in two modes. In the 'hold-transparent' mode the latch starts 'transparent' (the data it contains follows the contents of the clock module). When the latch push-button is pressed the latch stays transparent until the beginning of the next word (until the next Q0 time occurs) and then the 4019 switches over and the number in the SR is circulated

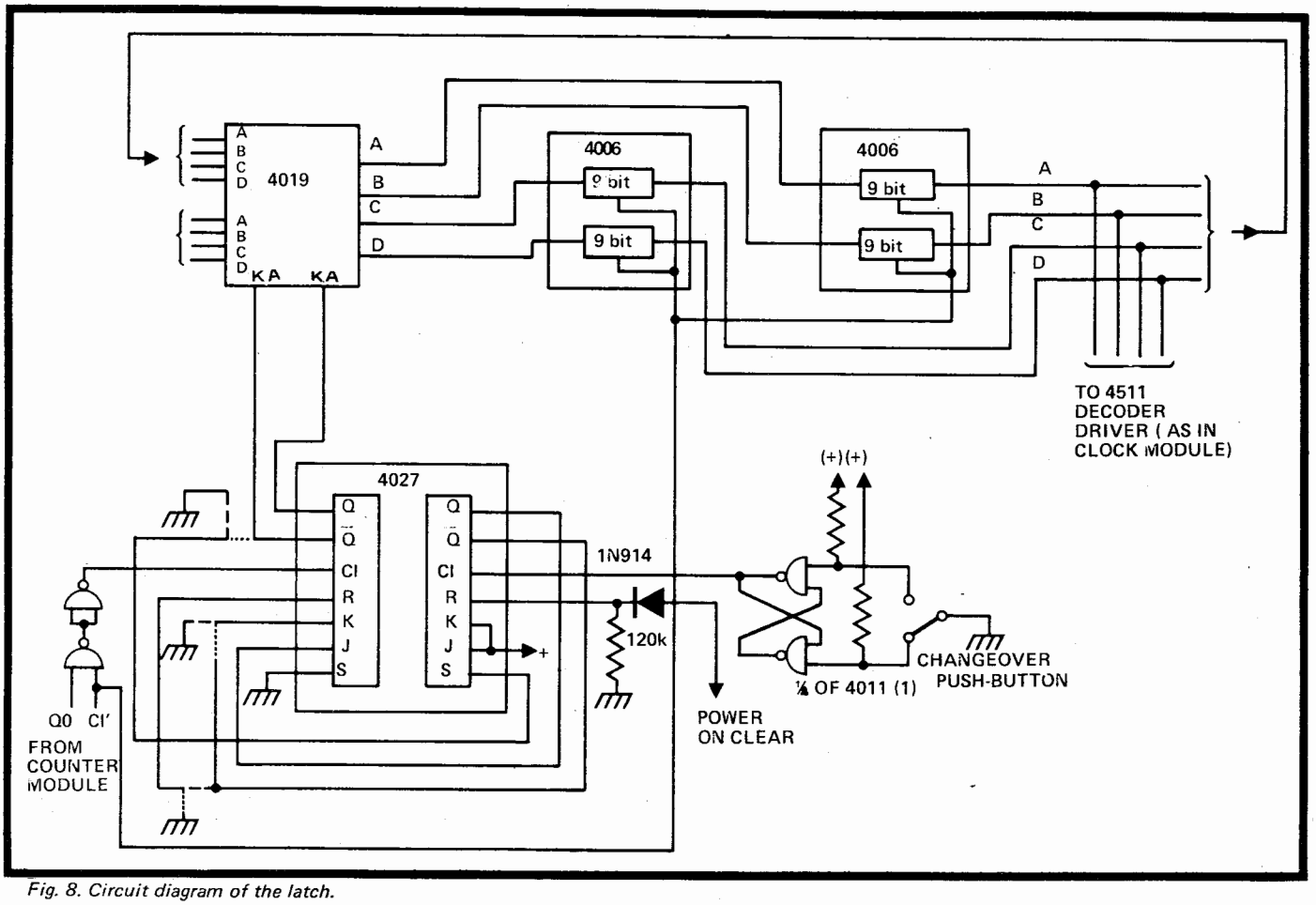


Fig. 8. Circuit diagram of the latch.

DIGITAL STOPWATCH

and displayed: the latch 'holds' the time at which the button was pressed, accurate to within +1msec. Further pressing of the latch button causes the module to alternate between the 'transparent' and 'hold' states.

Wiring the J-K Flip-Flops the second way makes it operate in the 'hold-hold' mode. In this mode the latch starts off 'holding' its contents. If the latch button is pressed, in the middle of the next Q0 time the 4019 is switched to loading new data into the SR. In the middle of the following Q0 time the 4019 switches back to recirculating and holding the data. Thus in this mode the display always appears 'frozen', but each time the latch button is pressed the contents of the latch are 'updated' to show the number in the clock module at that moment. This mode is expected to be found most useful in applications where the latch is controlled by an external source. In either mode the "Power On Clear" circuit is connected so that when power is switched on, or when the Master Reset button is pressed, the latch is loaded with zero, and in the first mode it is set to its 'transparent' state. In both modes, two NAND gates (½ of 4011 (1)) eliminate any effect of contact bounce in the push-button switch.

Selection of one mode or the other is governed by wiring up three jumpers or switches. On the PCB there are holes for three horizontal jumpers and three vertical jumpers. If the horizontal ones are connected (indicated by faint dotted lines in Fig. 8) the latch will operate in the hold-hold mode. If the vertical ones are connected (indicated by bold dashed lines in Fig. 8) it will operate in the hold-transparent mode. The display selection and driving circuitry used in the latch modules are identical to those used in the counter module.

Some users may find it best to attach a display to only the latch module, thus saving cost while still obtaining a Stop-watch 'split' action. As mentioned earlier, any number of latch modules may be connected to one clock module. The outputs from the clock module are simply attached to several modules instead of just one.

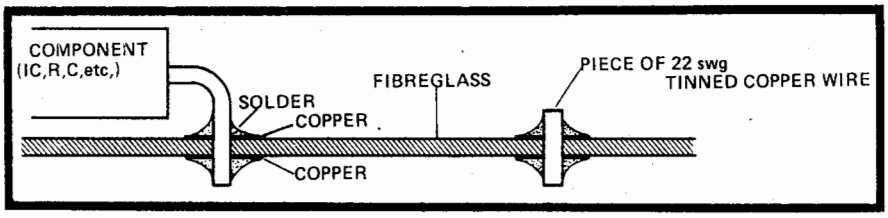


Fig. 9. How to make connections through the board.

CONSTRUCTION

The modules are best assembled on double-sided PCB's as shown, due to the circuit complexity. Connections between copper on the top and bottom of the boards are made using component leads where possible. Otherwise small pieces of tinned copper wire are used (see fig 9 above).

The recommended method of mounting the CMOS IC's is to use Soldercon pin sockets which can be soldered to both sides of the board (and are inexpensive). The ICs may be soldered in but this makes fault-finding very difficult. On the component side of the board, care must be taken only to apply solder to the flat side of the Soldercon Pins.

Connections between modules are made very simple, and easy to check, using flat cable and 24 pin plugs and sockets (using 24-way pin-headers and Soldercon pins in a 24-pin DIL layout). Connections between modules and display PCBs are also made using flat cable and 14-way DIL pin-headers and IC pin sockets.

The PCB's were designed so that one clock module, one latch module and either two DL33 6 digit displays or one DL704 or FND500 8 digit display, with batteries, switches, etc, would all fit into the smallest of the new Vero plastic cases, using a transparent red perspex front window in the space normally occupied by an aluminium panel. If greater complexity is required, one of the larger boxes in the same range may be used.

GETTING HOLD OF THE COMPONENTS

Sintel (53 Aston Street, Oxford), who designed these modules can sell the following at reduced prices.

Stopwatch Module Kit (SMK). . £19.95
(This comprises the PCB and all the parts normally soldered to it: CMOS, SKTS, CRYSTAL, Resistors, Caps, etc. etc...)

Latch Module Kit (LMK) £11.25
(This comprises all parts plus Vero pillars for support and flat cable for interconnection with SMK)

CHOICE OF DISPLAY MODULES

DL704 Display Kit (DL7K) (.3"). £6.96
(This kit comprises a display PCB and 6 DL704).

DL33 Display Kit (DL3K) (.1"). . £7.10
(This kit comprises of a display PCB and 3 DL33 3-Digit packs)

FND500 Display Kit (FNDK) (.5"). £11.15
(This kit comprises a display PCB and 6 FND500)

CASE

Verocase £3.17
(This case is big enough to accomodate one SMK and one LMK plus two DL3K or one of DL7K or FNDK, and the case is supplied with a red perspex panel).

ALL PRICES ARE INCLUSIVE OF VAT AND P&P

EXTRAS

A stop-watch which gives time to millisecs is great but the average human finger can't do much better than 1/20th of a second. We expect some constructors will need to actuate their modules using electronic, rather than mechanical, pulses.

ELECTRONIC START-STOP

Electronic starting and stopping can

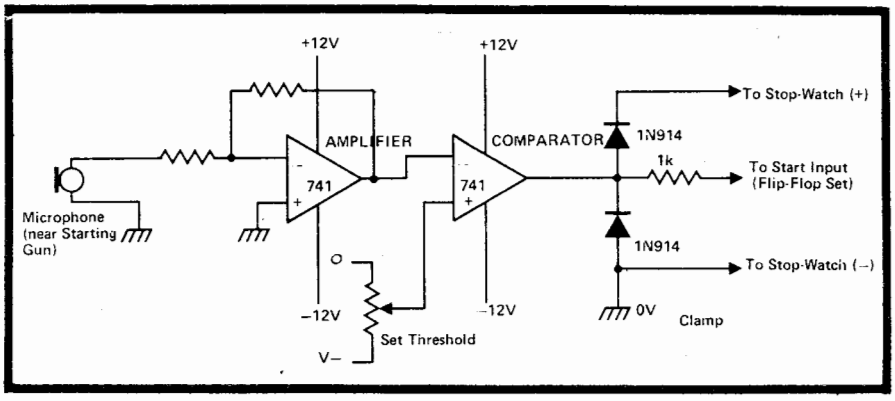
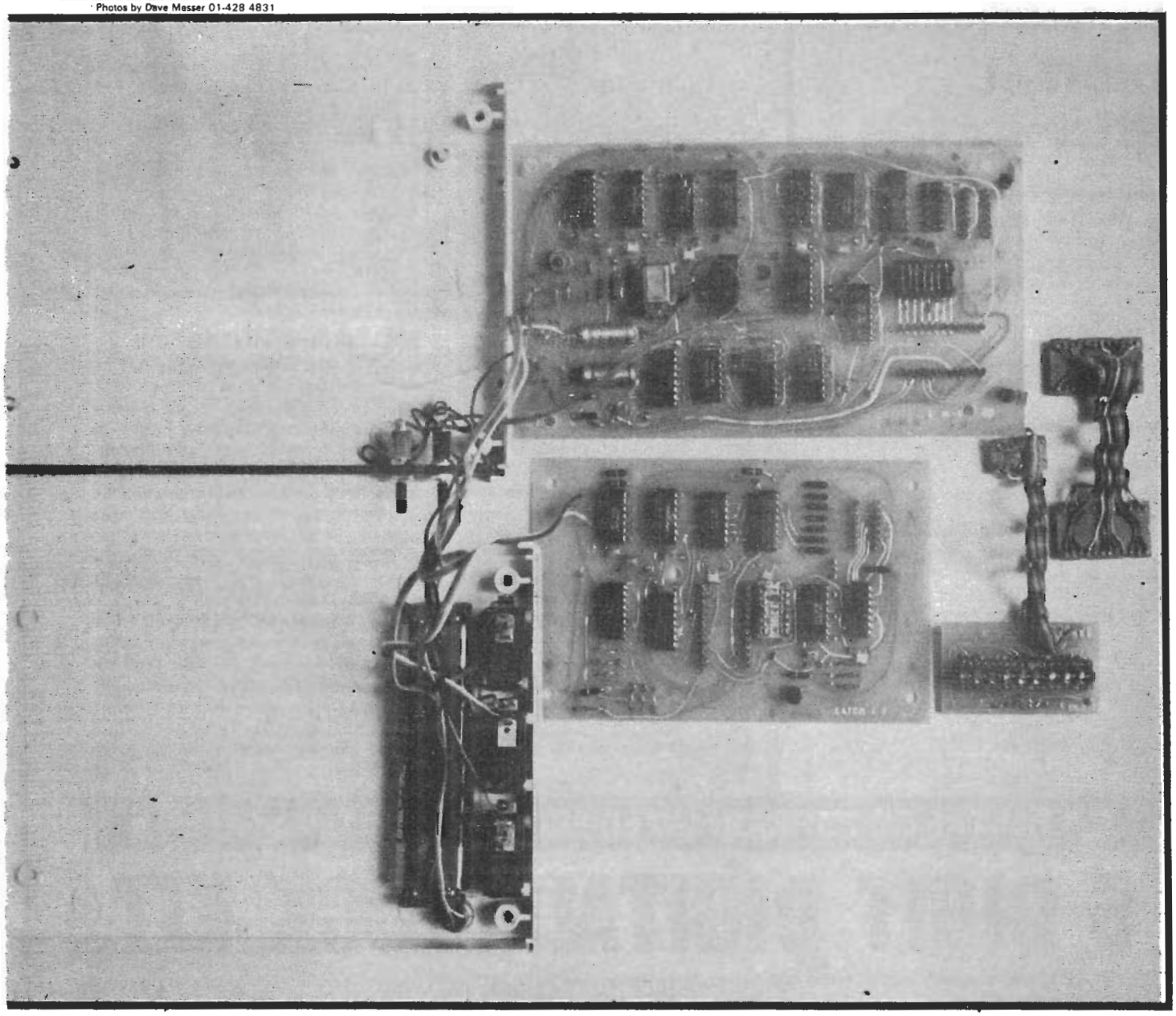


Fig. 10. A simple circuit for using the sound of a starting gun to start the Stopwatch.

Photos by Dave Messer 01-428 4831



The insides of the stopwatch. The clock board is at the top,the latch beneath. Here we show one display, but a second display module will plug in directly. A small saving can be made by soldering the flat cable directly onto the boards rather than using the LSI plugs as shown.

be achieved by feeding positive going pulses to the set and reset inputs of the clock module 4027 A Flip-Flop. These pulses do not have to be 'clean' but it should be noted that the state of this Flip-Flop is not determined if both these inputs are high simultaneously.

Obvious electronic timing systems would be ones where the start time is derived from a signal driving a solenoid operated starting gun, or from sound pulses. Below is a simple circuit of a suggested sound operated start system (see fig 10).

A simplified suggested light operated start or stop is as shown in fig 11.

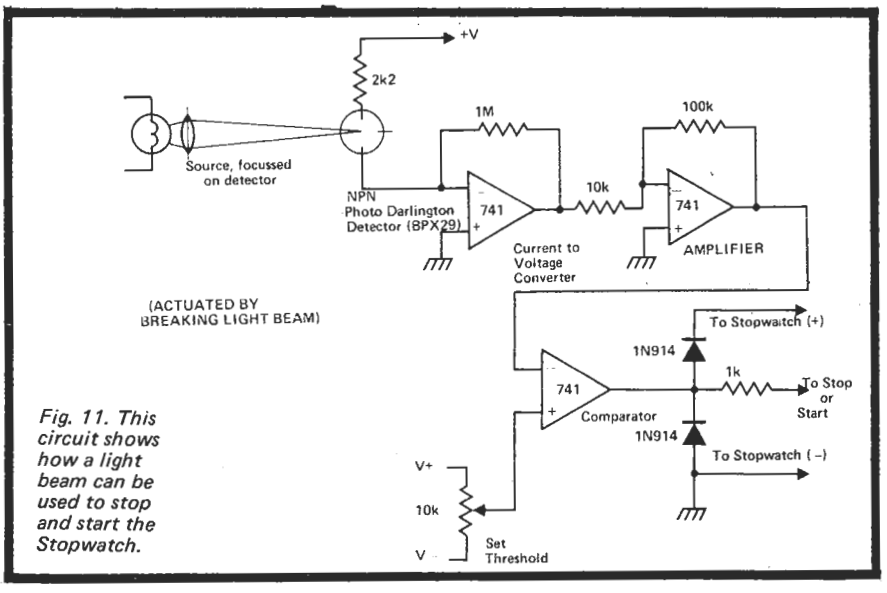


Fig. 11. This circuit shows how a light beam can be used to stop and start the Stopwatch.

ETI TIMING MODULES

DIGITAL STOPWATCH

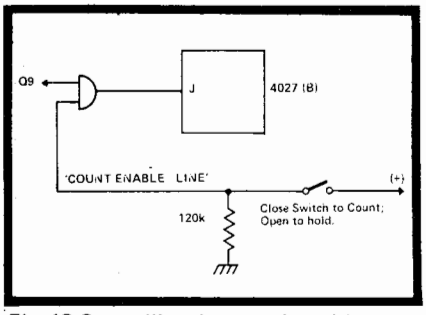


Fig. 12. Controlling the counting with a toggle switch.

COUNTING CONTROLLED BY TOGGLE SWITCH OR CONTINUOUS SIGNALS

If the count enable line (normally driven by the Q output of the 4027 A Flip-Flop, on the clock module) is high the module will count, if it is low it will hold its value. Thus the counting can be controlled by driving this line from an external signal instead of from the flip flop output. For example the counting can be controlled by a toggle switch:

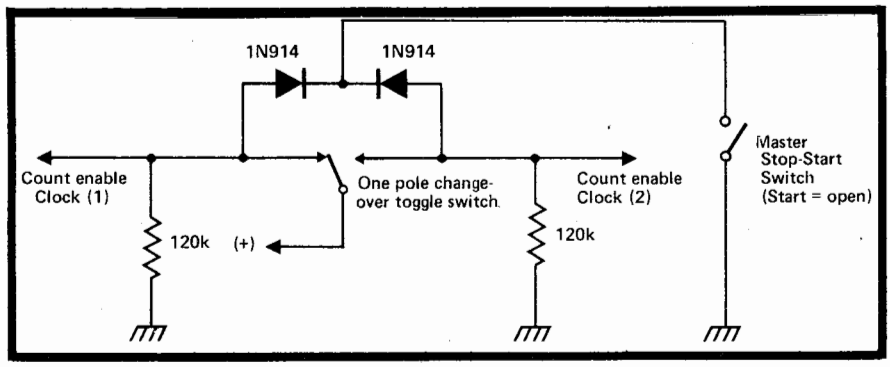


Fig. 13. Two clock modules can be wired up to give a chess clock.

CHESS CLOCK

To build up a system which compares the accumulated time spent in each of two states, such as a chess clock; one could use two clock modules with their count enable lines connected like this:

They should also have their reset lines connected together. When using more than one clock module in one system, such as this chess clock, considerable savings can be made by constructing the crystal oscillator and 4020 divider on only one of the modules, and taking the 10KHz signal from this to the other boards.

ENDLESS POSSIBILITIES

Virtually any timing necessity can be satisfied using a system made up from the ETI TIMING MODULES. In our clock we used two displays – but we could have used just one display show the contents of the latch). We could have made a more complicated Stopwatch by adding more and more latches. With ten latches and ten switches you could give individual times to the first ten runners, swimmers, racing cars .....

The possibilities mushroom when you consider the comparator module as part of a system. A clock becomes an alarm clock or timer. If you use the output to reset the clock you have a programmable pulse generator with a period ranging from milliseconds to tens of hours. ●