Date display, BST switch and alarm

Add on circuits for the time code clock

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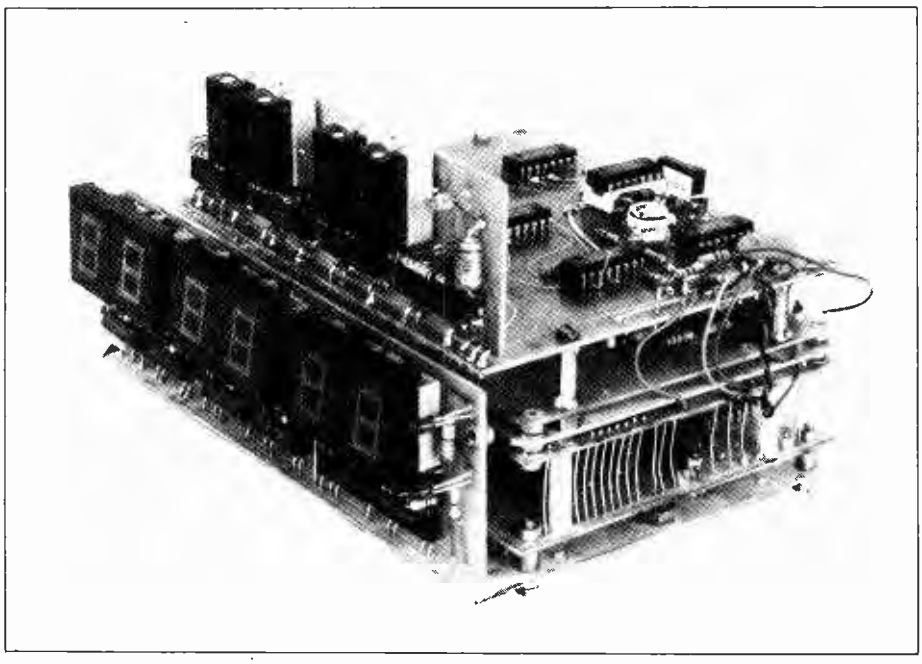
This article describes a decoder which enables the self setting time code clock, *Wireless World* August 1976, to display the day and month and automatically switch the GMT/BST converter. A second circuit provides an alarm facility which can be programmed with thumb wheel switches. The complete design offers an alarm clock and calendar of unquestioned accuracy, 1 second in 3000 years, which never requires settting and which takes care of leap seconds, leap years and British Summer Time automatically.

The 60kHz Rugby MSF transmission now includes date information in addition to the established time of day code. A British Summer Time bit is also encoded as well as a further parity check on the date information alone. The hours and minutes are transmitted as previously and are complete 200ms after the minute edge as shown in waveform A of Fig. 1. Date information is in the same b.c.d. format and follows on with the carrier representing a 1 and no carrier a 0. A logic 1 is also transmitted in the BST slot if British Summer Time is in operation.

The wide range of c.m.o.s. integrated circuits has made their choice attractive for this part of the design. They enable power saving and interface easily with existing t.t.l. circuitry. The three input signals required are available from the edge of the existing seconds-counter p.c.b. without any dismantling. Waveforms obtained at these points when decoding takes place are shown in Fig. 1. A and F are shown in the inverted form.

Circuit description

Data arrives serially and is assembled into parallel form to drive the displays. The data is clocked into a shift register composed of IC_1 and IC_2 see Fig. 2, in a similar fashion to the time-code part of the clock. A 100Hz oscillator is required to start at the moment the time decoder



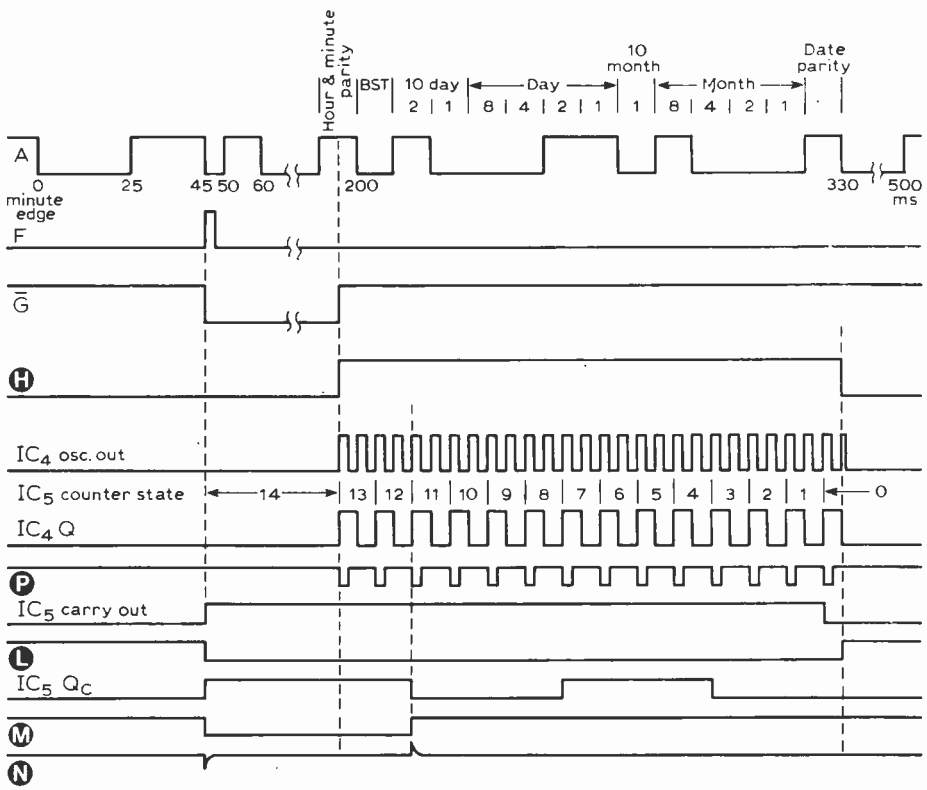


Fig. 1 Waveforms from the date decoder circuit. The three input signals are taken from the time decoder of the original clock.

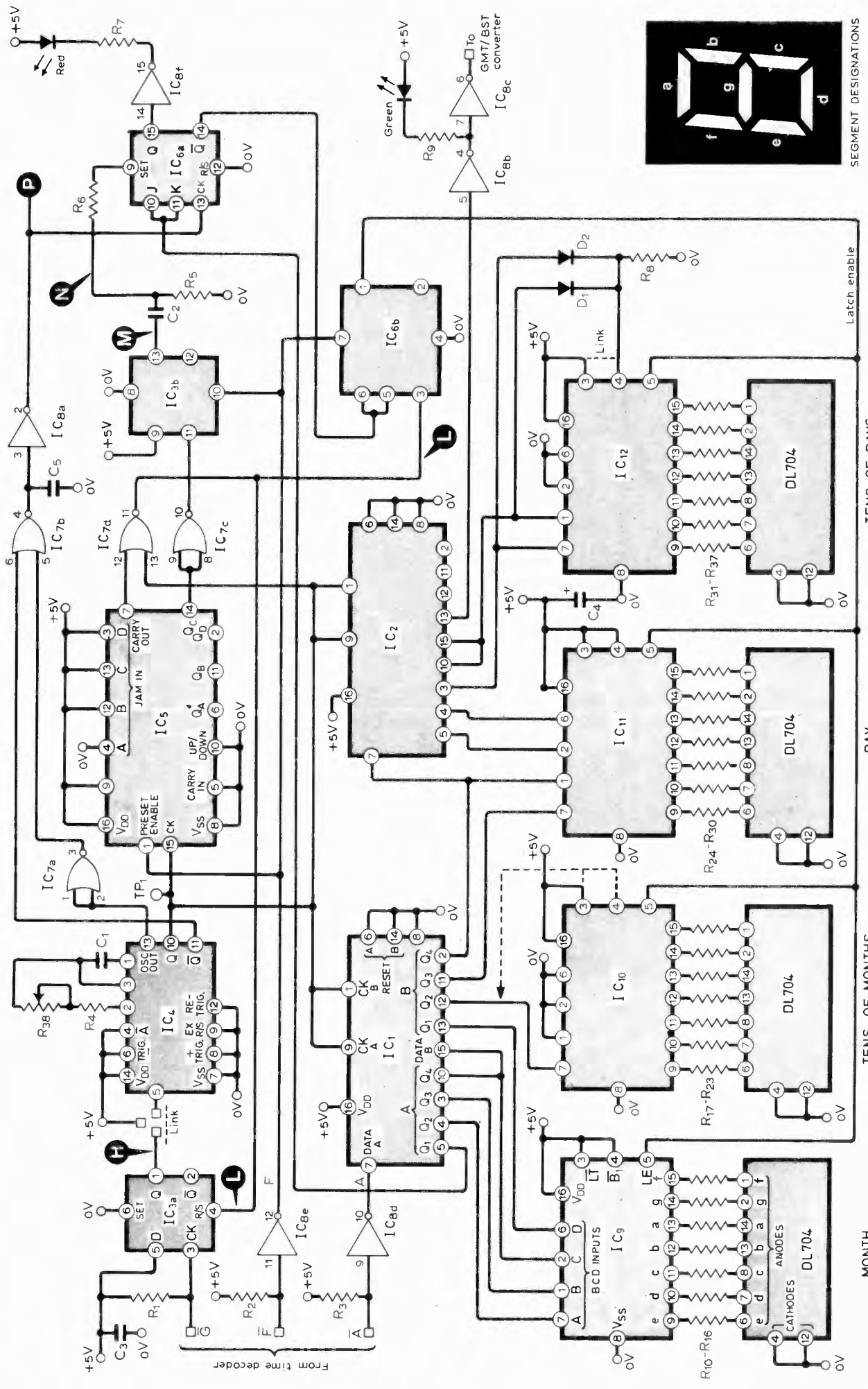


Fig. 2. Circuit diagram of the date decoder and BST switch. For normal operation pins 4 of IC_{10} and $_{12}$ are connected to +5V. If leading zero blanking is required, pin 4 of IC_{12} is connected to D_1 and D_2, and pin 4 of IC_{10} is connected to pin 7 of IC_{10}.

100Hz clock stops so, in order to avoid any modification to existing units, a separate clock generator is used. A c.m.o.s. astable multivibrator is used, which incorporates gating, provides an oscillator output, and the oscillator output divided in frequency by two. The positive edge of the waveform G, obtained from the time-decoder, represents the starting point and is used to clock a D-type flip-flop IC_3 (a) which enables astable IC_4. The resulting oscillator output is shown in Fig. 1 together with the Q output, which is the half-oscillator-frequency waveform. Gating by IC_7 (a)(b), and spare inverter IC_8(a) is used to generate the NAND function of these two waveforms to give the signal P, which has a positive edge delayed by 2.5ms for the parity checking circuit.

The positive edge of the Q output clocks data A into the shift registers and clocks a pre-settable counter IC_5. This i.c. counts down from the previously pre-set count, which is determined by the state of the "jam" inputs at the time of the preset enable signal shown as F in Fig. 1. When the counter reaches zero on the arrival of the fourteenth positive clock edge, the "carry out" terminal goes low. This signal is NOR gated with the clock Q to produce L so that when Q also goes low 5ms later, IC_3 is reset, which stops the astable. This happens 5ms after the last active clock edge, and the positive edge of L clocks the JK flip-flop IC_6(b). The purpose of this is to provide a "latch enable" signal or otherwise, for the display decoders.

Parity checking

The new parity bit refers only to the date code and does not include the BST bit. The transmitted parity bit is such that the signal always contains an odd number of 1s. Just before the arrival of the date at the minute, the signal F pre-sets the counter, resets IC_3(b), and sets IC_6(b). The D type flip-flop IC_3(b) is used to determine the start of parity checking by setting IC_6(a) when the counter output Qc first goes low as the count of 11 is reached. The positive transition of IC_3(b) is differentiated by C_2 R_5 to provide a pulse which sets the parity checking JK flip-flop IC_6(a). The Q output of this device is set high by the pulse and changes state for every 1 present at the J and K inputs which are connected to the signal A. The Q output of IC_6(a) should finish low because of the odd number of 1s. If an even number are received the Q output remains high, which is indicated by a l.e.d., and inhibits the display of the code.

When the latch enable signal is high, the display decoders store the information that was present just prior to the high. The Q output of IC_6(b), which is connected to the latch enable inputs, is set high before the entry of the new date code, and is clocked 2.5ms after the completed parity check by the positive edge of L. If an error is detected, IC_6(b)

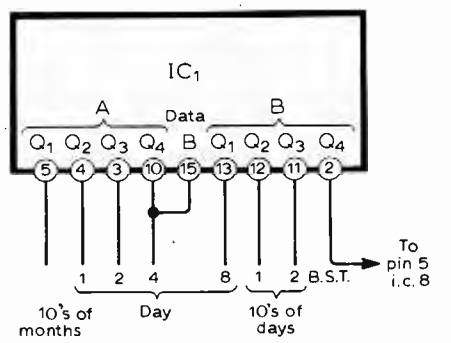


Fig. 3. Outputs of IC_1 when the simplified display is used.

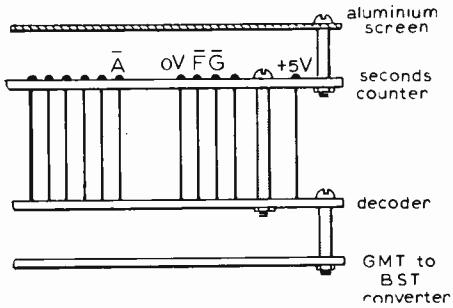


Fig. 4. Output from the original clock module. A sixth connection is made from the date decoder board to the GMT/BST converter for automatic switching.

JK inputs are low inhibiting any change on receipt of the positive edge of L. The Q output remains high until the next minute which prevents information from being displayed when a parity error is indicated. Entry of the date code at each minute does not require display blanking because the displays are latched to the stored code from the previous minute and do not display the new code until it has been validated.

To display only the day number without a parity check and register the BST information, shift register IC_2 and others parts may be omitted by simply pre-setting counter IC_5 with the binary equivalent of 9 instead of 14. A pre-set 9 requires 1001 at the "jam" inputs which is achieved by taking pins 12 and 13 of

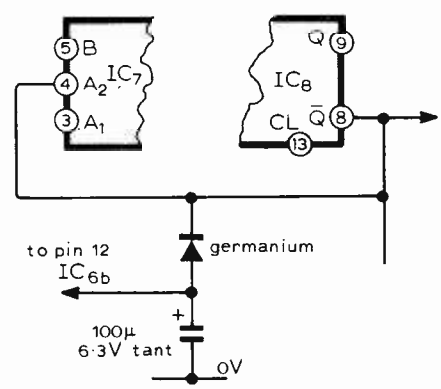


Fig. 5. Modification to the existing time-decoder circuit (Wireless World, Aug. 1976, p.49, Fig. 4). This addition prevents retriggering if the 13 bit date-code appears the same as the time-code.

the counter to 0V instead of +5V, and pin 4 to +5V instead of 0V. The day is then strobed into IC_1 and indicated by what are normally the month displays. Pin 1 of IC_{10} must be connected to pin 11 of IC_1, instead of 0V, to obtain the full code for tens of days, and segment "g" of the display does require a drive resistor in this case. The BST bit now appears on pin 2 of IC_1 which may be linked to the appropriate vacant hole for pin 13 of IC_2. Finally, the "latch enable" line is wired to the "carry out" terminal of IC_5 so that the displays do not flicker when the new information is entered into the shift register. In addition to $IC_{2, 6, 11}$ and $_{12}$, C_2, $R_{5, 6}$ and $_7$, the segment drive resistors and displays normally used for days and tens of days may all be omitted for this scheme. Fig. 3 shows the outputs obtained from IC_1.

Stability

The control range of R_{38} has been deliberately limited to about ±9% so that accurate setting may be achieved. The initial adjustment for any 4047 may vary by ±4% from the norm which leaves ±5% adjustment for capacitor and resistor tolerances. A metallized polycarbonate film capacitor is recommended which is superior to polyester film, and it is suggested that R_4 is a metal oxide type, selected on test, if sufficient control range is not available. The time-code 100Hz clock is required to be within about ±3% to synchronize with the incoming data. When the date code is used an overall accuracy of about ±1.8% is required. The 555 timer used in the time-decoder and the 4047 both have typical specifications of about 50 p.p.m./°C in this application.

Construction

The date decoder and display can be built on two printed circuit boards and mounted on top of the existing clock module as shown in the photograph. Five connections to the date decoder are taken fro. the edge of the seconds counter board as shown in Fig. 4. No interference has been observed on the receiver output as a result of this positioning but the supply leads should be short and kept away from the ferrite-rod aerial. Power required by the date decoder is determined by the number of segments illuminated and reaches a maximum at a current of about 180mA with 26 segments on. The total five-volt supply current of a complete clock with date display can reach about 900mA which is within the capabilities of the specified regulator i.c.

For setting up, the 4047 astable is allowed to run by linking pin 5 to +5V and R_{38} is adjusted for a frequency of 100.0Hz at TP1. A socket should be used for IC_4 because the 4047 has a different gate-oxide protection circuit which is only 30% as effective as the static discharge protection at other terminals.

The date information may be displayed as 08 01 for the 8th January or 8 1

with the leading zeros blanked by the dotted links in Fig. 2. The display drivers include a blanking input which may be taken low for this purpose. In the case of the tens of months digit, the code itself can provide the control directly but for tens-of-days, decoding of the zero condition is required using diodes D_1 and D_2. When the two bits of the tens-of-days code are both zero the diodes are in the non-conducting state and R_8 holds the blanking input low on the display. If either or both bits are high, either or both diodes conduct to enable normal display of the data.

Double recognition of the start code

The transmitted pattern of bits in the date code on certain dates may be interpreted as the start code at certain times on those dates. A simple addition to the time-decoder board will eliminate this possibility by "locking-out" re-triggering of the decoder until the end of the date sequence. A capacitor holds the output of IC_6(b) high for approximately 150ms after Q returns high at the end of the time code, as it charges via the input current of IC_6(b). It is discharged by IC_8(b) Q output going low. The track to pin 12 of IC_6 is cut and the pin is connected to the junction of the diode and capacitor as shown in Fig. 5. The diode is a germanium type for low forward voltage drop and the capacitor a tantalum bead type.

Components list

Integrated circuits		Resistors	
1-3	4015	1-3	8.2k
4	4047	4	200k
5	4029	5	100k
6	4027	6	10k
7	4001	7	220
8	4049	8	100k
9-12	4511	9	150
		10-37	390Ω
		38	47k cermet

Capacitors

1	0.01μF polycarbonate ±5%
2,5	1000pf ±20%
3	0.1μF disc ceramic
4	47μF 6V electrolytic

Miscellaneous

L.e.ds, 1 red, 1 green

Common cathode 0.3in displays. DL704 or equivalent

$D_{1,2}$ 1N916 if fitted.

Printed circuit boards

A set comprising two double sided boards and one single sided board for the date decoder/BST switch, display, and alarm circuit (to be described next month) is available for £8.00 inclusive from M. R. Sagin, at 23 Keyes Road, London N.W 2. The decoder board allows leading zero blanking, and the alarm board offers automatic cancelling after a preselected number of minutes. A set of five p.c.bs and special components are still available for the original time code clock as detailed in the August 1976 issue of Wireless World.