Getting extra control over output periods of IC timer

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The 555-type IC timer, which is a versatile circuit building block, becomes even more useful when its low and high output periods are controlled fully. The two circuits shown here, for example, enable the designer to have full-range, completely independent control over the timer's output periods, or, conversely, to make the periods fully dependent so that the output duty cycle can be varied easily over a wide range while keeping output pulse rate constant.

Circuit (a) is for independent control over the periods. Diodes D_1 and D_2 provide separate paths for the timing capacitor's (C) charging and discharging currents. Potentiometers R_1 and R_2 control the high and low periods independently over the timer's complete normal range. Resistor R_3 is included to provide the same minimum fixed resistance in the discharge loop as resistor R_4 provides in the charging loop.

When $R_1 = R_3$ and $R_2 = R_4$, a single calibrated dial can be shared by potentiometers R_1 and R_2 (through a concentric control). If $R_1 = R_2 = 10$ megohms and $R_3 = R_4 = 1{,}000$ ohms, the ratio of high-to-low or low-to-high periods can approach 10,000:1.

Circuit (b), which is only a slightly modified version of circuit (a), makes the periods dependent. As potentiometer R_1 is varied, one period is decreased while the other is increased proportionately. If $R_1 = 10$ megohms and $R_2 = R_3 = 1{,}000$ ohms, the timer's duty cycle will range from about 0.01% to 99.99%, with little change in the output pulse frequency.

In both circuits, the voltage drop across the diodes decreases the effective voltage across the RC timing network, so that the output periods will be smaller than they usually are. Normally, the timer's high output period can be described by:

$$T_{HI} = RC\,ln[(V_{CC} - V_1)/(V_{CC} - V_2)]$$

where R is the total resistance in series with timing capacitor C, V_{CC} is the supply voltage, V_1 is the low trigger threshold, and V_2 is the high trigger threshold.

For these circuits, however, the constant voltage drop across the diodes must be accounted for. If each diode drop is approximately 0.6 volt, then:

$$T_{HI} = RC\,ln[((V_{CC} - 0.6) - V_1)/((V_{CC} - 0.6) - V_2)]$$

The lower the supply voltage, then, the greater is the effect of the diode drop. When the timer is operated in its astable mode, the period is roughly 0.76RC for a 15-v supply, and for astable operation with 5-v supply, the period is about 1.4RC. This means that the timer's output periods will be more sensitive to variations in the power-supply voltage, which may be a disadvantage in some applications. □

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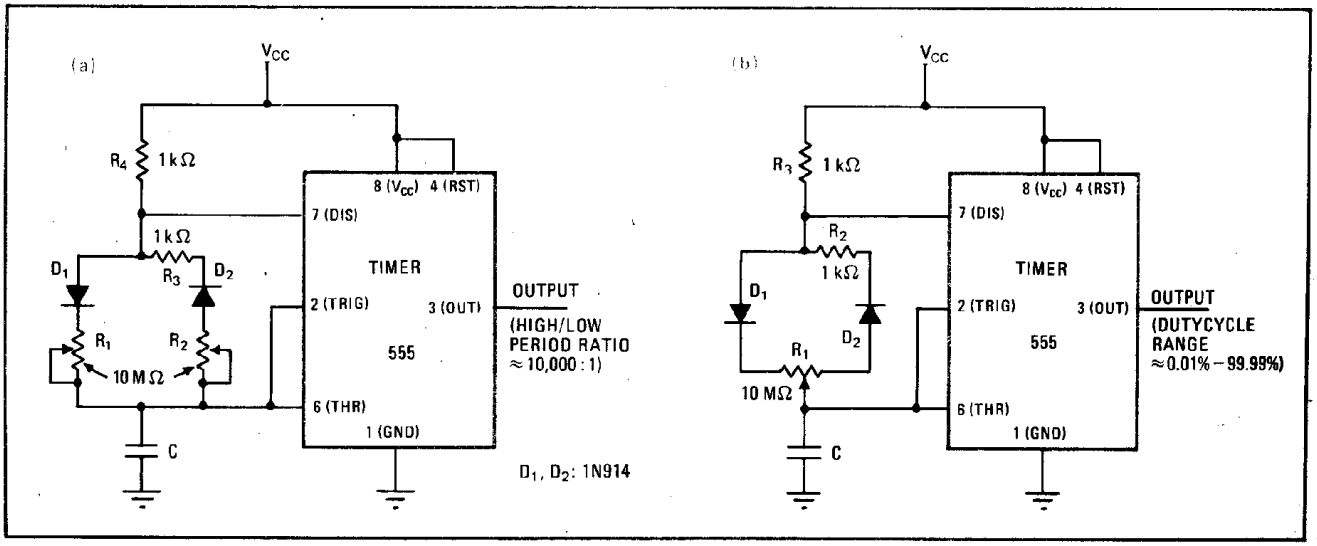

Simple but effective. When a pair of diodes is used to separate the charging and discharging paths of an IC timer, the high and low output periods of this device can be controlled easily. The periods can be made independent of each other, as in (a), or fully dependent without changing the output pulse frequency, as in (b). The diode drops, however, make the timer more sensitive to supply variations.