the IC "time machine"

BY WALTER G. JUNG
Contributing Editor

Once you understand how the 555 IC timer works, there are many fascinating projects you can build

ONE might think that the number of "standard" IC building blocks would be limited since, by definition, a standard device is one which is usable in a wide variety of applications. However, just in the last year or so, a new type of IC has shown definite signs of becoming a standard. Interestingly enough, this category of device was not represented previously by an IC specifically designed to fulfill its function. This chip is the "555" IC timer, a versatile, self-contained timing control circuit with the capability of astable (free-running) or monostable (one-shot) operation over a wide range of pulse widths from microseconds to minutes. Futhermore, it operates from a single wide-range power supply (+4.5 to +16 V), and, as another bonus, has an output current of 200 mA.

Timing functions can of course be realized by other IC techniques, such as digital or op-amp multivibrators. However, when high-current loads are to be driven or single-supply operation is a must, both of these methods can be unattractive due to the number of components required. The picture changed, though, when Signetics introduced the first IC timer, the NE555, an 8-pin commercial device with a price tag in the range of $1. The 555 has quickly established itself and is now available from a number of sources. There are also dual versions now on the market.

The usefulness of the 555 is enhanced by its impressive performance specifications. Consider, for instance, its initial timing accuracy, which is typically within 1% of the calculated value. This degree of accuracy is good for supply voltages of +5 or +15 V, since the 555 by design provides an output pulse width that is independent of the supply voltage. This means you needn't be concerned with regulated supplies to maintain stability. In addition, once it is set up, a 555 will hold its pulse width. For instance, pulse-width variation is typically only 0.005% per degree C of temperature change—which is quite stable. In

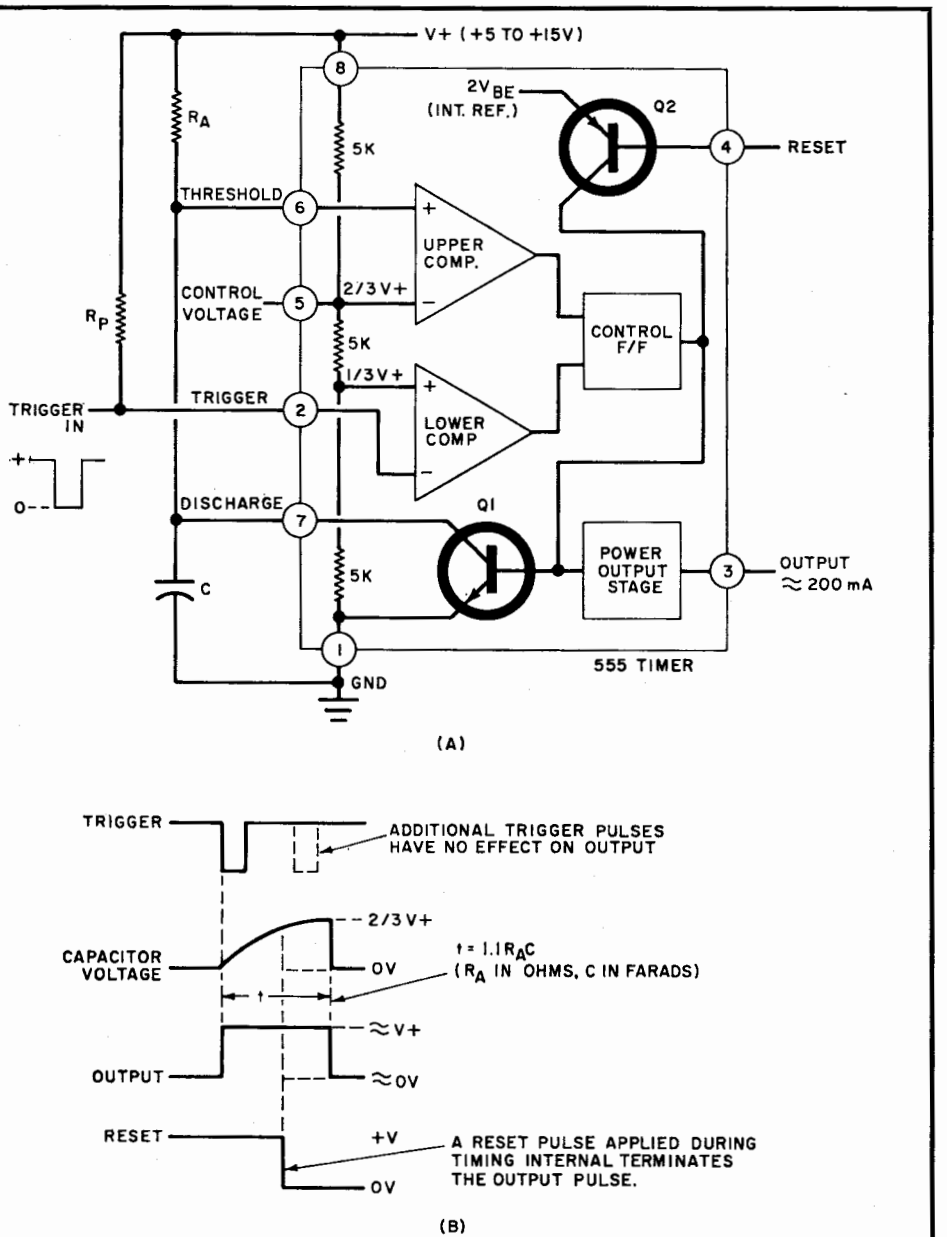

Fig. 1. Internal logic (A) of the 555 timer and waveforms (B) during triggered operation.

fact, the 555 can be considered to be temperature independent over the modest temperature environments of experimental projects. (This is true of course *if* the *R* and *C* timing components are also temperature stable.)

What Makes the Timer Tick. Knowing the basic principle of what it does, a look inside a 555 is helpful in determining how it works and how to use it most effectively. The block diagram in Fig. 1A shows the 555's functional components and its basic mode of operation—as a triggered one-shot timer. The internal circuit, while actually fairly complex, has a minimum of external connections (8 pins).

The circuit provides the functions of control, triggering, level sensing, and discharge, with a power output stage which

delivers a high-level gate (near the V+ level) for the duration of the timing interval. Yet the complete timing operation is determined by only two external components, resistor R_A and capacitor C.

Monostable Mode. In the standby state, the control flip-flop holds *Q1* on, clamping timing capacitor C to ground. In this state, the output (pin 3) is at ground level. The internal bias divider composed of three 5000-ohm resistors provides bias voltages of 2/3 V+ and 1/3 V+ to the upper and lower limit comparators, respectively. These two levels determine the voltage thresholds which, in turn, determine the timing interval.

Since the lower comparator is biased at 1/3 V+, it stays in its standby state as long as the trigger input (pin 2) is held high (greater than 1/3 V+) by R_P. When pin 2 goes low, the lower comparator sets the flip-flop, turning off *Q1*, and the output goes to its high state (near V+). Since capacitor C is now unclamped, it charges exponentially (through R_A) toward V+. After a period of time equal to $1.1R_AC$, the voltage across C reaches 2/3 V+, which is the threshold of the upper comparator (pin 6). At this time, the upper comparator resets the flip-flop, which turns on *Q1*, discharging C to zero and returning the output to the low (standby) state.

The 555 monostable timing sequence is shown in Fig. 1B. In addition to the basic operation described above, there are two other points of interest. One is that any additional input triggers (shown dotted in Fig. 1B) during the timing interval will not affect the output. That is, once triggered, the cycle will time out regardless of a subsequent trigger. Trigger pulse duration should be less than the output pulse width. This can be accomplished by differentiation, which also improves noise immunity.

A second point is that the reset function, when activated by a low-level input at pin 4, turns on *Q1* and terminates the output pulse. The output is held low as long as pin 4 is low. The use of the reset input is optional. If not used, pin 4 should be tied to V+ to avoid possible triggering from noise.

The 555's interesting feature of an output pulse width that is independent of supply voltage comes about from the fact that the timing voltage reference (2/3 V+) and the charging rate of C are both proportional to the supply voltage. Consequently, variations in the supply affect both in a manner that cancels changes in the time interval.

Note also that the upper threshold voltage is made available at pin 5. This allows external control of pulse width if desired. If this feature is not used, it is recommended that pin 5 be bypassed to ground with a small (0.01 microfarad) capacitor to prevent noise problems.

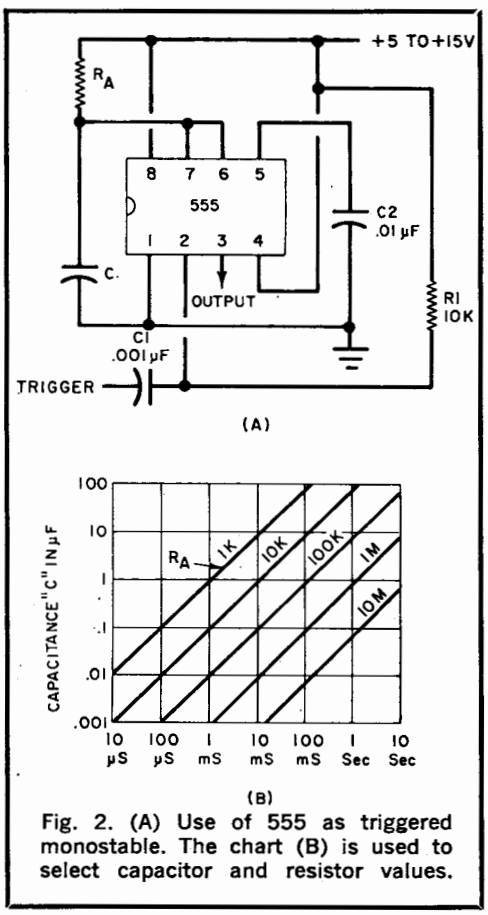

Fig. 2. (A) Use of 555 as triggered monostable. The chart (B) is used to select capacitor and resistor values.

Triggered Monostable. A triggered monostable circuit is shown in Fig. 2A. It includes the *R1C1* network, which prevents any possibility of mistriggering on positive edges. Values for *R1* and *C1* are not critical.

Values for R_A and C are selected from the timing chart shown in Fig. 2B. For best performance, there are several guidelines that should be followed concerning R_A and C. Stay within the range of resist-

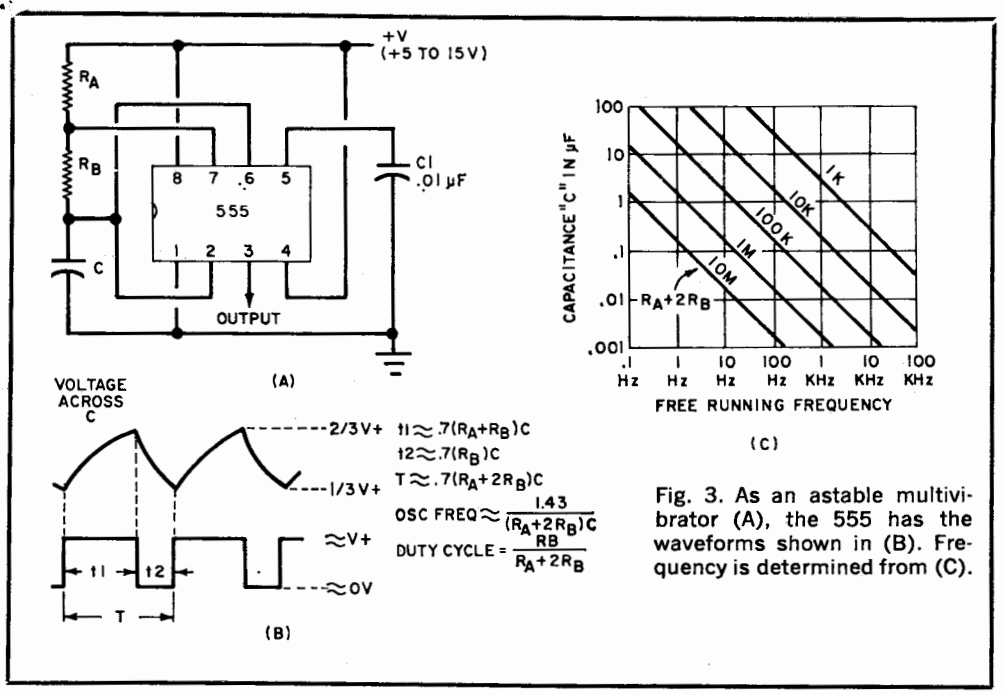

Fig. 3. As an astable multivibrator (A), the 555 has the waveforms shown in (B). Frequency is determined from (C).

ances shown, and avoid the use of large-value electrolytics if possible since they tend to be leaky. Leakage is, of course, more of a problem with long timing periods (large values of C), a "fact of life" which limits the upper range of timing. If electrolytic capacitors are necessary, tantalums should be used because of their low leakage. Voltage derating will also help minimize leakage current. With timing components of good quality, the 555 will provide accurate, stable pulses.

Astable Mode. The second basic operating mode of the 555 is as an astable multivibrator (Fig. 3A). Here the timing resistance is split into two sections, R_A and R_B, with the discharge transistor (pin 7) connected to the junction. Upon start up, C charges toward V+ through R_A and R_B until the charge reaches 2/3 V+, which triggers the upper comparator. The capacitor then starts to discharge toward ground through R_B until the charge reaches 1/3 V+, when the lower comparator triggers. This starts a new charge cycle.

The capacitor is charged and discharged between the limits of 2/3 V+ and 1/3 V+, as shown in Fig. 3B. The output state is, as before, high during the charge cycle and low during discharge. Timing equations for this mode are somewhat more complex (Fig. 3B). However, values for the resistances and capacitance can be chosen by using Fig. 3C. Since the capacitor is charged by two timing resistors and discharged by only one, the output waveform is asymetrical, not square.

Times *t1* and *t2* (and thus the frequency) are independent of V+, as in the monostable circuit.

Types and Sources. Type numbers for 555 timers from the various manufacturers are: Signetics, NE555V; National, LM555CN; Motorola, MC1455P1; Lithic Systems, LS555; Fairchild, NE555V; Intersil, NE555V. These are all single, 8-pin minidip devices.

Dual 555 units are: Signetics, NE556A; Exar, XR-2556CP; Lithic Systems, LS555-2. The Signetics and Exar devices are 14-pin dual inline units, while the Lithic Systems unit is 16-pin, with pins arranged identically to two "vertcally stacked" 555's.

The following are available from Circuit Specialists Co., P.O. Box 3047, Scottsdale, AZ 85257: NE555V at $1.25; LS555-2 at $1.80. All prices are for individual units and postpaid.

(We are planning some interesting applications and construction projects using the 555 timer chip. These will appear in upcoming issues; watch for them.—Ed.) ◈