

# DIGITAL STOPWATCH

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This digital stopwatch can count up to 99.9 seconds with a resolution of 0.1 second (or in steps of 0.1 second) or up to 999 seconds with a resolution of 1 second. This has been made possible by employing clock frequency options of 10 Hz and 1 Hz, respectively.

The stopwatch can be used to accurately measure short time intervals. It is portable and operates off four 1.5V rechargeable Ni-Cd cells.

## Circuit description

Fig. 1 shows the block diagram of the digital stopwatch. It comprises clock generator IC MM5369, quad 2-input

NAND gate IC CD4011B, presettable divide-by-'n' counter IC CD4018B, binary coded decimal (BCD) up-/down-counter IC 4510B, BCD-to-7 segment latch/decoder/driver IC 4511B and common-cathode display IC LTS543.

Fig. 2 shows internal connections and block diagram of IC MM5369, which is commonly used for generating clock pulses in digital timepieces. The MM5369 is a CMOS IC with 17 binary divider stages that can be used to generate a precise reference from commonly available high-frequency quartz crystals of

3.579545 MHz. An internal pulse is generated by mask programming the combinations of stages 1 through 4, 16 and 17 to set or reset the individual stages.

IC MM5369 advances by one count on the positive transition of each clock pulse. Two buffered outputs are available: the crystal frequency for tuning purposes and the 17th-stage output. The IC is available in an 8-lead as well as 14-lead dual-in-line epoxy package and features:

1. Crystal oscillator
2. High speed (4 MHz at 10V V<sub>DD</sub>)
3. Wide supply range of 3V to 15V
4. Low power
5. Fully static operation
6. Low current

Fig. 3 shows the circuit of the digital stopwatch. IC MM5369 (IC1) along with resistor R1, capacitors C1

PARTS LIST	
<i>Semiconductor:</i>	
IC1	- MM5369 17-stage oscillator/divider
IC2	- CD4011B quad 2-input NAND gate
IC3, IC4	- CD4018B presettable divide-by-'n' counter
IC5, IC6, IC7	- CD4510B BCD up-/down-counter
IC8, IC9, IC10	- CD4511B BCD-to-7 segment latch/decoder/driver
DIS1-DIS3	- LTS543 common-cathode, 7-segment display
LED1	- Red LED
<i>Resistors (all 1/4-watt, ±5% carbon):</i>	
R1	- 2.2-mega-ohm
R2, R27	- 1-kilo-ohm
R3, R4	- 22-kilo-ohm
R5-R25	- 330-ohm
R26, R28	- 680-ohm
<i>Capacitors:</i>	
C1, C2	- 33pF ceramic disk
C3	- 0.0022µF ceramic disk
<i>Miscellaneous:</i>	
X <sub>TAL</sub>	- 3.579545MHz crystal
S1-S3	- Miniature pushbutton microswitches
S4	- SPDT switch
S5, S6	- On/off switch
	- 14- and 16-pin IC bases
	- Nickel-cadmium cells 1.5V (4 Nos)
	- Multistrand wires
	- Solder metal
	- Suitable mounting cabinet

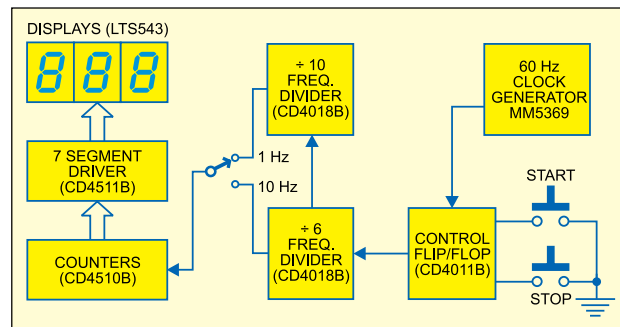


Fig. 1: Block diagram of digital stop watch

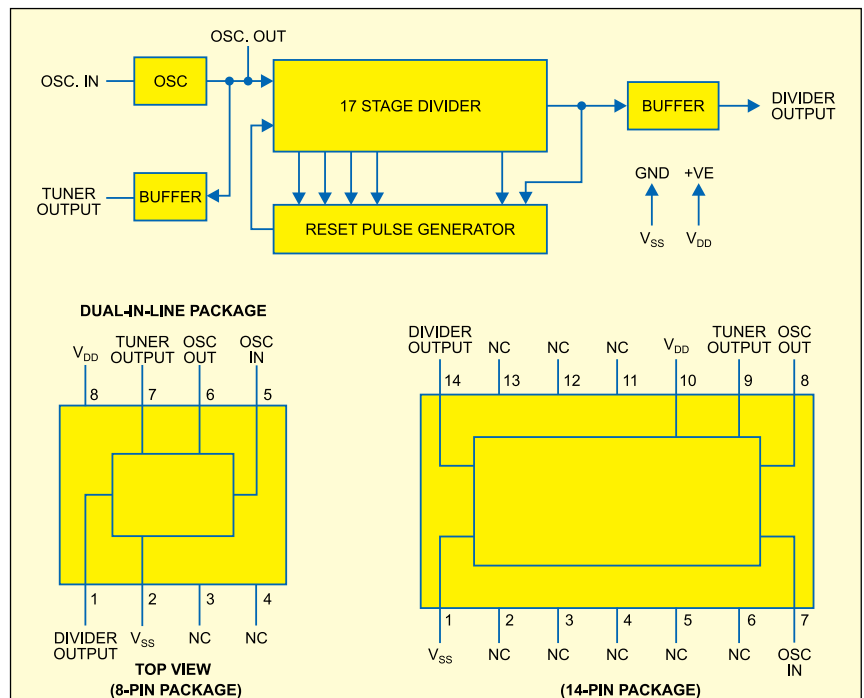


Fig. 2: Internal connections and block diagram of IC MM5369

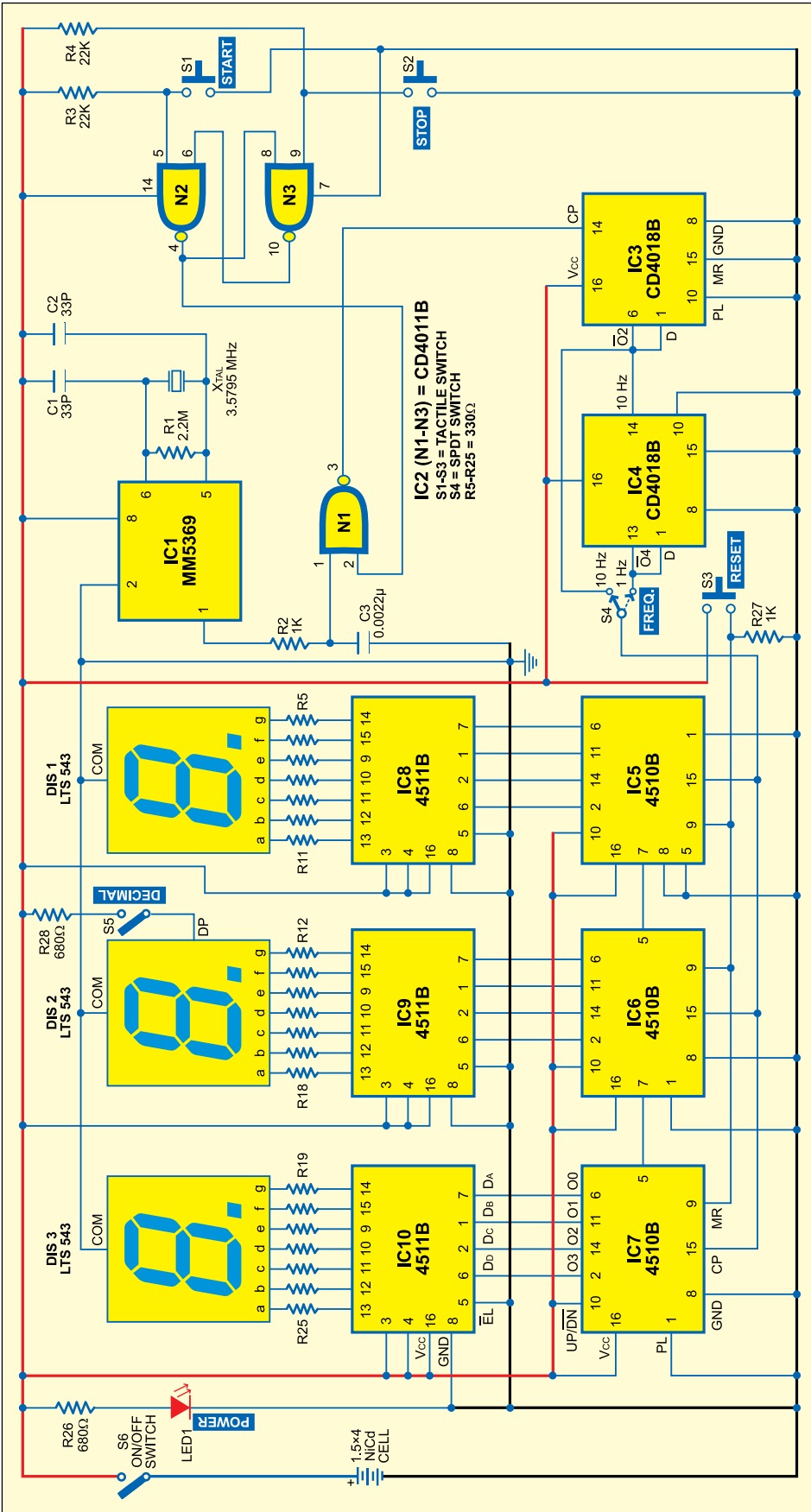


Fig. 3: Circuit of the digital stop watch

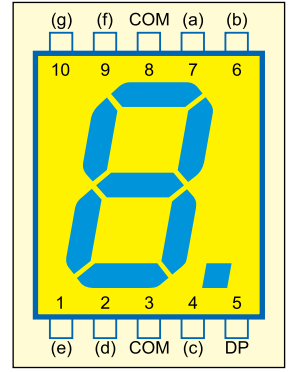


Fig. 4: Pin configuration of IC LTS543

and C2, and 3.579545MHz crystal generates a 60Hz clock signal at its output pin 1. This 60Hz clock signal is fed to IC CD4018B (IC3) via an arrangement of NAND gates.

Whenever the start switch is pressed momentarily, pin 4 and therefore pin 2 of IC CD4011B (IC2) goes high to enable NAND gate N1 and the clock signal is passed onto IC CD4018 (IC3). When stop switch S2 is pressed momentarily, NAND gate N1 is disabled due to pin 4 of IC2 going low and the clock pulses don't reach IC3.

IC3 and IC4 (each CD4018B) are presettable divide-by-'n' counters, where 'n' could be 2, 3, 4, 5, 6, 7, 8, 9 or 10. IC3 has been wired as a divide-by-6 counter by feeding its O2 output back to data input pin 1. IC4 has been wired as a divide-by-10 counter by feeding its O4 output back to data input pin 1.

For 60Hz clock input, IC3 outputs a 10Hz clock signal. This clock signal is fed to IC4 and it outputs a 1Hz clock signal. Switch S4 is used to select the required frequency.

IC5, IC6 and IC7

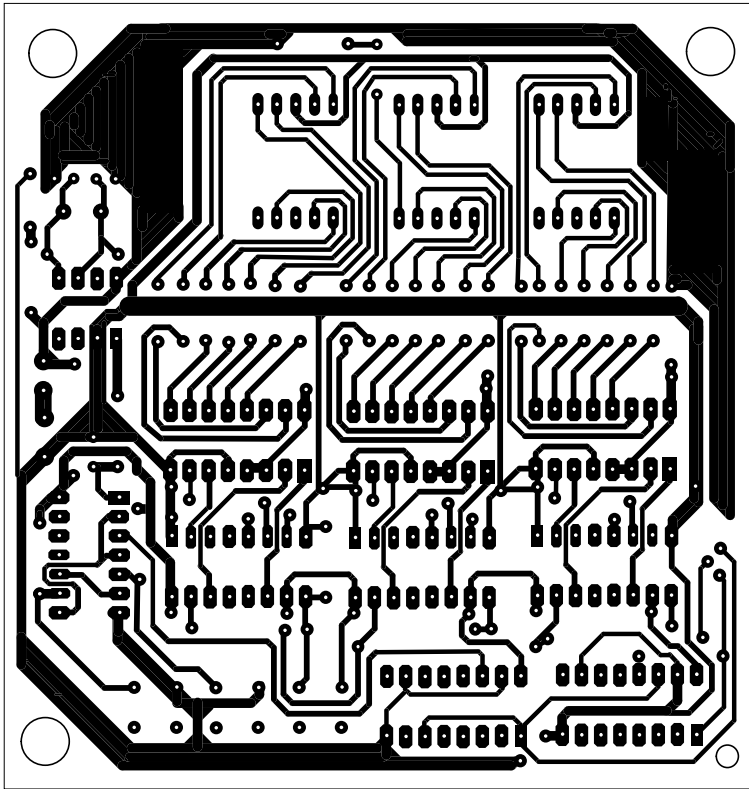


Fig. 5: Actual-size, single-side PCB layout for the digital stop watch

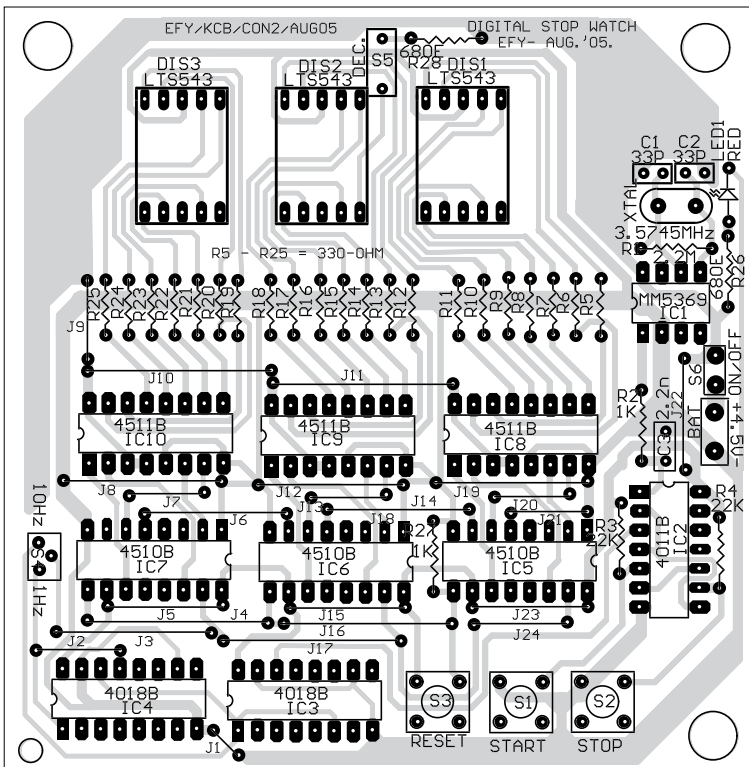


Fig. 6: Components layout for the PCB

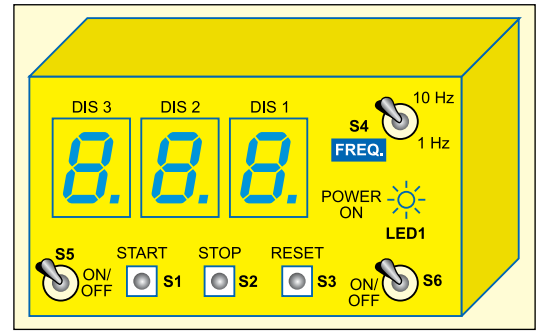


Fig. 7: Proposed display panel box

(each CD4510B) are presettable up/down BCD decade counters. These counters are connected in a cascade arrangement and can count up to 999 clock pulses. Therefore, when fed with a 1Hz clock, the maximum time delay achieved between start and stop operations is 999 seconds. Similarly, when the clock frequency is chosen to be 10 Hz and decimal-point switch S5 is flipped to 'on' position, the maximum attainable time delay is 99.9 seconds.

Reset switch S3 can be used to reset the counter to all zeros before start. Usually, the reset terminal is connected to ground via resistor R27. It is connected to +5V when you momentarily press reset switch S3 to reset the counter.

IC8, IC9 and IC10 (each CD4511B) are BCD-to-7-segment latch/decoder/driver ICs. These can directly drive 7-segment, common-cathode LED displays.

DIS1, DIS2 and DIS3 (each IC LTS543) are 7-segment displays of common-cathode type. Pin configuration of IC LTS543 is shown in Fig. 4. R5 through R25 are current-limiting resistors.

## Construction

A single-side, actual-size PCB for the digital stopwatch is shown in Fig. 5 and its component layout in Fig. 6. The proposed display panel box is shown in Fig. 7. All the 7-segment displays, LED1 and switches are mounted on the front panel. ●