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ACCURATE TIMEBASE FOR DIGITAL ELECTRONIC CLOCKS

Inexpensive circuit maintains digital counting automatically when power is lost.

IF YOU OWN a digital clock, its likely you expect it to maintain extremely high accuracy, especially if it displays seconds. Digital clocks, however, have a special problem not found in the ordinary electromechanical clock.

The problem is caused by a momentary power outage, lasting a second or two, that may occur at any time of the day or night. This outage may be brief enough to produce only a flicker of the display, yet brief as it is, the clock's digital counter circuit can generate a timing error. An electro-mechanical clock will integrate the outage and the clock dial may skip a second or so, with no real harm done.

The timebase described here is designed to overcome the problem in digital timekeeping and, in doing so, virtually eliminate the inaccuracies commonly encountered.

Power Line Vs. Crystal. If the ac power-line frequency is measured at any given instant, its frequency might vary from exactly 60 Hz by as much as 0.03%. This is the accuracy over the short term. The long-term accuracy, however, is actually much better than this by several magnitudes, as we shall see. A digital clock powered from a hypothetical glitch-free, uninterrupted commercial power line might show an error of only two or three seconds a year. Since there are 3.15×10^7 seconds in a year, this works out to an accuracy of better than ±0.00001%, a far cry from the ±0.03% specified.

This seeming paradox is resolved by the fact that the power-line frequency is periodically corrected to a frequency standard so that its long-term average frequency is maintained close to exactly 60 Hz.

Unlike an electromechanical clock whose mechanical inertia makes it extremely forgiving of glitches and transients, a digital electronic clock depends upon an uninterrupted, glitch-free timebase. Interrupt the timebase, even momentarily, and the clock loses its count. This is why filters and a large filter capacitor cannot do a complete job of maintaining accuracy during momentary power dropouts. Fast transients can be attenuated and the operating dc voltage can be maintained but there is no way to maintain the 60-Hz counting line frequency when power is interrupted.

The glitch problem is severe and has prompted many designers to turn to the crystal-controlled timebase. The crystal timebase, contrary to popular belief, is not a perfect cure for the problems mentioned above. Most crystals available to the hobbyist have rated accuracy of ±0.001% to ±0.005%, which is better than the short-term accuracy of the power line but nowhere near its long-term accuracy. Also, over the long haul, all crystals age. Hence, unless a crystal timebase is periodically recalibrated, this slow frequency drift adds to decreasing accuracy. Needless to say, going to a crystal timebase provides glitch-free operation and improved short-term accuracy but at the expense of greatly deteriorated long-term accuracy.

The low-cost Digital Clock Timebase, shown in Fig. 1 wired to part of a typical digital clock, uses the best of both techniques to meet all our requirements for an ideal timebase. It uses the power-line as the primary timebase for long-term accuracy. When a glitch or power outage is detected, two things occur. First, there is a rapid transfer to a crystal-controlled 60-Hz standby timebase, which takes over for the duration of the glitch. Second, smooth transfer is made to battery backup power when the power-supply filter capacitor in the clock can no longer support the system. The circuitry that does all this is low-power CMOS for minimum battery drain.

How It Works. The two functions of the timebase are shown in Fig. 1. When the clock's +V supply drops low enough to forward bias *D2*, rechargeable backup battery *B1* smoothly takes over. Battery *B1* also supplies V_{DD} for the standby timebase. The useful charge of the battery is extended if the clock's display and other nonessential loads are blanked when operating from the battery. Diode *D1* isolates these loads so they operate only from the clock's built-in power supply.

During a momentary power outage, the filter capacitor may not discharge to the transfer point immediately. Since the power-line counting frequency is lost for the entire duration of the outage, a faster way to sense power outages must be used, a function provided by *IC2*.

Retriggerable monostable multivibrator *IC2* is configured as a missing-pulse detector whose output pulse width (at pin 7) is set for 20 ms or slightly greater than the period of the 60-Hz line frequency. The detector is triggered once at the beginning of each cycle by the differentiated output of Schmitt trigger *IC1A*. Input to the trigger is the same 60-Hz primary timebase input to the clock IC. Since the detector cannot time out, its output remains low, keeping gate *IC1B* disabled. The output of gate *IC1B* is inverted by *IC1C*, sending a logic 0 to the OR gate.

During a glitch or other power outage, the line frequency, (and, hence, the retrigger pulse) lapses. Detector *IC2* is now free to complete its cycle to time out 3.3 ms after *not* receiving a retrigger pulse. Its output then goes high and enables *IC1B* to apply the standby *IC3* crystal-controlled 60-Hz timebase to the clock.

Crystal-controlled oscillator/divider *IC3* continuously generates 60 Hz from a commonly available 3.58-MHz color-TV oscillator crystal. When enabled by the detector, *IC1B* gates the standby timebase to the high-level OR gate made up of *D3*, *D4*, and *R5*. Either the high-level half-sinusoid primary timebase or the CMOS-level square-wave standby timebase is then gated to the 50/60-Hz input of the clock IC.

When primary power returns, almost a reverse action occurs. As the filter capacitor in the clock recharges, it again crosses the transfer point. Then the glitchless transfer is back to the power supply. The primary timebase, rising in step with the filter capacitor voltage, is gated to the 50/60-Hz input of the clock IC and to detector *IC2* via Schmitt trigger *IC1A*. The detector output immediately goes low, disabling gate *IC1B* to remove the standby timebase.

Construction. The timebase is best assembled on a printed-circuit board,

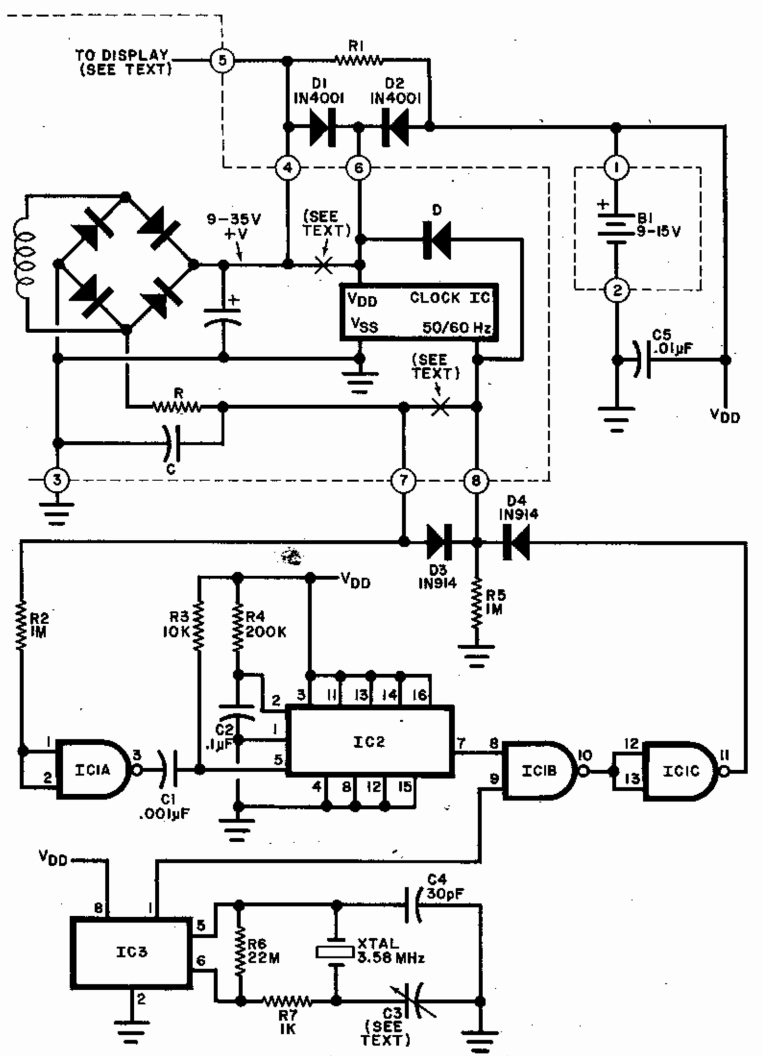

Fig. 1. In power outage, digital counter and rechargeable battery power supply automatically take over.

PARTS LIST

B1—9-to-15-volt rechargeable battery (see text)
C1—0.001-μF, 50-V disc ceramic
C2—01-μF, 50-V Mylar
C3—20-pF, 50-V disc ceramic or 10-40-pF trimmer, see text
C4—30-pF, 50-V, disc ceramic
C5—0.01-μF, 50-V, disc ceramic
D1, D2—1N4001
D3, D4—1N914
IC1—4093B Schmitt trigger
IC2—MC14538B dual monostable (Motorola)
IC3—MM5369 oscillator/divider (National)
R1—see text
R2, R5—1-megohm, ¼-W resistor
R3—10,000-ohm, ¼-W resistor
R4—200,000-ohm, 5%, ¼-W resistor
R6—22-megohm, ¼-W resistor
R7—1000-ohm, ¼-W resistor
XTAL—3.58-MHz, color-TV oscillator crystal
Misc.—IC sockets or pins, battery holder, etc.

Note: The following is available from CM Circuits, 22 Maple Ave., Lakawanna, NY 14218: etched and drilled pc board at $3.25, plus $0.50, postage and handling. New York state residents, please add sales tax.

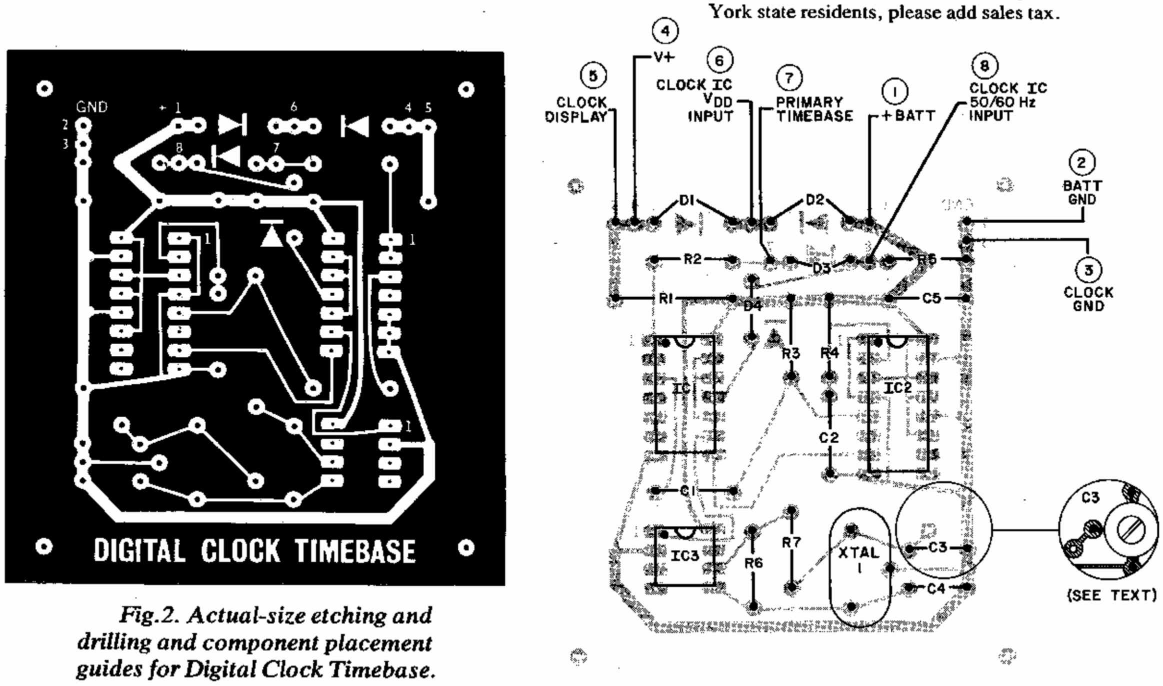

Fig.2. Actual-size etching and drilling and component placement guides for Digital Clock Timebase.

but other wiring methods can be used. Illustrated in Fig. 2 are both the etching-and-drilling and component-placement guides. Sockets for the ICs are optional but highly recommended. The circled numbers in the schematic correspond to input/output points on the pc board.

The value of *R1* to be used in your system is calculated by Ohm's Law. For example, suppose your power supply has an output of 25 volts and you have previously determined that a 12-volt nickel-cadmium-cell with a capacity of 0.5 ampere-hour (AH) will do for backup. The battery is trickle-charged at a hundredth of the rated battery capacity, which in our case is 5 mA. Using the formula (power-supply voltage minus battery voltage) divided by (desired charging current plus standby timebase operating current), we obtain (25 - 12)/(0.005 + 0.0025), or 1733.3 ohms. You would then use an 1800-ohm (nearest standard value) resistor for *R1*. Determining the power rating of *R1* by I^2R reveals that a standard 1800-ohm, 1/4-W resistor will do nicely.

When selecting the backup battery to be used, keep in mind that many clock ICs will keep time at a lower potential than the minimum operating voltage specified on the data sheet as long as the display is not driven. (Mount the battery off the pc board.)

Installation. In the typical digital clock shown in Fig. 1, the clock chip's 50/60-Hz timebase input is usually filtered by RC and clamped to V_{DD} by diode *D*. Break this line as shown and wire it to gate input 7. Wire gate output 8 back to the 50/60-Hz input of the clock IC. Note that the timebase will keep accurate time only for 60-Hz systems.

The +V output from the filter capacitor usually drives all circuitry directly. Break this lead as shown and wire it to gate input 4. Reroute the display and other nonessential wiring to gate input 5. Wire gate output 6 back to the V_{DD} inputs of the clock IC and other essential circuitry.

Calibration. The accuracy of the crystal is usually much greater than the instantaneous accuracy of the 60-Hz line frequency. For most purposes this accuracy will suffice, but for those who want a more accurate calibration and have access to an accurate frequency counter, the oscillator frequency can be trimmed to exactly 60 Hz. Replace fixed capacitor *C3* with a 10-to-40-pF trimmer capacitor and adjust until pin 1 of *IC3* shows exactly 60 Hz on the counter. ◇