Principles of Logic Analysis — 2

In this second of our short series of articles on the basic principles of logic analysis, we first look at the conventional measuring instruments which can be used in logic circuits, and their suitability. Then we look at logic analysers, and the way they work.

by WOLFGANG SCHUBERT

To begin this month, let us first consider the various measuring instruments which can be used in logic circuits and their suitability for the various measuring problems.

Voltmeter

In the digital field, a voltmeter can only be used for the measurement of supply voltages and static signals because the response of the voltmeter is far too slow to register brief changes in signals.

Oscilloscope

In addition to the measurements possible with a voltmeter, an oscilloscope can be used to analyse repetitive processes. Level errors can be detected using an oscilloscope. A multi-beam oscilloscope can be used to provide quantitative information on the timing relationship of signals.

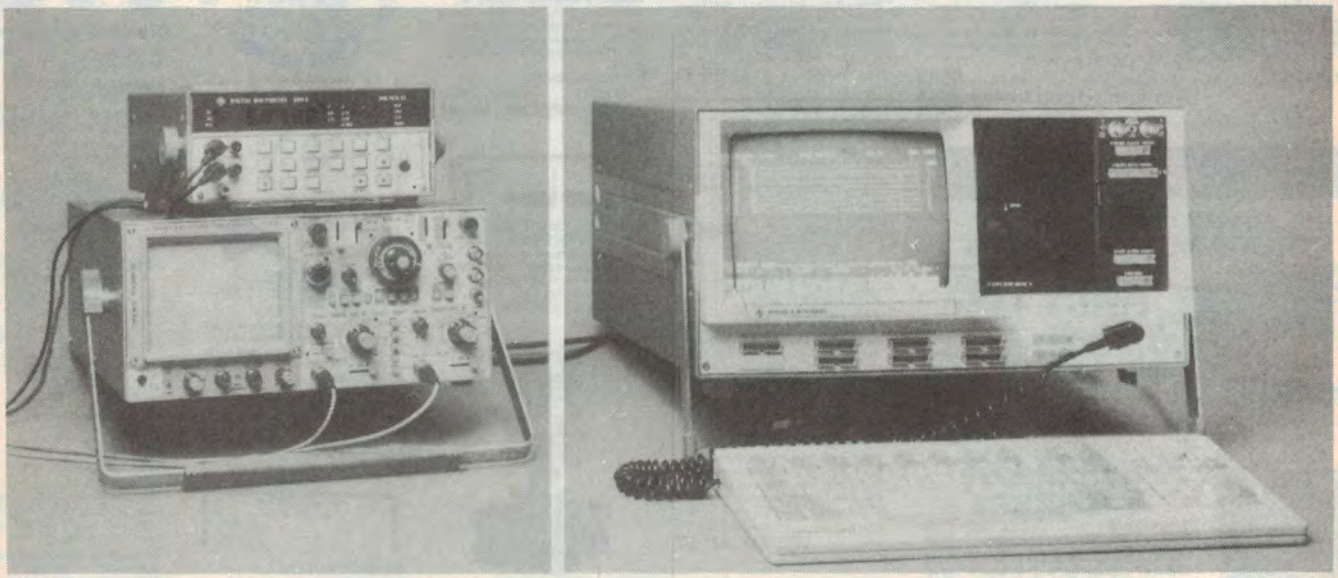
Before an oscilloscope can be used successfully with such types of measurements, it is necessary for the examined processes to be periodic since a stationary oscillogram cannot otherwise be obtained. The use of storage oscilloscopes to analyse single events is usually difficult because the oscilloscope triggering must be set "blind" in the case of single or seldom events and the measurement may have to be repeated very often before a meaningful oscillogram is obtained.

Development system with in-circuit emulator

The in-circuit emulator of a development system replaces the CPU in a microprocessor circuit and enables the CPU program to be executed step-by-step, with a view to gaining an insight into the internal processor registers as well as the external memories and peripherals connected to it.

Many users believe that they do not require a logic analyser if they use an in-circuit emulator for test purposes. This is not correct, for several reasons:

- This means for filtering out relevant sections of the program using an in-circuit emulator are very limited compared to the possibilities offered by a logic analyser.



Conventional test instruments like a voltmeter or oscilloscope (left) are of limited use in checking logic circuits. A logic analyser like that at right is much more suitable.

The LAS logic analyser system from Rohde & Schwarz, capable of both state and timing analysis as required.

• Many in-circuit emulators do not operate in real-time. Errors which only occur at the full operating speed cannot be detected by them.

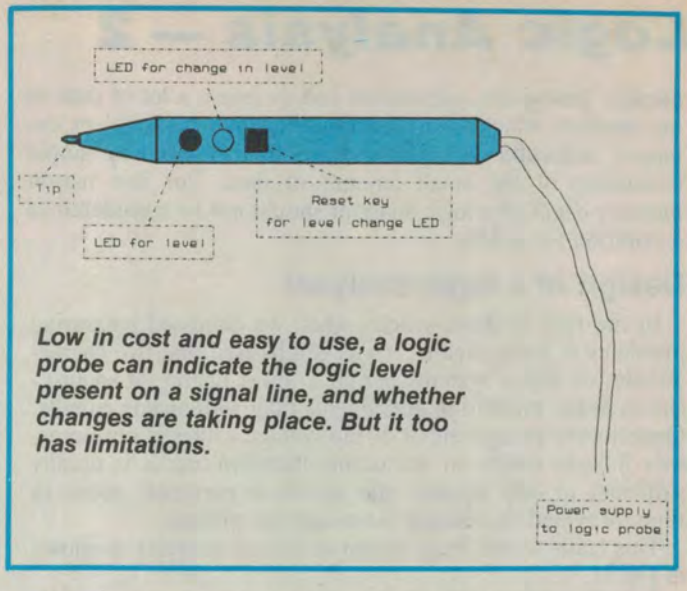
• The in-circuit emulator replaces the microprocessor and therefore only "sees" events which can be detected by the processor. Faults in the peripheral units connected to the circuit cannot be detected.

It is often only possible to detect the *effects* of hardware malfunctions, but not the causes.

Example: Because of a fault in the address decoding for the memory modules of a microprocessor circuit, all write events of the microprocessor are simply lost instead of entering the addressed RAM location. The in-circuit emulator can no longer read the supposedly written cell; the fact that it was not even physically addressed remains undetected.

Logic probe

The logic probe is a very useful instrument for answering elementary questions in logic circuits: what is the level of a signal line and has this line changed its level at some time? But it is obviously not suitable for more detailed measurements.



Low in cost and easy to use, a logic probe can indicate the logic level present on a signal line, and whether changes are taking place. But it too has limitations.

Of the measuring problems mentioned in the previous article, the following cannot be solved satisfactorily using the previously mentioned instruments:

• Simultaneous monitoring of a large number of test points.
• Analysis of discontinuous events
• Analysis of single events

These tasks, and many more, can be solved using a logic analyser. The principle and mode of operation of logic analysers will now be explained.

Objective: data reduction

Each digital system can be considered as a data source which continuously outputs data during operation. These data are usually present at the same time as a clock: such circuits are referred to as synchronous circuits.

In order to obtain information on whether a system is functioning correctly, the data can be tested to see whether they correspond with the values expected for intact systems. This method of direct comparison between a good circuit and a circuit of the same type is often used with automatic test setups but can no longer be considered if no "good" circuit is available as a reference or if more information is required than simply Go/Nogo.

A different method is used in logic analysis. The required result can be considered as a bit which is then zero if the circuit does not function, and one if it functions correctly. The function of the logic analyser then becomes a data reduction function: the data flow, which can be of any width and basically of unlimited duration, output by the device under test is to be reduced according to criteria set by the user to generate the "bit" which provides information if the circuit is operating correctly or not.

This data reduction takes place in two steps: during the data acquisition stage, parts of the unlimited data flow are filtered out and stored if they are relevant to the information concerning correct functioning.

There are two possibilities for data evaluation:

• The stored data are displayed in such a manner that the user themselves can easily generate the Go/NoGo bit. This could be referred to as "user-based postprocessing".

• The stored data are processed in the logic analyser by intelligent evaluation programs and the information concerning correct functioning appears directly on the monitor.

Two procedures to generate the "bit" are conceivable, because data reduction takes place in two steps: a limited re-

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duction during data acquisition and therefore a lot of data in the analyser which may then be difficult to evaluate, or extensive reduction during data acquisition followed by simple evaluation of the small amount of data. For this reason *memory depth* of a logic analyser should not be considered as a criterion for quality.

Design of a logic analyser

In the first of these articles when we discussed measuring problems of logic circuits, it was emphasised that two characteristics of digital systems permit a lower degree of sophistication in the measuring instruments than with analog circuits. Quantitative measurement of the voltage values is not necessary if level errors do not occur. Furthermore, it is usually sufficient to only monitor the signals at particular points in time, provided that timing errors are not present.

This leads to the basic design of a logic analyser as shown in Fig.11.

A logic analyser consists of a memory, a sequence controller, a clock generator, a computer, a display (screen) connected to the computer and external data and clock probes via which the device-under-test is connected. The probes are comparators programmed to the thresholds of the logic family to be analysed and therefore only output the information HIGH or LOW.

Data are applied from the data probes, to the memory if a clock signal occurs and if the sequence controller requests this. The clock may come from the device-under-test itself (external clock) or from the clock generator in the logic analyser (internal clock).

The sequence controller is a circuit programmed by the computer prior to recording according to inputs made by the user. It monitors the input data and requests the memory to accept data. At the end of recording, the data collected in the memory are evaluated by the computer and displayed.

Differences between logic analysers and oscilloscopes

Fig.12 shows, using an analog signal sequence for illustration, how the simplifications of the actual signal sequence during storage in the logic analyser, namely the division of

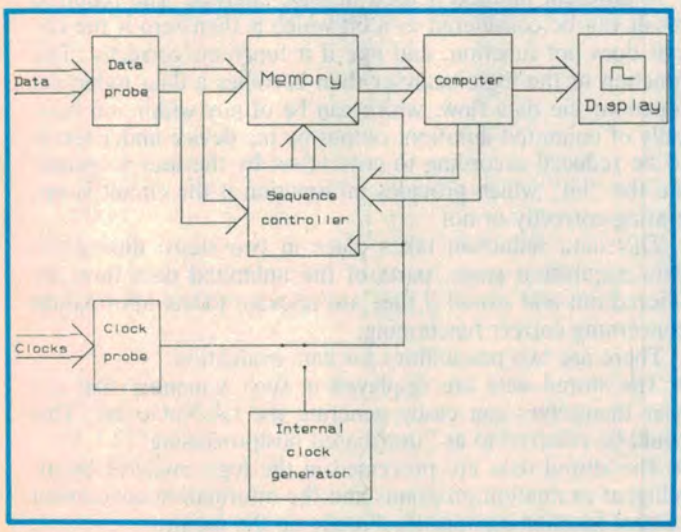

Fig.11: The basic design of a logic analyser. Data is strobed into a memory, analysed and displayed.

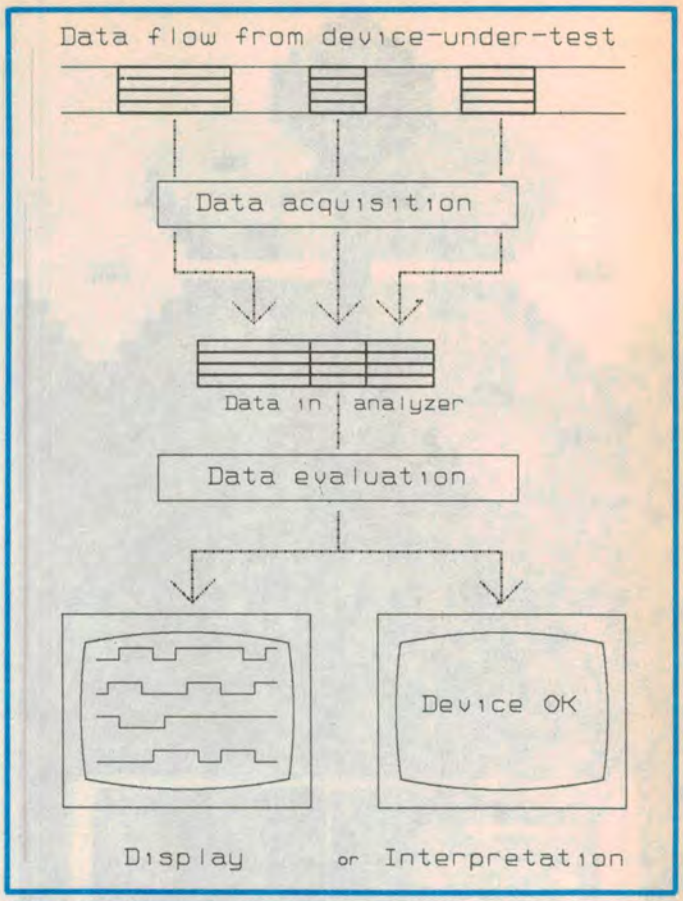

Fig.10: Logic analysis consists essentially of two stages of data reduction; one during the acquisition of data, the other during its evaluation.

the levels into LOW and HIGH and the acquisition of these levels at discrete points in time, have an effect on the display.

The top curve shows the actual analog signal and how it would be displayed on an oscilloscope. This signal is applied to the data probe of the logic analyser. If the set threshold is 0 Volt, the level-discrete signal shown in the centre results at the input to the logic analyser memory.

This signal is only applied to the memory when a clock occurs. The result is a level-discrete and time-discrete signal present in the memory as a sequence of "0" and "1".

Conversion of this sequence into a timing display results in the bottom curve: the integral between the signal edges can no longer be reconstructed and may therefore be incorrect by up to one period of the clock.

Logic analyser families

It is easy to see that the timing accuracy of the signal reconstructed during evaluation from the stored data is improved if the clock frequency used for sampling is increased. The time interval between two signals can only be determined sufficiently accurately if sampling takes place several times within the interval.

The tendency in logic analysers is therefore towards higher and higher sampling frequencies. However, such high frequencies result in problems in the implementation of the memory and the sequence controller which then have to be designed using fast, expensive technologies such as ECL (emitter coupled logic) which also have high current drain. The costs also increase with the number of channels measured.

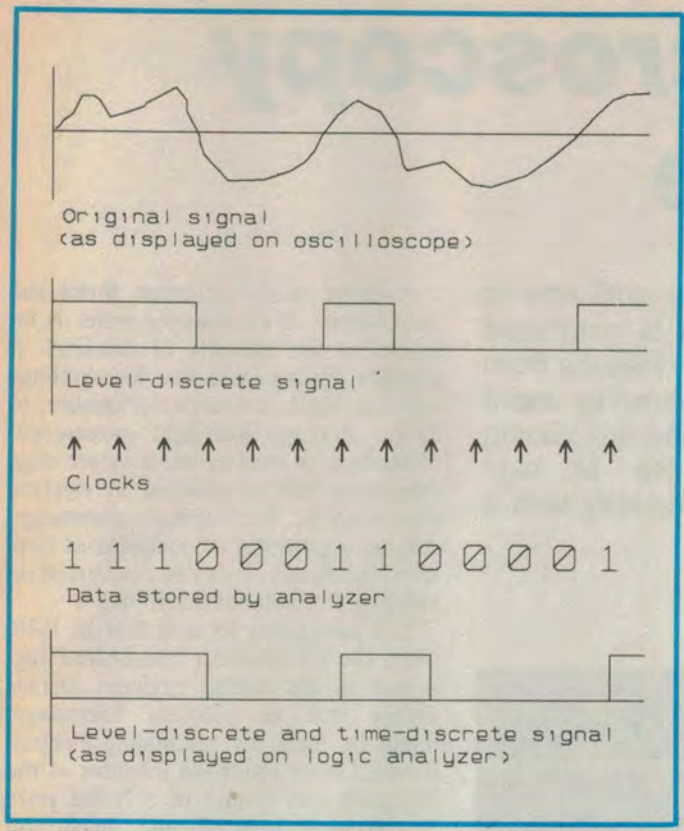

Fig.12: A logic analyser does not store or display an analog facsimile of the original signal, but a simplified logic level-discrete and time-discrete version.

Characteristics of the analyzer families

	Timing analyzer	State analyzer
Number of data channels	few (≤ 24)	many (≥24)
Highest sampling frequency	large (≥ 100MHz)	small (≤ 20 MHz)
Memory size	large (≥ 1 kbit)	small (≤ 1 kbit)

These factors have resulted in two families of logic analysers:

State analysers with a large number of channels, a low limiting frequency and a larger trigger intelligence are usually operated using an external clock obtained from the device-under-test. They are primarily used to determine state errors.

Timing analysers on the other hand have a higher limiting frequency and — for economical reasons — a lower trigger intelligence and a smaller number of channels. If the sampling rate is high enough, they can be used to trace timing errors and to measure delay times between signals.

Example: The 100MHz analyser LAS-B1 in the Logic Analysis System LAS from Rohde & Schwarz.

Table 2 shows a summary of the basic characteristics of the two families of logic analysers.

In the next article we will look at the way logic analysers are used in practice.

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