Feedback Phase to Face

Part IV

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Unlike the positive feedback blocks seen so far, regeneration forces both the sections to go into conduction. Once it reaches the state of conduction, it is no longer a slave of gate signal. The system latches on to a new state and remains there as long as the system is uninterrupted. It can be reverted into its original state only by cutting off the source of energy which helps in sustaining the life of the system. The negative slope portion of the current voltage characteristics is the result of positive feedback and its successive amplification, which eventually leads to short circuiting or shunting action of the device.

The process of relaxation is based on the return of the state of a system to its original condition after a brief disturbance. The disturbance may be external or may be due to feedback generated within the system itself. The system is liable to absorb the command and succumb to it. It can assume only one of the two specific states.

The periodicity between the active and passive states can be controlled externally. In fact, the input of the system can only be of importance in overturning a given state. Thus if the output information is to have some meaning, it is ıperative that the input also should have a predictive ature. The system accomplishes this action, subject to practical limitations, in absolutely regenerative positive feedback within itself. It can be thought of as a system that has two quasi-stable states of equilibrium, in each of which the operating parameters change slowly until critical values are reached at which transition takes place very rapidly to the other state.

The useful properties of relaxation devices include their ability to generate non-sinusoidal waves of desired form which are rich in harmonic contents. Such devices have susceptibility to tuning and modulation by means of a direct voltage and can be synchronised to a frequency approximating a multiple or sub-multiple of the frequency of oscillation of the circuit.

Delayed feedback of appropriate magnitude is the secret of square wave and pulse oscillators. Perhaps the term 'gain' is never fully proper for use with reference to these systems.

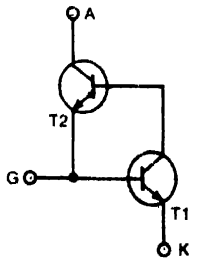

Fig. 25: Schematic configuration of a SCR.

While avoiding the term gain or amplification, it is still possible to state some characteristics of the typical relationships between input and output magnitudes for signals in typical reflexes.

The reciprocal feedback system shown in Fig. 26(a) is called a multivibrator. The feedback is delayed by a factor of fixed magnitude to improve its intelligibility and the delays in both the branches may not be identical. As might be imagined, reciprocal feedback systems are not complex. One unit is interested in the lateral inhibition of the other. Two inhibitory actions are followed by two sign changes in

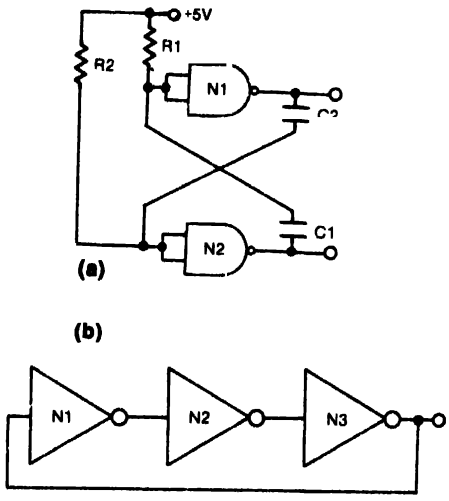

Fig. 26(a): Multivibrator using NAND gates. (b) The reciprocal feedback system using inverter gates.

any signal as it passes round the loop. Perhaps it does illustrate a serious point. The system has a positive feedback but it differs from a simple feedback system by the fact that it has two inputs and two outputs. The loop gain is high and a threshold occurs in the pathway.

The best known temporal effects are produced by simple delays. One class of operations which modifies signals is the alternation of temporal relationships in the signals. Delay of one signal can provide a temporary storage of that signal which allows it to interact with a large signal. The system relies on positive feedback. Temporary storage of information lasts only for a definite multiple of the delay factor.

It follows from all this that the amplitude is independent of frequency. Consider, for example, an odd linear combination of inverter gates where the output is tied back to the input of the chain. The output remains oscillatory as a consequence of the propagation delays introduced by each gate and it does not wait for a separate control input. Assuming that all the gates have approximately equal propagation delay, the time period of oscillation equals '2tn', where 't' is the propagation delay and 'n' is the number of inverter gates (odd) employed in the system.

Negative resistance devices that have more than one stable states are the cornerstones of digital memory. In the first place, they are completely non-reactive at all frequencies

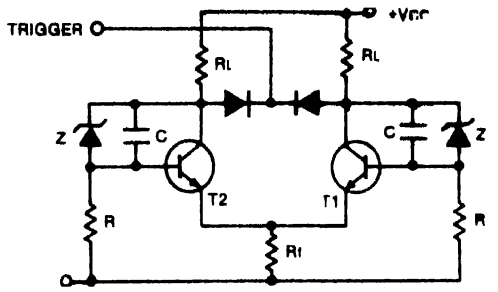

Fig. 27: Schematic showing Eccles-Jordan bistable circuits.

which means that in an ideal case there is no circuit capacitance or inductance. This requirement is obviously almost impossible to fulfill because in any physically attainable circuit, there are always shunt capacitance and series inductance.

Secondly, the states can be made completely symmetrical. A symmetrical circuit has equal magnitudes of currents and voltages in the possible stable states of equilibrium and each respond identically to the external commands that switch it from one state to another.

Eccles-Jordan bistable circuits (Fig. 27) apparently arose from the feature of positive feedback between the systems and their mutual inhibition cum dominance. The active state of T1 also means the passive state of T2 and vice versa. The reduction of positive feedback or the introduction of negative feedback is partially prevented by the presence of capacitor C across the zener. These capacitors cannot charge or discharge instantaneously on the arrival of the command signal.

Rapid changes of collector voltage of one active device

Break Frequency

The frequency where the magnitude of an output voltage or current has dropped to 0.707 of its mid-frequency value is called the break frequency. The basic reason for the selection of this unusual number is that for a sinusoidal wave its RMS (root mean square) value is equal to 0.707 times its maximum value, i.e. 0.707 is approximately equal to the reciprocal of crest value.

The crest value for sinusoidal waves is equal to 1.414, which is the square root of 2. The relationship between the RMS value and maximum value is specified in terms of current by the equation

$$Im^2 = 2\ I^2RMS$$

For a wave of any form, the ratio of maximum to RMS value is called the crest, peak or amplitude factor.

The break frequency is also known as 0.707 frequency or the band edge. The significance of 0.707 frequency is a more apparent with a resistive load to the amplifires of where the output power will be dropped to 0.5 (the square of 0.707) of its mid-frequency value. Base locked break frequency. That is why the break -pted for their often termed as 'half power frequency' width modulated ratio of 2 is approximately equal to along with thyristors is break frequency is also known as the power supplies.

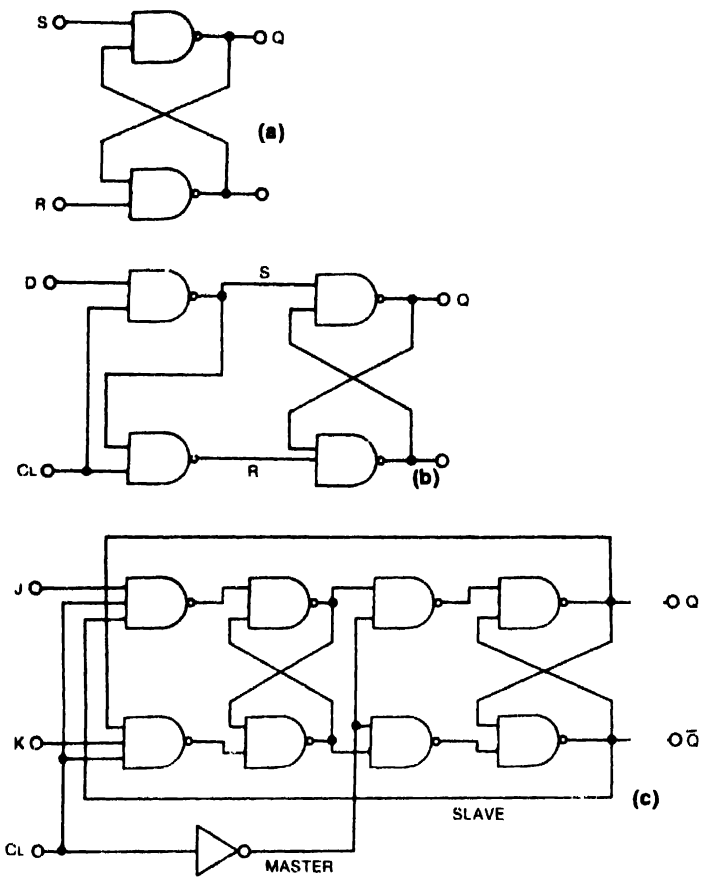

Fig. 28(a): Simple RS flip-flop using NAND gates. (b) Incorporation of gates in RS flip-flop. (c) The master-slave JK flip-flop.

during its transition are reflected on the base voltage of the other active device. Speed-up capacitors, as they are often called, ensure that transistors conduct alternately when the successive command pulses are used to trigger the circuit. Maximum open loop gain and hence a high speed transition between the states is made possible by the zener diode, which practically forms an open circuit if the collector voltage is held below its breakdown level.

The multiple feedback system, an even more common deviation from simple feedback systems, is found to be more effective in storing bits of previous information. Clearly, these are multi-input/output systems and the interaction between the inputs, whether it is derived from the external source or from the output of the system itself, will determine its current status. Delay in the positive feedback path may be equal to zero or an integral multiple of the delays of input signals

A simple set/reset flip-flop has two basic blocks, mutually monitoring individual outputs so that their states can be controlled upon the external commands. The delay involved in the process of feedback is close to zero. Various forms of flip-flops such as data, toggle, master-slave JK etc employ similar strategies where delay is made a function of the input signal itself. Note that the behaviour of the circuit is different depending upon the relative magnitudes of the delays. This may give rise to a phenomenon called 'critical race.' It should be noted that logic '0' applied to S and R inputs simultaneously in a NAND flip-flop is a disallowed input condition since it produces an invalid output state with both the outputs at logic '1'.

In applications such as memories, it is necessary to remember what the logic state of a single input has been, even after the input has subsequently changed. An additional gate technique is adopted in S/R flip-flop to isolate the data input from the flip-flop after the desired data have been stored (Fig. 28(b)). With this modification, so long as the clock input is held high, the Q output of the S/R flip-flop will follow the data input. However, once the clock goes low both the inputs to the flip-flop are held at logic '1' so that it will no longer change state and whatever data were present before the clock transition are stored.

The master-slave JK flip-flop is considered as the universal flip-flop. It can be used as an R/S flip-flop by using the preset and clear inputs. It can be converted into a D (data or delay) flip-flop by connecting an inverter between J and K inputs. A toggle action follows if J and K inputs are held high. This versatility is floated on the system by the judicious use of feedback techniques.

If the Q output of the slave is initially low, then the master flip-flop will be set by a high at the clock input. The slave remains reset, however, so there is no danger of the feedback to the master section.

When the clock input goes low, the information is transferred from master to slave because the inverter in the clock route enables the slave section to receive the relevent information from the master counterparts. This is followed by a change in feedback to the master section, thereby resetting it to its initial state. Note that the behaviour of the flip-flop can be predicted by observing the J and K inputs in the previous interval just before the occurrence of the trailing edge of the clock pulse.

Ring counters use an integral multiple of delay with respect to the input signal. Once the desired state is reached, a feedback is applied instantaneously to the inputs. The purpose of the feedback is to preserve the information content and shift it in the specified direction at the speed of the clock pulses. All the flip-flops in a given chain of the ring counter will change their status simultaneously, hence the name synchronous counter (Fig. 29). If all Q outputs are

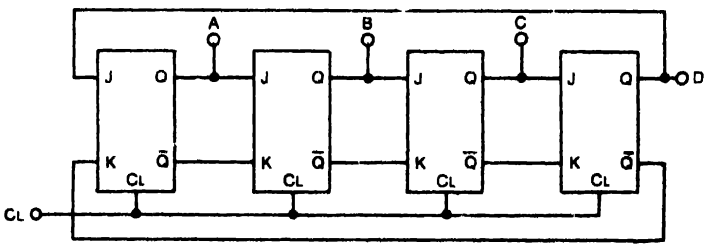

Fig. 29: Flip-flops in a chain formation.

initially held at zero, the system is bound to reject its input commands. A start signal is therefore necessary to load the counter with specific information.

Johnson counter, or twisted-ring counter, eliminates the problem of starting the signal by cross coupling the feedback lines. Information storage or counting is synchronous and the system is self-starting. Such a counter has '2n' unique states, where n is the number of flip-flops in the counter (Fig. 30).

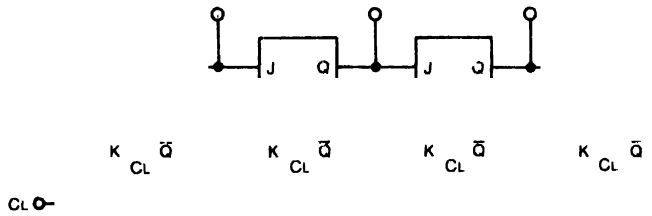

Fig. 30: Johnson counter using number of flip-flops.

Asynchronous or ripple counter also makes use of feedback technique, mainly to bring back the system into the initial status. Here the changes in the blocks are not simultaneous and the feedback may not necessarily be from the final output (Fig. 31).

The ripple counters are less complex and less expensive but provide a lot of unwanted spikes during state transitions. With the help of proper feedback sections and gates, they can be converted into both up counter and down counter. Several different types of counters are available to the designer, varying mainly in the feedback pattern rather than the basic configuration. Note that in a shift register the cornerstone of the counter family is quite restrictive such that it cannot go from just any state to another.

The innocuous switches at the gates may burst with incisive glitches and sproggies when they are operated, which can upset the digital applecart. Minute changes in applied voltage between the upper and lower threshold at the input generate invalid changes at the output of the logic gate.

Contact debouncer, the checkmate for the display of anger of the gate at its switching, is a simple case with no delay of feedback into the same system to store the information for a period decided by the external source (Fig. 32). The very first crossing of the input voltage over the upper threshold takes the output to high state and it is fed back instantly to the input to maintain its newly acquired state. However, a residual error may be expected at the equilibrium state.

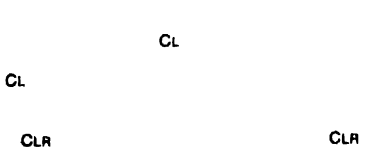

Fig. 31: Schematic showing changes in flip-flop chain.

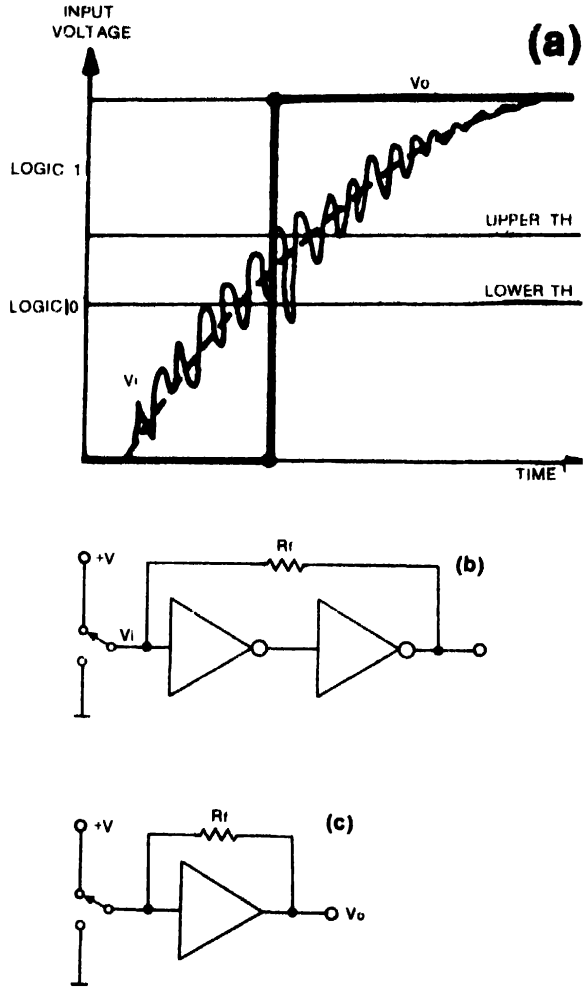

Fig. 32(a): Debouncing circuit using inverter gates. (b) Debouncing circuit using buffer gates. (c) Graph showing first crossing of the input voltage over the upper threshold level.

The principle of the phase locked loop (PLL) is not new. It was used in some deluxe communication receivers in the mid-1930s. Later, it was found to be highly effective in TV receivers for the synchronisation of the vertical and horizontal deflection units. PLL circuits are extensively used in CB transceivers, frequency synthesisers, function generators etc.

Phase locked oscillators exhibit comparatively high stability and low phase noise which are the desired features of the local oscillator in UHF digital radios. The phase locked sources in communication systems are accepted for their spectral purity. The efficiency of pulse-width modulated bridge rectifier using a PLL system along with thyristors is considered to be 'the ultimate' in the power supplies.

In principle, a PLL circuit can be likened to an op-amp connected with feedback, such that the output voltage of the op-amp varies to keep a similar voltage at both inputs. The PLL circuit varies the frequency of its output, so that the frequency of both its input signals remains the same. Seemingly, there isn't anything remarkable about its operation. It is a type of servo system whose output frequency locks on to, and follows, an input reference signal. Furthermore, its output frequency can be an integral multiple of, and in phase with, the input frequency. Hence, it is logical to begin with a description of the entire PLL circuit and its operation in general.

The PLL system consists of a phase detector, a low pass loop filter and a voltage controlled oscillator or VCO. Essentially, it is a control system in which the control is based on the phase difference between the input signal and the signal from the VCO. In a conventional automatic frequency control system, some difference of frequency is required to produce an error signal. In the PLL, only a difference of phase within each cycle results in a precise correspondence between the input signal and the VCO output.

The input reference signal and the output of the VCO are locked in phase by comparing the phase of the two signals in a detector that converts any phase difference into an error voltage or current. The magnitude and polarity of error voltage proportionally shifts the phase and frequency of the VCO in the direction that causes it to track the input frequency and phase. The speed with which the PLL adjusts the VCO to follow up any change in the input frequency depends on the low pass filter, which in turn determines the bandwidth of PLL.

If the frequency of the VCO is exactly equal to the input, the error signal can be evolved only in the phase difference between these signals. The phase difference (ϕi - ϕv) is detected and a corresponding voltage is produced as Vd (Fig. 33). Since the expected variations are small compared to the frequencies fi and fv, the error voltage Vd is subjected to a low pass filter and if necessary the filtered voltage is then amplified to a satisfactory level so as to control the VCO operation.

Any tendency of either fi or fv to change will result in a increase or decrease of (ϕi- ϕv) and the filtered voltage Vd. This process ultimately leads to a state where (ϕi- ϕv) is equal to zero or fi is exactly equal to fv. Now the system is said to be in lock.

In the correct sense, the system is a proportional controller with a phase error inversely proportional to the loop gain. Since the phase of a signal is the time integral of its frequency (frequency is the time derivative of phase), the whole system operates as an integral controller with respect to the frequency.

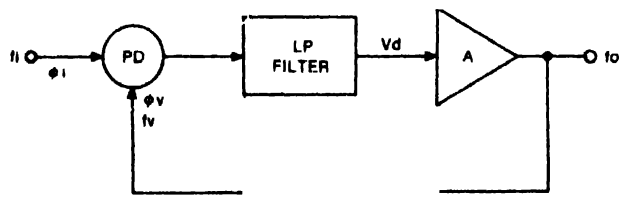

Fig. 33: Block diagram of a phase lock loop (PLL).

When the system is not in lock, there are two distinct possible outcomes. If fi differs from of fv up to a certain value determined by the components of the system, the feedback voltage will differ proportionately, eventually driving the system into the lock. For this (fi-fv) must lie within the passband of the low pass filter. Once it is in lock, the VCO frequency is identical to that of the input signal.

The action of the loop causes the phase to take on just that value which is required to generate the DC control voltage necessary to change the frequency of the VCO from its free running value to the frequency of the input signal. This action allows the PLL to track frequency changes of the input signal once the lock has been acquired. The range of frequency over which the PLL can acquire lock is known as the capture range. However, beyond a specific range, (fi-fv) will not create any impression on Vd mainly by the low pass filter, due to which the PLL behaves like a helpless onlooker.

The loop transfer function H(s) is the ratio of the phase angles ϕv(s) to ϕi(s). The performance of the loop is dependent on the form of filter which may be a simple lag or lead network. Active equivalents may also be used for better tracking ability of the system. However, the constraints in the selection of filters are the conflicting requirements of bandwidth. The bandwidth should be as narrow as possible to avoid phase jitter due to noise. On the other hand, for best tracking and acquisition or for minimum transient error due to signal modulation, the bandwidth should be as large as possible.

It is difficult at this point to suggest what the state of electronics without feedback would be like. Opinions concerning the role of feedback have changed radically in the past few years. The present single and dual loop feedback are not suitable for a number of reasons, including the loss of amplitude and the inhibition and modulation of the actual signal. Observations indicate that there is a best frequency for a given set of operating conditions and away from that, the system evokes subtle variations. In the recent past, considerable interest has developed in the possibility of multiple feedback for the optimisation of man-machine systems.

A great deal of theoretical as well as experimental research will be needed before further significant progress can be made. However, the general approach of the feedback model still stands as the best means to probe into some well defined situations. Here, no attempt has been made to be all-inclusive. The simple systems reviewed here are meant only as a starting point for limitless refinement of our knowledge which instils in the brain that function called mind

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