Digi-Course II

Chapter 6

We have seen so far how divider and counter circuit can be constructed using cascaded Flipflops.

In this chapter, we shall see another practical application of the cascaded Flipflops; the 'Shift Register'

1

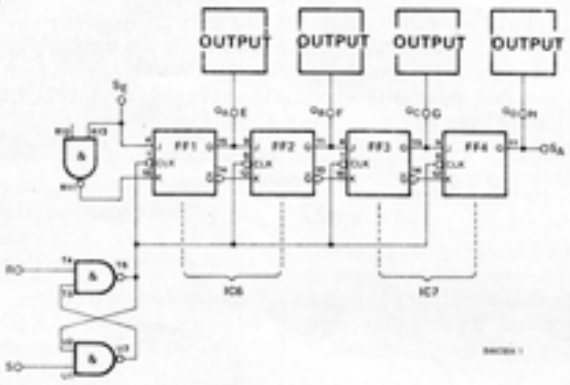


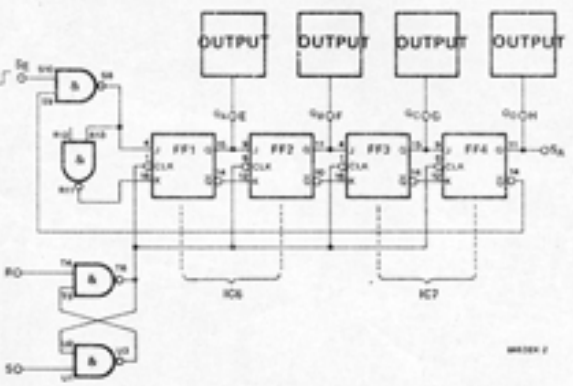
Figure 1 shows a cascade of four Flipflops connected in such a way that the outputs Q and $\overline{Q}$ of each Flipflop are connected to the inputs J and K of the next Flipflop. The clock inputs of all four Flipflops are connected together. A 'NAND' gate inverter is inserted at the input of the first Flipflop so that the possibility of having J/K = 1/1 or 0/0 is eliminated. The state of input SE is thus taken as a single input to the cascade and travels to the next Flipflop on occurance of a clock pulse at the clock input. If we sent the in put SE = "1" at the first clock pulse and then reset it to "0" before the second clock pulse, we can observe that this "1" will travel to the next Flipflop on every subsequent clock pulse. On the fifth clock pulse the "1" gets out of the last Flipflop and as the output of the last Flipflop is floating, it is lost from the cascade.

The clock pulses are generated by alternately connecting the R and S inputs to the ground line. The NAND gate Flipflop consisting of gates T and U switches states on each transition and the clock is "debounced"

As the circuit described in Figure 1 is used to shift the data at the input forward to the next Flipflop on every clock pulse, it is called a 'Shift Register'. For proper functioning of the circuit, all unused inputs of IC 6 and IC 7 must be connected to "1"

Figure 2 shows how we can prevent the "1" from getting lost on the fifth pulse.

2



Here the $\overline{Q}$ output of the last Flipflop is connected back to the input of the first Flipflop, through the OR gate obtained by using a NAND gate. A NAND gate functions as an OR gate with inverted inputs. In the circuit of figure 2, SE must always be held at "1" and taken to "0" only at the first clock pulse, so that a "1" is entered into the Shift Register. At the fifth pulse when QD switches from "1" to "0", QD switches from "0" to "1" and this "0" being shifted out of the FF 4 appears at the input Sg of the NAND gate S. This in turn appears as a "1" at the output pin S8 and enters Flipflop FF 1 on the fifth clock pulse. This "1" again travels through the cascade for next four clock pulses, and appears at the QA output of FF 1 on the 9th clock pulse. This operation continues as long as we provide the clock pulses. This modified circuit is called the Ring Counter.

As the Flipflops can assume any state when power is switched on for the first time, we must initially Reset all the Flipflops to "0" before starting the clock pulses, otherwise the initial condition of the Flipflops will keep on rotating through the Ring-Counter.

The circuit of figure 2 has only four Flipflops; and can count only four clock pulses. If we want to construct a Decimal Ring Counter we need 10 Flipflops. This will have its feedback line which activates after every 10 pulses. Another Decimal Ring Counter can be operated from this feedback pulse used as a clock pulse. Practically, such circuit are not constructed using individual Flipflop ICs. Fully integrated Shift Register or Ring Counter ICs are available for these applications.

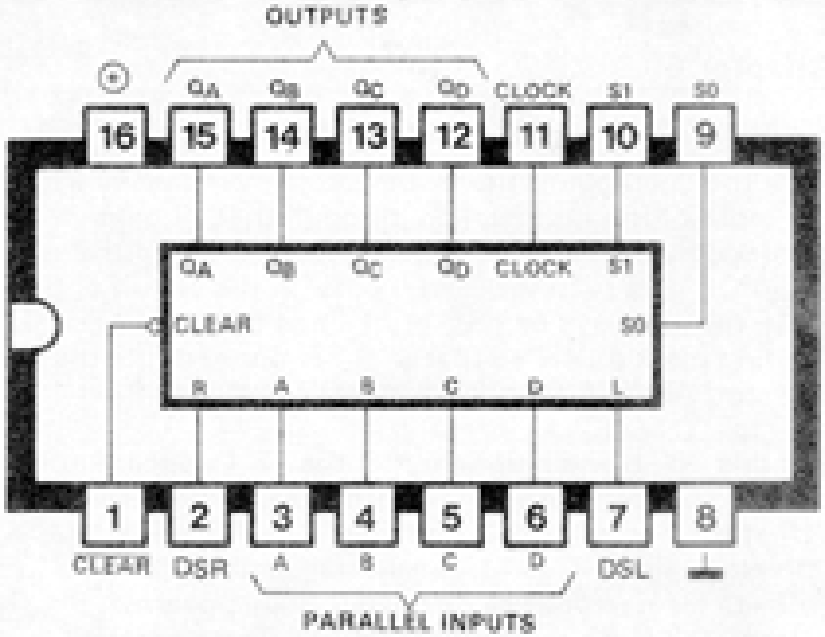
Shift registers are often used in Computer Technology, and rather than entering 1 bit, a series of bits is entered. For example, a bit sequence of 1001 can be entered into a Shift Register using clear and preset inputs and shifted out bit by bit. This will represent a serial transmission of the binary number 1001 (Decimal 9)

If the sequence 1001 is entered bit by bit into a shift register on 4 clock pulses, we have the combination 1001 at the outputs Q_A, Q_B,Q_C and Q_D at the end of the fourth clock pulse, thus representing a serial input of the binary number 1001 into the 4 bit Shift Register, which gives a parallel output 1001 at the end of the 4th Clock pulse.

In the first case when we set the 4 Flipflop outputs to 1001 before giving the clock pulses, it can be described as parallel input/serial output operation. In the second case, where we had all Flipflops set to zero, and entered the sequence 1001 bit by bit at every clock pulse, it can be described as serial input/parallel output operation.

Data transmission between two devices can either be serial or parallel. Serial transmission requires only two lines, one data line and one ground line. Parallel transmission requires one line for each bit and an additional ground line. For 8 bit data transmission in parallel mode, we would thus require a 9 core cable. However, as the parallel transmission can take place in one shot, it takes much less time than in case of serial transmission. An 8 bit data to be transmitted serially will require minimum 8 clock pulses, whereas if it is transmitted parallely it will take only one clock pulse. (almost 8 times faster!)

3 **74LS194**



You can try the serial and parallel data transmission using two Digilex Boards. The internal block diagram of a 4 bit Shift Register IC 74 LS194 is shown in Figure 3.

This particular IC can operate as Shift Left or Shift Right Register. The direction of Shift is decided by the combination at the inputs S0 and S1 a 01 combination gives Shift Left and a 10 combination gives a Shift Right operation. A 11 combination allows parallel entry of data The Clock input is blocked by the 00 combination. CLEAR input is used to reset all the outputs to "0"

Pins DSR and DSL are used as the data input pins during Shift Right and Shift Left operations.