CMOS LOGIC ICs

Part III-CIRCUIT IDEAS

In the preceding articles of this series, we have studied in detail the characteristics, behaviour and methods of use of CMOS logic devices. The knowledge we have gained would be useless if it is not put to use. At this stage, one point must be made clear. Although it was stressed in the previous article that CMOS devices should be handled with care, this does not mean that they are so delicate that the hobbyists and other users are scared off from using them!

People who may feel afraid to use them, have just not understood what was said – all devices have a built-in protection against a wide range of handling conditions, but still they must be used carefully so as to avoid unexpected failure and corresponding disappointments. So if one just avoids touching the IC pins, uses a well-insulated soldering iron and follows some of the general operating procedures, it is usually sufficient to work with these ICs, in the average case under normal environments of a laboratory (though not for industrial production which demands high reliability). So, a fresh look at CMOS for all your requirements will show the benefits they give you.

Coming to the actual application, it is not necessary to describe the applications of each gate and IC, since they are functionally identical with similar TTL devices, which users are assumed to be familiar with. Further, individual ICs are described better in the manufacturers' data sheets. The same logic system design procedures usually adopted for TTL ICs stand for the CMOS devices, except for specific differences like voltage levels, current, speed, pin connections etc. Thus, here we will discuss more about circuit designs which utilise the specific characteristics of CMOS devices.

Pulse circuits

CMOS digital gates find a wide application in pulse generation and shaping circuits. The circuits described here, can generate fixed width pulses corresponding to a given pulse train input. The output pulse width, in some cases, depends entirely on the characteristic of the CMOS gate used while in other cases, it depends on external RC connections.

Pulse stretcher. The circuit in Fig. 1 can be used to obtain pulses of specified width from narrow input pulses. A positive pulse at the input causes the inverter output to be low, discharging the capacitor through the diode D1. The capacitor is rapidly discharged so that the Schmitt trigger inverter input is brought too low and the output goes high. Check that the size of capacitor is small enough so that it can be rapidly discharged within the period of a narrow input pulse. This implies that,

$$\text{Inverter current sink} > \frac{V_{CC}}{t} + \frac{V_{CC}}{R}$$

where t is the input pulse width. When the inverter input returns to zero, after time 't' seconds, the diode blocks the inverter from charging the capacitor, which is charged from the supply through the resistor. When the Schmitt input

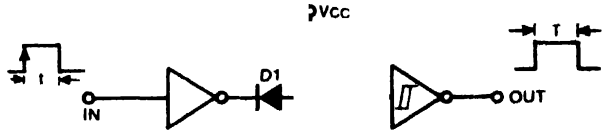

Fig. 1: Pulse strecher.

reaches its upper threshold level V_{T+}, the output goes low and remains in this state until another pulse comes to the input. Thus the output pulse period is given by

$$T = RC \log_e \left(\frac{V_{CC} - V_D}{V_{CC} - V_{T+}}\right)$$

where V_D is the diode drop (0.6 V for silicon diodes).

Monoshot. The circuit of Fig. 2 is a monostable multivibrator. Normally, the input is zero and the first NOR gate output is high, keeping the capacitor discharged. Since the second NOR gate input is also high, its output will be low,

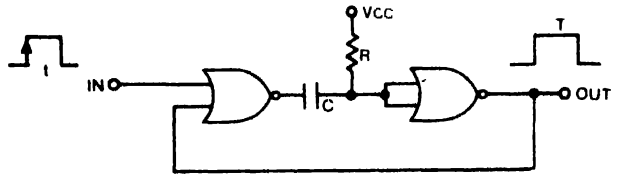

Fig. 2: Monoshot.

which confirms again that the first NOR output will be high.

When a high pulse appears at the input, the first NOR output immediately becomes low, bringing the second NOR input also to low state. This gives a high output, which is fed back to the input NOR. Now the capacitor starts charging from Vcc through the resistor and the first NOR output, slowly raising the input voltage to the second NOR.

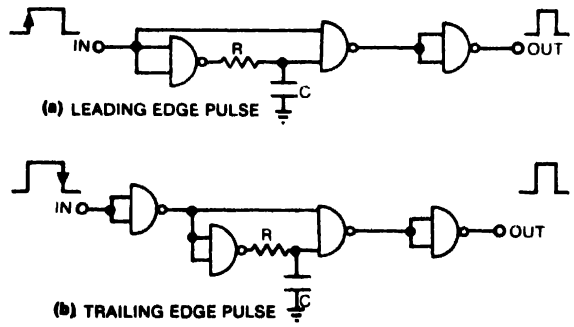

Fig. 3: Digital differentiator.

In the meanwhile, even if the input pulse has disappeared, the input NOR output remains at low, due to the high state output feedback. After a period T, the second NOR input rises above the logic high level and the second NOR output swings to low state. This brings the first NOR output back to the high state, and the circuit comes back to the original condition. The output pulse duration is given by

$$T = 1.4\ RC$$

Digital differentiator. Differentiators are used to produce a narrow pulse at the edge of a wider pulse. The circuit of Fig. 3 can produce such pulses either at the rising edge or falling edge of the input. In Fig. 3(a), when the input goes high, the first inverter output goes low. This is delayed by the RC filter and the delayed low-going pulse is fed to the output AND logic. Thus, the output will be high only for the duration of overlap between the two inputs, which corresponds to the delay produced. Thus a small pulse appears corresponding to the rising edge of the input.

In Fig. 3(b), the input signal is inverted, thus the output pulse corresponds at the falling edge of the input signal. For producing the delay, the RC elements can be replaced by a chain of CMOS gates, whose total combination does not invert the signal flowing through, but produces sufficient delay at the output due to the propagation delay of each gate.

Frequency doubler. The principle of delay can be used to double the frequency of any square waveform, as shown in Fig. 4. The input square wave signal is buffered by the first EXOR gate before being fed to the delay RC network. The delayed waveform is now EXORed with the input waveform to produce the output. This will be high only when one of the two input signals is high. Hence, a pulse will be produced at each edge, whose width corresponds to the delay produced.

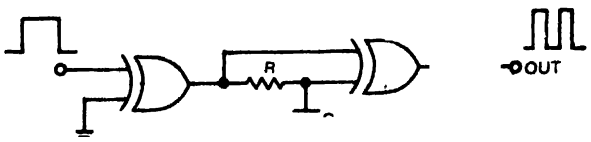

Fig. 4: Frequency doubler.

Thus, if the input is a square wave, the output will be a train of equally spaced pulses, with frequency double that of the input. As in the previous case, the delay element may be replaced by a chain of gates.

Linear application

As we have seen earlier, the CMOS inverter can be biased for operating in the linear mode. Thus, any CMOS inverting gate can be used in many of the common amplifier applications. Even without biasing the inverter, it can be used as a voltage comparator for numerous linear applications. A few such circuits are described here.

AC amplifier. Three CMOS inverters can be suitably biased for use as an AC amplifier with a gain of ten as shown in Fig. 5. Actually, the higher the open loop gain is achieved, the more accurate will be the closed loop gain. The open loop gain is multiplied by the number of stages (which must be an odd number) used inside the feedback loop.

Integrator. A shown in Fig. 6, CMOS inverter can be biased to operate as an integrator for AC signals, with an integrating time constant of RC.

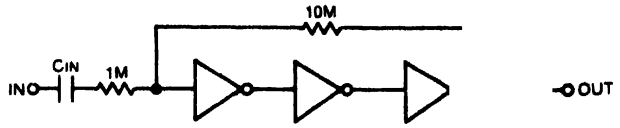

Fig. 5: AC amplifier.

Fig. 6: Integrator.

Post amplifier. Low power op-amps can be buffered with an CMOS inverter. This gives the advantage of operating the op-amp under no load condition with full voltage swing frequency capability and low power loss. Such a circuit is shown in Fig. 7. This circuit uses the low power advantage of both devices. At the output, more inverters may be paralleled (six inverters come in a single package) to obtain

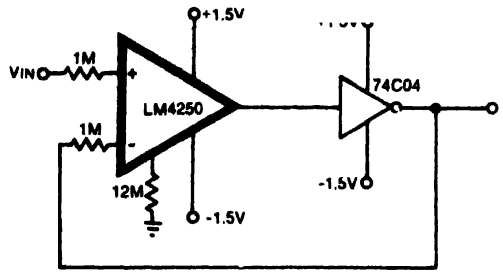

Fig. 7: Post amplifier.

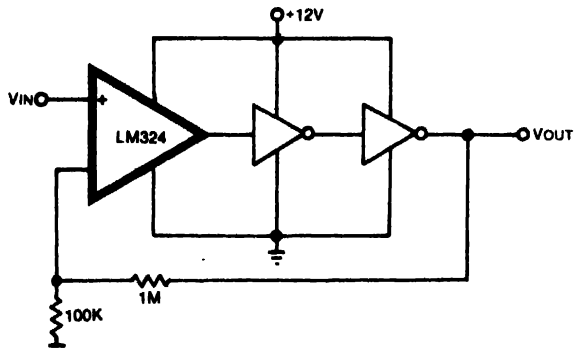

Fig. 8: Single supply amplifier.

increased current drive, even for ordinary op-amps, operating within the supply limits of ±7.5 V.

Single supply amplifier. The CMOS inverter can also be used with single supply op-amps such as the LM324 as shown in Fig. 8. The CMOS inverters can be paralleled for

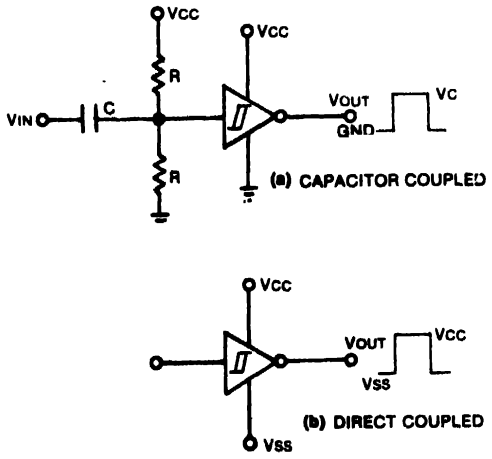

Fig. 9: Voltage comparator.

increased power to drive higher current loads. Loads of 5 mA per inverter can be expected under AC operating conditions.

Voltage comparator. A CMOS inverter with Schmitt trigger input can be biased to operate as a voltage comparator, within the range of its threshold voltages. Typical circuits are given in Fig. 9. The circuit of Fig. 9(a) biases the input to half the supply voltage and the input AC signal to be compared is coupled through the capacitor. The output is a rectangular wave, swinging in accordance with the voltage comparisons. The capacitor impedance at the lowest operating frequency should be much less than R/2. The circuit of Fig. 9(b) uses a split supply voltage between ±1.5 to ±7.5V, so that the input AC waveform can be directly coupled.

Light activated switch. A simple light activated switch can be made as per the circuit of Fig. 10. Since the input impedance of the CMOS is very high, input biasing is very easy. Only one LDR and a preset potentiometer is needed for sensing. The LDR and potentiometer forms a potential divider whose mid-point is biased suitably by adjusting the potentiometer, so that the inverter switches for the desired illumination. After that, whenever light falls on the LDR,

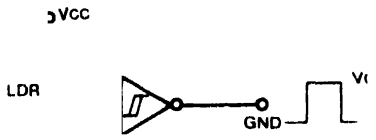

Fig. 10: Light activated switch.

the mid-point voltage rises as light intensity increases. When the upper threshold voltage is reached the inverter output will become low and remain low until the light intensity is reduced significantly.

Oscillators

At last we come up with a wide variety of CMOS oscillators to suit your various applications. These circuits offer the following advantages:

i) Guaranteed self-start
ii) Good stability with respect to power supply variations
iii) Wide operating supply voltage range (3V to 15V)
iv) Wide operating frequency range (less than 1 Hz to about 15 MHz)
v) Low power consumption
vi) Easy interface to other logic families
vii) Symmetrical output waveform (due to symmetry of output transistors)

Both RC and crystal oscillators are described here. The stability of the RC oscillator is sufficient for most applications. Certain applications, like time-keeping over long intervals, require crystal oscillators.

Single gate oscillator. The circuit of Fig. 11 is the simplest possible oscillator, using one Schmitt trigger input CMOS

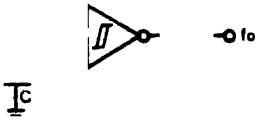

Fig. 11: Single gate oscillator.

inverter. The capacitor is charged and discharged through the inverter output in accordance with the gate input swings between the two threshold voltages, V_{T+} and V_{T-}. The output frequency is given by

$$fo = \frac{1}{RC \log_e \left[\frac{(V_{CC} - V_{T-})}{(V_{CC} - V_{T+})} \frac{(V_{T+})}{(V_{T-})} \right]}$$

Two gate oscillator. The circuit of Fig. 12 uses two ordinary CMOS inverters to form a square wave oscillator. The

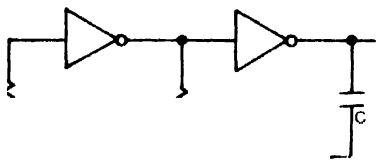

Fig. 12: Two gate oscillator.

only disadvantage of this circuit is that for low values of the capacitor, the circuit may not oscillate at all. The output frequency is given by:

$$fo = \frac{1}{1.4\ RC}$$

Three gate oscillator. To overcome the problem of the earlier circuit, another inverter is added to the circuit so that it will always oscillate. The circuit is shown in Fig. 13, using

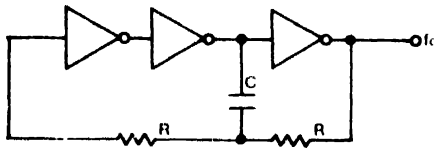

Fig. 13: Three gate oscillator.

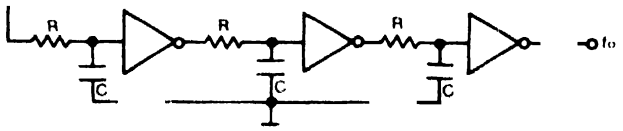

Fig. 14: Phase shift oscillator.

three inverters. Actually any inverting CMOS gate or combination of gates can be used. The output frequency is given by:

$$fo = \frac{0.56}{RC}$$

Phase shift oscillator. A phase shift oscillator using three CMOS inverters is shown in Fig. 14. The output frequency is given by:

$$fo = \frac{1}{3.3\ RC}$$

Crystal oscillator. Fig. 15 illustrates a crystal oscillator using only one CMOS inverter. Any odd number of inverters can be used, but due to propagation delays, fewer inverters give maximum possible frequency. At the crystal

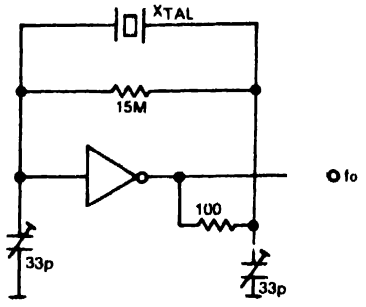

Fig. 15: Crystal oscillator.

frequency the feedback resistor biases the inverter for linear operation while the output frequency can be trimmed to a small extent by either of the two capacitors.

Voltage controlled oscillator. A simple VCO is shown in Fig. 16, using a CMOS inverter as an integrator, a CMOS Schmitt input inverter as a comparator with hysteresis and a transistor as a discharge switch. The inverter integrates the positive difference between its threshold V_{TH} and the input voltage V_{IN}. The output is a ramp till the positive threshold V_{T+} of the Schmitt trigger is reached. Now the Schmitt output goes low, giving a low going pulse output and turning

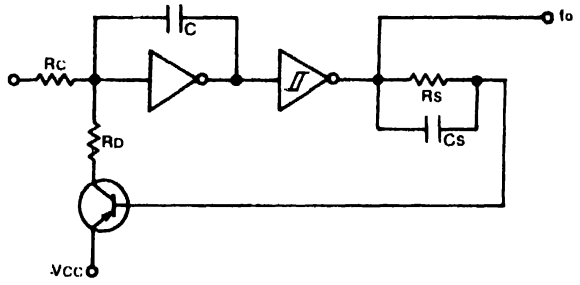

Fig. 16: Voltage controlled oscillator.

on the transistor switch. This discharges the capacitor through R_D while hysteresis keeps the switch on. Resistor R_D must be kept much smaller than RC to keep reset time negligible. With the capacitor discharge, the inverter output voltage falls, and when this becomes equal to the negative threshold V_T of the Schmitt input, the output becomes high and the transistor turns off. The cycle is repeated with a frequency given by

$$fo = \left(\frac{V_{TH} - V_{IN}}{V_{T+} - V_{T-}} \right)$$

where $0 \leq V_{IN} \leq V_{CC}$

The frequency dependence with voltage is given by

$$\Delta \frac{fo}{\Delta V_{IN}} = \frac{-1}{(V_{T+} - V_{T-}) RC}$$

where the negative sign indicates that maximum frequency will be obtained for V_{IN} equal to zero and frequency will decrease with increase of V_{IN}. At V_{IN} equal to V_{TH}, approximately 0.55 V_{CC}, the circuit will finally stop oscillating.

(To be continued)