DIGITAL ELECTRONICS BY EXPERIMENT pt4

IN THIS PART of the course we shall look into sequential logic using the 7400 IC as a building block.

Set the IC up on the board to make a circuit using two of the logic gates as shown in Fig. 1. The gate with its output taken to the LED should have its spare input marked R, while the spare input to the other gate should be marked S.

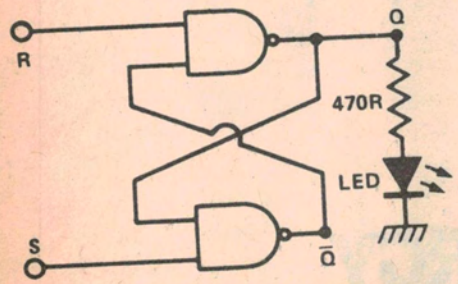


Fig. 1 Cross-coupled NAND gates forming an R-S flip-flop.

This circuit is a flip-flop, as you may have guessed from the cross-coupling of inputs and outputs. Complete the table shown in Fig. 2, and note that the output for R = 1, S = 1 is *not* the same in each case.

Sequential Logic

The R-S flip-flop, as this is called, is an example of a sequential logic circuit, in which the output depends on the *sequence* of signals at the input – in other words, the state of the output depends on the previous signals as well as the present ones. Strictly speaking this circuit is more of a *latch*, a circuit which temporarily stores an output while both inputs are high. Note that in normal use, we want two outputs Q and $\overline{Q}$ to be complementary ($\overline{Q}$ is always the inverse of Q) so that the input R = 0, S = 0 must not be used, since this gives Q = $\overline{Q}$ = 1.

In logic circuits, clocked flip-flops are much more common. A clocked flip-flop changes state only when a timing, or clock pulse is received. This is done by combining the flip-flop action with gating so that the signal inputs have no effect until the gating (clock) pulse arrives.

One type of clocked flip-flop is the D-type, and a typical truth table is shown in Fig. 3. In this type of circuit the signal (0 or 1) which is present at

R	S	Q
0	1	
1	1	
1	0	
1	1	

Fig. 2. Part truth for R-S flip-flop. When you complete the table, taking readings from your blob-board circuit, be sure to work through each state in sequence.

the D (for Data) terminal is transferred to the output at the clock pulse, and remains unchanged until the data changes *and* the clock pulse arrives.

Clocked Flip-Flop

The type of flip-flop chosen for this board is the J-K flip-flop. This is a more versatile device which combines clocking with gating to achieve a wide range of actions. On the type we have chosen, the SN7476, the action is the type known as "Master-Slave", which means that the input signals are accepted on the leading edge of the clock pluse, but the outputs do not change until the trailing edge comes along. This avoids problems which would occur if outputs were connected back to the inputs, as we shall see later.

The J-K flip-flop has five inputs and two outputs. The inputs are labelled J, K, Clock, Set and Reset (the Reset is sometimes called clear, and the Set terminal is sometimes called preset). The outputs are Q and $\overline{Q}$, with $\overline{Q}$ always the inverse of Q. We shall check the action of the J-K flip-flop using signals generated on the board.

From previous work you should have available one section of the 7414 connected as a low speed oscillator. This provides an ideal slow clock pulse, and you should already have an LED connected to the output of the 7414 to monitor this pulse.

Double Flip-Flops

The connection diagram of the 7476 is shown in Fig. 5. From this you will see that the 7476 contains two J-K flip-flops which are completely independent. For the first series of practical exercises we shall use only one half.

Solder connections from pin 13 of the 7476 to earth, and from pin 5 to the +5 V line. Now solder an insulated wire connection from the clock oscillator output to pin 1 of the 7476, so that flip-flop number 1 is activated.

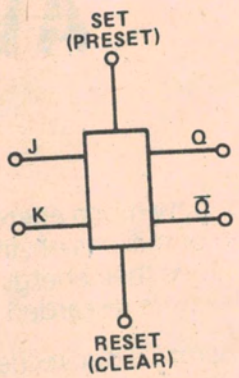


Fig. 4. J-K flip-flop symbol.

Connect pins 4 and 16 to earth so that J = 0 and K = 0, and connect switches so that the reset pin (pin 3) and the set pin (pin 2) can be connected momentarily to earth as needed. The circuit is now as Fig. 6, and the board appears as shown in Fig. 7.

Now connect a resistor from pin 15 (Q) to a spare pad, and an LED from the spare pad to earth. This LED will

D SIGNAL	Q BEFORE CLOCK	Q AFTER CLOCK
0	0	0
0	1	0
1	0	1
1	1	1

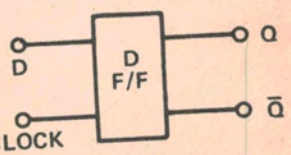


Fig. 3. D-type flip-flop and truth table. Note that, unlike the R-S flip-flop, changes take place only when the clock pulse arrives.

indicate the state of the Q output from the flip-flop.

Switch on, and look at the LED. Using the SET switch, set the output to give logic 1. (This happens when the SET switch is returned to 0, whatever the clock pulse is doing at the time.) When the switch is changed back again, does the output change at once? Or when a clock pulse arrives?

These changes and others which follow may be easier to observe if the clock pulse is very slow, and a 1 000 μF, or greater, capacitor may be used in the oscillator circuit. Later, a "debounced" switch will be used.

Complete this sequential truth table, in which Q_{n-1} is the value of Q just before the clock pulse arrives, and Q_n is the value of Q just after the end of the clock pulse (the 1 to 0 change). Can you decide when the change, if any, occurs? Is it on the leading or the trailing edge of the clock pulse?

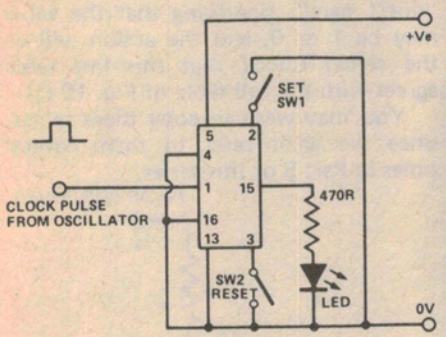


Fig. 6. Circuit for checking J-K action, see text for details.

Now switch off, and disconnect one end of the link between K pin (pin 16) and earth, so allowing K to float to 1. Now we have J = 0 and K = 1. Switch on and observe the output. Change the output by using a switch (which one will you use, SET or RESET?). Does the clock pulse affect the output after the switch has been returned to normal?

Switch off again and reverse the connections so that J = 1 and K = 0, and repeat your readings. Enter all the readings on the sequential truth table of Fig. 8.

From these exercises you will have found that the action of the J-K flip-flop can be controlled by the J and K inputs, which act to force the output to either 1 or 0 when the clock pulse arrives. The SET and RESET pins act independently of the clock, making the output go to 0 or 1, and holding it there until the reset or set voltage rises to 1 again, when the next clock pulse will cause whatever output is forced by the J and K voltages.

Toggling

With the power off, disconnect the wires from both J (pin 4) and K (pin 16). Switch on again, and observe both the output and the clock LEDs. Now complete the truth table of Fig. 8 (c). In this arrangement the J-K flip-flop is acting as a divide-by-two stage, for there is one complete output pulse for each two complete input pulses – we say that the flip-flop is *toggling*. At any time during this action, the output may be forced to 1 or 0 by the action of the SET or RESET pins, but it will revert to the toggling action when the SET or RESET is released.

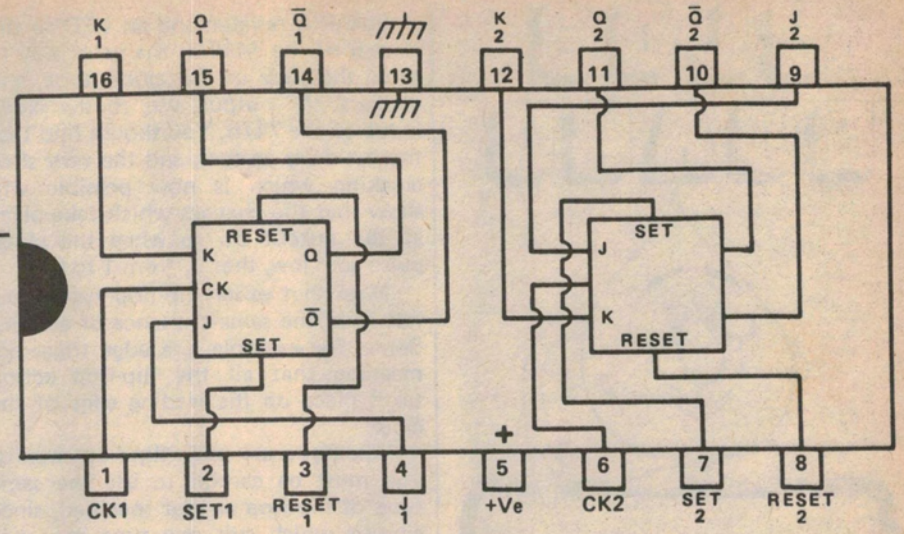


Fig. 5. Pinout of the SN7476 dual master-slave J-K flip-flop.

J=0
K=1

Q_{n-1}	Qn
0	
1	

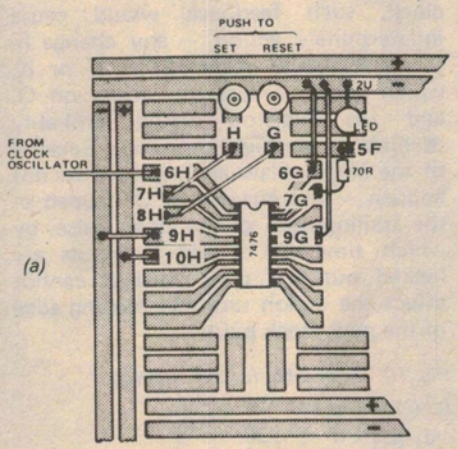
J=1
K=0

Q_{n-1}	Qn
0	
1	

J=1
K=1

Q_{n-1}	Qn
0	
1	

Fig. 8. Remaining truth tables for J-K action.



(b)

J=0
K=0

Q_{n-1}	Qn
0	
1	

Q_{n-1} – STATE OF Q (0 OR 1) BEFORE CLOCK PULSE

Qn – STATE OF Q (0 OR 1) AFTER CLOCK PULSE

Fig. 7. (a) The layout on the board, with the LED in position.
(b) Form of part truth table.

Try applying a clock pulse obtained from a switch, as in Fig. 9 (a). Wire the switch to the board and replace the connection between the 7414 clock generator and the flip-flop with a connection from the switch output on the flip-flop clock input. Turn on the 5 V supply, and use the switch as a slow clock generator. You will probably find that the output is erratic, sometimes seeming not to change the output when the switch is operated.

This is caused by switch contact bounce.

Switch Debouncing

With power off, rewire the switch with a resistor and a capacitor to one of the spare sections of the 7414, as shown in Fig. 9 (b). This is a simple de-bouncing circuit.

Solder a resistor and an LED to the output of the 7414 in the usual way to show the state of the clock pulse, and connect the output also to the clock input of the 7476. You should find that the action is perfect, and the very slow clocking which is now possible will show that the changes which take place at the output do so when the clock pulse goes low, that is, from 1 to 0.

Note that other flip-flop types may not have the same sequence of actions. Some, for example, are edge triggered, meaning that all the flip-flop action takes place on the leading edge of the clock.

When you are using flip-flop circuits, you must be careful to use the same type of flip-flop as that specified, since circuits which suit one type may not suit another. In particular, the 7476 "Master-Slave" type of flip-flop has a particularly complex action.

In essence, the action is that on the leading edge of the clock, the information which is present (1 or 0) at the J and K inputs is stored and once the clock pulse has reached its 1 value, these inputs are locked out, meaning that changes in J and K will now have no effect. At the trailing edge of the clock pulse, the flip-flop action takes place to change the output. The reason for this construction is that several types of circuits, some of which we shall build in this series, use feedback connections between the output of the flip-flop and its J or K inputs.

If all the action of the flip-flop happened at the leading edge of the clock, such feedback would cause indeterminate action – any change in Q would cause a change in J or K, which might cancel the effect on Q, and the flip-flop would probably oscillate at the high frequency. Because of the Master-Slave action, this does not happen – the changes in Q happen at the trailing edge of the clock pulse, by which time the J and K inputs are locked out and their voltages cannot affect the action until the leading edge of the next clock pulse.

Fig. 10. Truth table for J-K flip-flop
(a) Complete truth table

J–K FLIP–FLOP

INPUTS		OUTPUT	OUTPUT
J	K	Q BEFORE CLOCK	Q AFTER CLOCK
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Investigation

You should already have one section of the 7414 set up as a high frequency oscillator with earphones, or similar, to detect the output note. What is the effect of leading the output of the 7414 oscillator to the clock terminal of the 7476 with J = 1 and K = 1? Listen to the output wave from Q and compare it with the signal from the oscillator.

Can you now design an "octave" oscillator? This circuit will use a single oscillator, but its output will be alternately at oscillator frequency, then at half oscillator frequency (one musical octave below) according to the input to the gate. The gate input could then be obtained from another slow oscillator.

Finally, Fig. 10 (a) shows the complete truth table for the 7476. Fig. 10 (b) shows a changes truth table, in which the settings of J and K to produce certain changes (or non-changes) are listed. In the last table, X means "don't care", signifying that the value may be 1 or 0, and the action will be the same. Check that this last table agrees with the full table of Fig. 10 (a).

You may want to copy these tables, since we shall refer to them several times in Part 5 of this series.

To be continued.

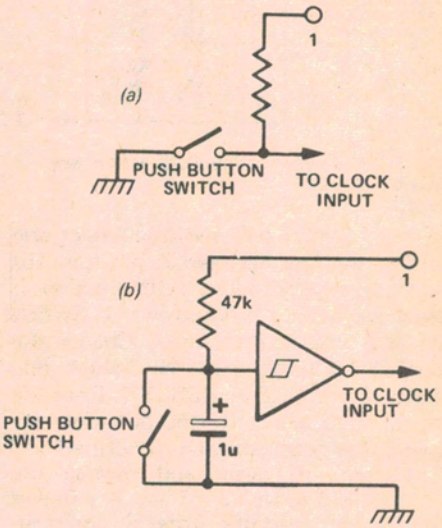


Fig. 9. (a) Using a push-button-switch as a clock pulse supply.
(b) A debounced switch circuit.

(b) Shortened truth table for changes only.

J	K	Q_{n-1}	Qn
0	X	0	0
1	X	0	1
X	1	1	0
X	0	1	1