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When designing a data acquisition system (DAQ) for processing AC signals, your test results may not meet your required specifications, mainly due to poor distortion performance. What should you do under these circumstances? You might check the signal source first, followed by the power supply, the printed circuit board (PCB) layout, and so on, but the issue still exists. Did you consider other reasons, like improper settling of the input signal? That could be a very important consideration.

In this post, I'll talk about how signal settling – and improper settling of the input signal – can affect distortion performance.

Figure 1 shows a simplified model of a successive approximation register [SAR analog-to-digital converter \(ADC\)](#) input circuit and the time-domain charging response of the internal sampling capacitor.

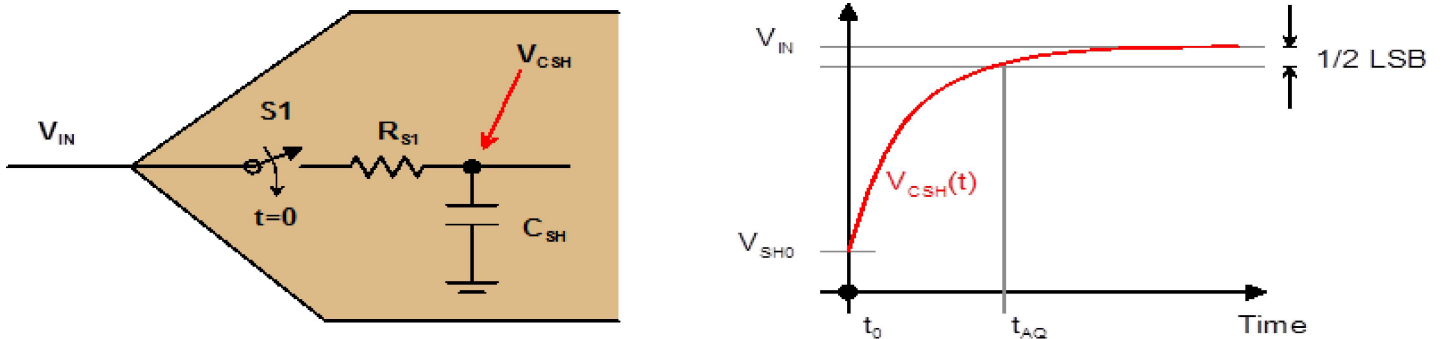


Figure 1: Charge distribution to settle signal

$$V_{CSH}(t) = V_{CSH}(t_0) + [V_{IN} - V_{CSH}(t_0)] \times (1 - e^{-\frac{t-t_0}{\tau}}) \quad \tau = R_{S1} \times C_{SH} \quad (1)$$

During the acquisition phase, there is a charge transfer from the input signal source to the ADC's internal sampling capacitor, C_{SH} . The V_{IN} signal on C_{SH} must settle to at least one-half the least significant bit (LSB) of the final value during the acquisition time, t_{AQ} . Obviously, if the input source requires a longer settling time than t_{AQ} , the residual voltage error across C_{SH} at the end of t_{ACQ} will be greater than one-half the LSB, and the ADC output will be inaccurate.

But distortion is not merely an accuracy issue observed at some value of the input voltage. Distortion signifies a nonlinear relationship between the ADC's input and output. In other words, the ADC transfer curve does not follow the equation of a straight line with constant slope and intercept over the ADC

- input range. So the question is, how can improper signal settling at the ADC input produce distortion or nonlinearity in the ADC response?

Generally, [SAR ADCs](#) have a switch-capacitor input structure with an integrated analog-sampling switch. The on-resistance of the switch, R_{ON} , has a nonlinear resistance with respect to the input signal voltage.

Figure 2a shows a typical R_{ON} vs. the input voltage curve of the complementary metal oxide semiconductor (CMOS) analog switch. The nonlinear on-resistance modulates the settling time constant so that the residual voltage error (V_{ERR}) between the input sinewave and the signal across the sampling capacitor at the end of t_{AQ} is also nonlinear, as shown in Figure 2b. If the on-resistance is ideally constant, the error curve will be a straight line (shown in Figures 3a and 3b), and there will be no distortion in the ADC output.

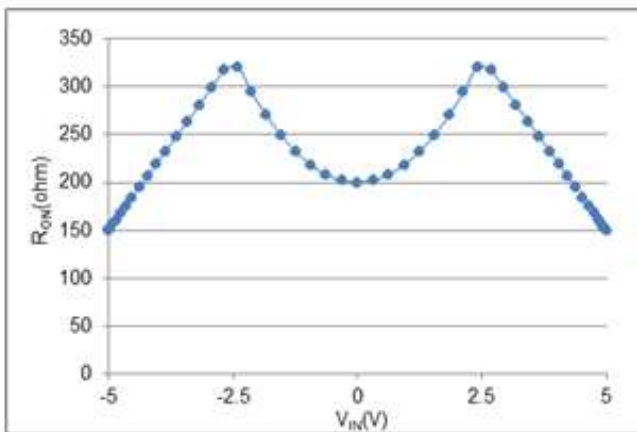


Figure 2a: Typical R_{ON} vs. input voltage

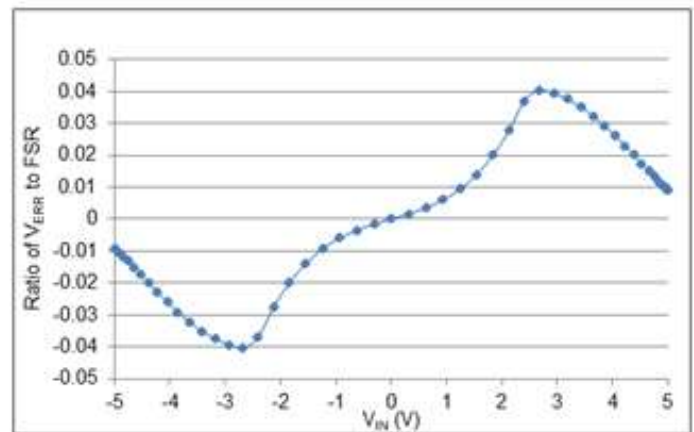


Figure 2b: Ratio of V_{ERR}

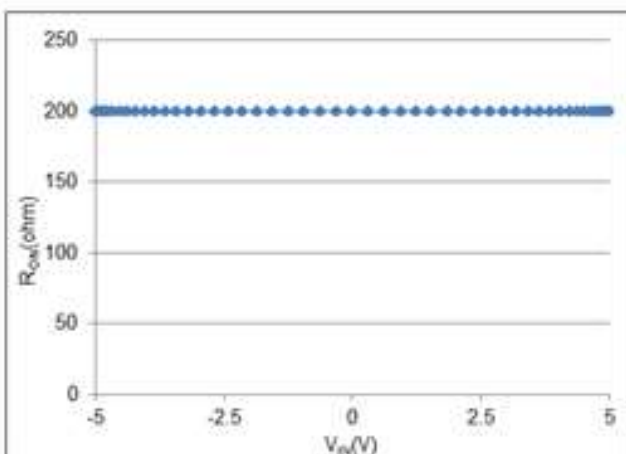


Figure 3a: R_{ON} vs. input voltage for constant on-resistance

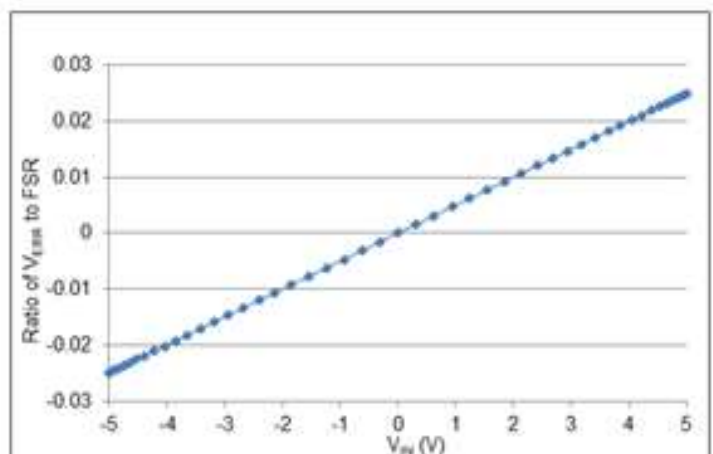


Figure 3b: Ratio of V_{ERR}

Let's take a look at one example with a settling problem. Industrial power-automation applications do not use front-end amplifiers with a SAR ADC due to cost and design-simplification reasons. Figure 4

- shows a typical circuit.

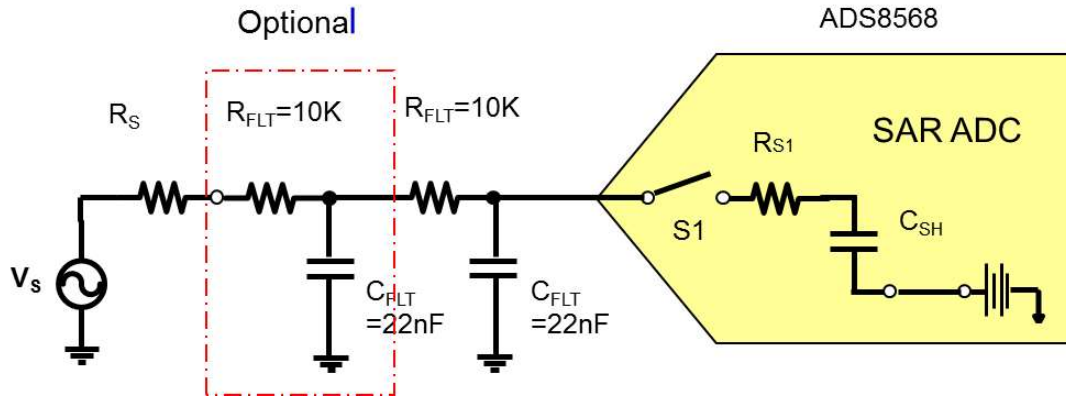
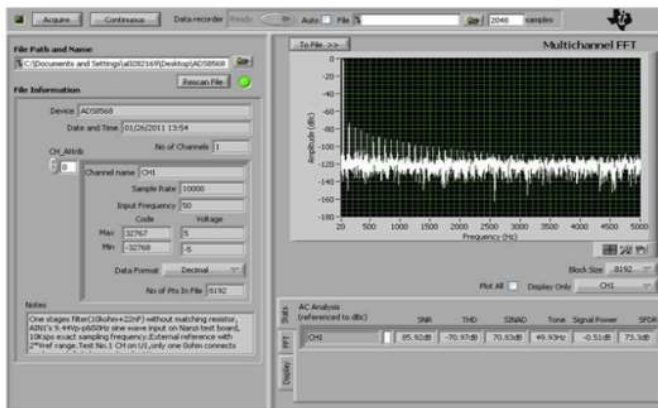


Figure 4: Typical ADC circuit without a front-end amplifier

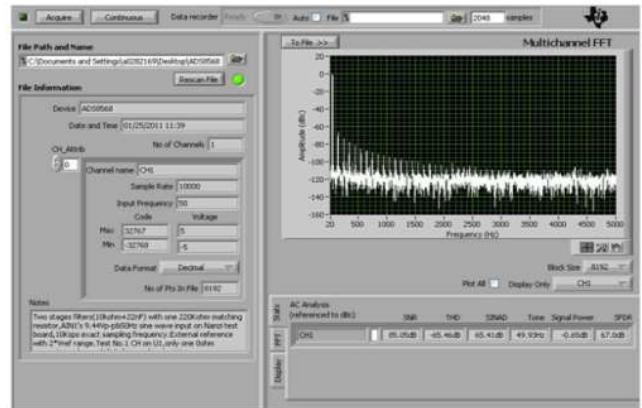
Figure 5 shows the AC performance of the circuit using the 16-bit, 8-channel [ADS8568](#) SAR ADC with a front-end RC filter. A higher value of resistor and capacitor will get a better filter effect without using the active filtering in the circuit shown in Figure 4. However, this results in poor total harmonic distortion (THD), which is much worse than the -90dB spec in the [ADS8568 datasheet](#). A second-order RC filter will make the performance much worse. The root reason is that the input signal, V_s , has not settled properly on the sampling capacitor, C_{SH} , during the ADC's acquisition time.

Sampling Speed	SNR	THD	SINAD	SFDR	Filter
10ksps	85.92	-70.97	70.83	73.3	First order
10ksps	85.05	-65.46	65.41	67.0	Second order

Bad



first order filter: $R_{FLT}=10k\Omega$, $C_{FLT}=22nF$



Second order filter: $R_{FLT}=10k\Omega$, $C_{FLT}=22nF$

Figure 5: Poor AC performance of the [ADS8568](#) with a simplified front end RC filter

You can resolve this settling problem and improve performance by doing two things:

- 1. Increase acquisition time by decreasing the sampling rate directly. You can calculate the real acquisition time with Equation 1, increasing t_{ACQ_Real} time by reducing the sampling rate, because the ADC datasheet specifies a maximum value for (conversion time) (Equation 2):

$$t_{ACQ_Real} = 1 / \text{Sampling rate_Real} - t_{CONV_Data_sheet} \quad (2)$$

Figure 6 shows a refreshed test result with a second-order filter. The AC performance is significantly improved from the previous -65.46dBc to -92dBc THD with a 10Ksps to 1Ksps sampling rate reduction.

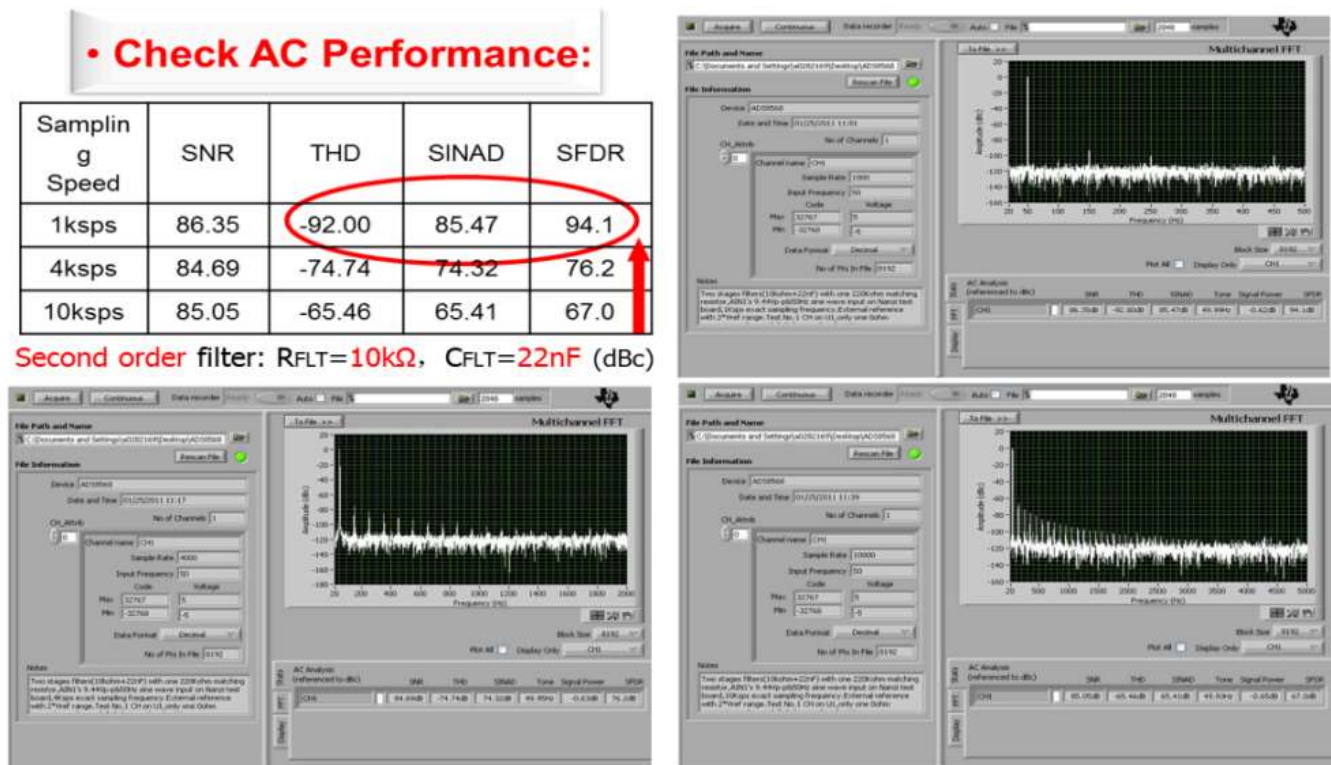


Figure 6: Test result with acquisition time increase

- Speed up settling by reducing the order of the filter's and decreasing X_{FLT}/R_{FLT} value. By reducing the front-end capacitor from 22nF to 820pF with the same 10kΩ resistor for a single-order filter, the THD improves from -70.97dBc to -96.88dBc with the same 10Ksps sampling rate. You can further THD performance to -103.61dBc for a slow 1Ksps sampling rate.

Figure 7 shows the measured results. Please note that there is a trade-off between settling-time improvement and the effect of RC filtering.

• Check AC performance:

Sampling Speed	SNR	THD	SINAD	SFDR
1ksps	85.56	-103.61	85.49	107.4
4ksps	85.03	-99.30	84.87	105.8
10ksps	86.08	96.88	85.73	106.8

First order filter: $R_{FLT}=10k\Omega$, $C_{FLT}=820pF$ (dBc)

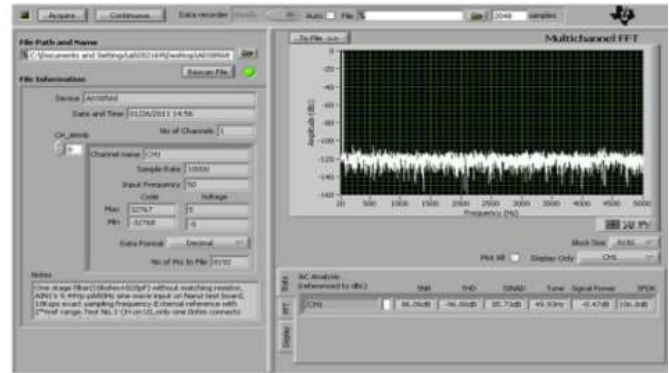
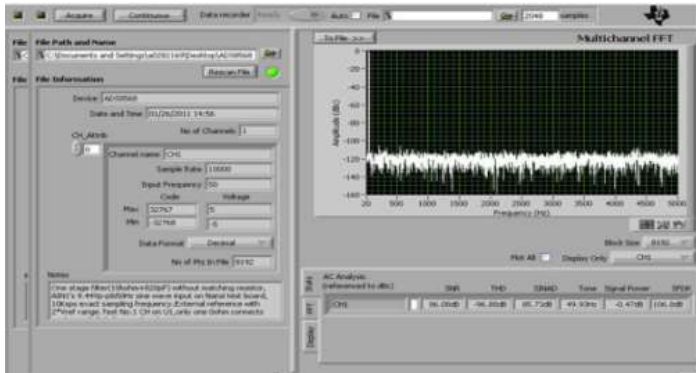
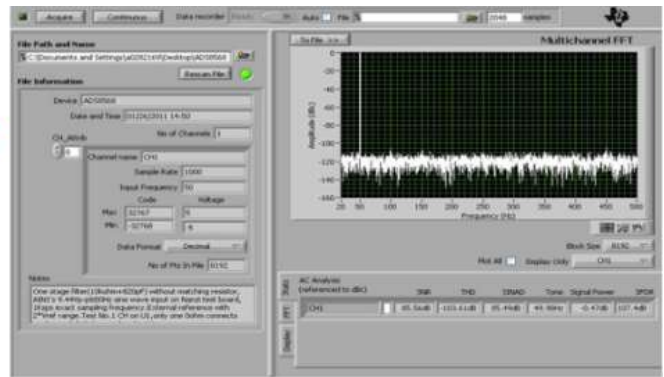


Figure 7: Test result with settling improvement

There are a variety of ways to resolve the settling challenge. However, these two methods are the simplest. Pay special attention to signal settling when designing a SAR ADC data acquisition system. Have you resolved the settling challenge in a different way? Leave a comment below on how you found success or what you tried that didn't work.

Additional resources

- [Learn more about designing with ADCs in the Data Converter Learning Center.](#)
- See a [SAR ADC applied](#) in five TI Designs reference designs, optimized for various industrial data acquisition applications.
- [Watch this short video](#) to get to know TI's [SAR ADC](#) portfolio.



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