How to Design Transistor Switching Circuits

MANNY HOROWITZ

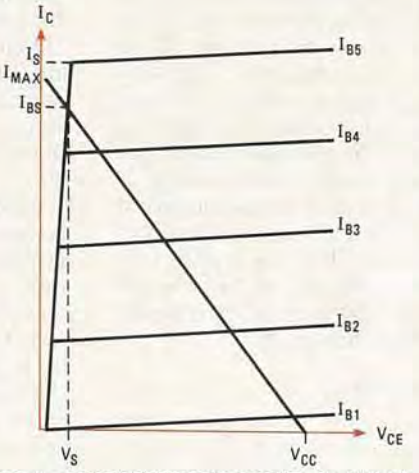

FIG 1.—CHARACTERISTIC CURVE of a typical bipolar transistor.

This month we'll learn how to design switching circuits using transistors, as well as other devices.

WE'VE ALREADY LEARNED ABOUT HOW transistors and other solid-state devices are used in circuits such as amplifiers, oscillators, etc. There are, of course, many other applications for those devices. One of the most common, and useful, of those applications is in electronic switching circuits. Unlike analog circuits where the output signal is some function of the input, in switching circuits the output is in one of only two states—on or off. This month, we are going to begin our look at electronic switching circuits, beginning with the most basic of them, the transistor switch.

Transistor switches

To use a transistor as a switch it must be biased so that the device is in either one of two states. In one of those states, the transistor is "off" and no collector current flows. In the other, the transistor is "on" and the collector current is limited only by the resistances in the emitter and collector circuits.

There are three common ways to bias a transistor so that it operates as we just described. Those methods of biasing are refered to as modes of operation. In what is referred to as the *saturated mode* of operation, the transistor is turned on by biasing it so that it is in, as you might have guessed, saturation. When that happens, the voltage across the transistor, called the saturation voltage, is at a minimum and depends on the collector current and load resistance. The device is turned off by biasing it so that it is in cutoff.

When a transistor is turned on in the second mode of operation, the *current mode,* it is biased so that the transistor operates near, but not quite in saturation. The collector-emitter voltage is somewhat above the saturation voltage of the device. Once again, the transistor is turned off by biasing it so that it is in cutoff.

Switching speed is faster in the current mode of operation than it is in the saturated mode. It is still faster, however, when the transistor is used in the *avalanche mode*. In that mode, the on and off states of a transistor are maintained in the breakdown portion of its curve. The switching speed of a transistor in the avalanche mode is exceeded only when tunnel, snap-off, hot-carrier, or pin diodes are used as the switching devices.

Switching modes

A transistor's characteristic curves can be approximated as shown in Fig. 1. Each curve (which here is shown as a relatively horizontal line) represents the relationship between the collector current, I_C, and the collector-emitter voltage, V_{CE}. You'll note that several of those curves are plotted in the figure. That's because the relationship between I_C and V_{CE} depends on the base current, I_B; each curve shows the relationship for a specific value of I_B.

The more-or-less vertical solid line near the vertical axis represents the saturation resistance of the transistor. That resistance is equal to V_S/I_S. At the maximum permissible transistor collector current, I_S, the minimum voltage that can be across the transistor is V_S, the saturation voltage. That voltage is reduced at lower collector currents.

A load line is also shown in the figure. It extends from V_{CC} on the V_{CE} axis to

I_{MAX} on the I_C axis. You'll note that even when the transistor is fully turned on by the application of a large current to the base, the collector current cannot reach I_{MAX} if the device's load line is as drawn in Fig. 1. The maximum current that flows is determined from the point where the load line crosses the saturation resistance curve. Collector current at the intersection of the two lines is at its maximum. It cannot be made any larger no matter how much the base current is increased.

Saturation and current modes of operation function only if a steady input voltage is applied to the base circuit of the transistor to keep it in either the on or off state. Examine the circuit shown in Fig. 2. The transistor is kept in the off state by the presence of $-V_{BB}$ at the base. That supply applies a negative voltage to the base with respect to the emitter. That negative voltage keeps the transistor turned off. When a sufficiently positive voltage is applied between the base and emitter at input V_{IN}, the transistor is on and collector current flows. Thus the applied voltages determine the state of the transistor and whether or not there is any collector current flowing through R_L.

Saturation mode

Switching is not instantaneous, especially in the saturation mode of operation. It takes time for the transistor to go from an off state to an on state as well as from an on state to an off state. Let's start our examination of the saturation mode by assuming the transistor is turned off. We'll be referring to Fig. 2 once again as we proceed through the following discussion.

When a positive pulse of voltage is applied to V_{IN}, it is also applied to the base of the transistor. That positive pulse causes base current to flow instantly, but there is a lapse of time before the base-emitter voltage reaches even a 0-volt level. Collector current, on the other hand, does not start to flow until the base-emitter voltage is just above zero. The time between the application of the positive voltage to the base and the instant that the collector current reaches 90% of its maximum, is referred to as the turn-on time. The phrase "delay time" is also used to describe that turn-on period.

After the positive input voltage has been removed, the negative ($-V_{BB}$) supply takes over to restore the transistor to an off state. But that does not occur instantly. First, the base current becomes negative for a while, but eventually the base-emitter junction ceases to conduct current in either direction. As for the base-emitter voltage and collector current, they remain positive for a short interval after the positive switching voltage has been removed. The time it takes for the collector current to drop to 90% of its maximum after the positive voltage has been removed is called storage time. It is caused by the capacitances formed in the transistor when it is in saturation. Those capacitances are charged when the transistor conducts and discharged relatively slowly after the transistor has been turned off.

Capacitor C_B is not an essential component in the circuit. It is included only to increase the switching speed. To determine what its capacitance must be you must first determine the saturation current, $I_{C(SAT)}$, of the transistor; it is equal to V_{CC}/R_L. Next, calculate what R_X should be by setting it equal to V_{BB}/I_{CBO} where I_{CBO} is the collector-to-base leakage current when the transistor is operating at its maximum temperature. Continue the design by plotting the load line for the collector circuit as shown in Fig. 1. From that plot, estimate the approximate base current, I_{BS}, at the point where the load line crosses the transistor's saturation resistance curve. In Fig. 1, it is about midway between I_{B4} and I_{B5}. If the maximum voltage applied to the input of the circuit is $V_{IN(max)}$,

$$R_B = V_{IN(max)}/I_{BS} - I_{CBO}$$

Capacitor C_B is used to increase the positive drive on the transistor at the instant that V_{IN} is applied. Its capacitance can be calculated mathematically, but it is best that the circuit be built and different capacitors placed across R_B until it is determined which capacitor will provide you with reasonable performance in a particular switching application.

Another factor that you may run into when designing a switching circuit is latch-up. In that situation, the reverse voltage applied to the base circuit is insufficient to bring conduction down to its lowest level. Instead, collector current drops only to some level above the desired minimum. That low current is determined by the point where the load line crosses the breakdown section of the collector curve. (The breakdown portion of the curve is illustrated in Fig. 3. It is the vertical sections of curves 1, 2 and 3.) Should latch-up occur, increase the negative or reverse-bias voltage that is applied to the base circuit.

Current mode

To improve the switching speed of a transistor it should be kept out of saturation when turned on. When that is done, the transistor is said to be operating in the current mode. In that mode of operation, the off states are identical to those in the saturated mode, while the on states differ in that in the current mode the transistor is kept just slightly out of saturation. (The excess charge in the base is kept to a minimum.)

In the current mode of operation, the transistor can be kept off by a resistor-battery combination connected between the base and ground. That is shown in the current-mode switching circuit shown in Fig. 4. Note that there is also a resistor-battery-diode combination in the emitter circuit of the transistor; let's take a closer look at it.

Diode D1 is kept turned on at all times because of the polarity of the V_{EE} supply. If a silicon junction diode is used, about 0.7 volt is across the device. If there is no voltage between ground and the base,

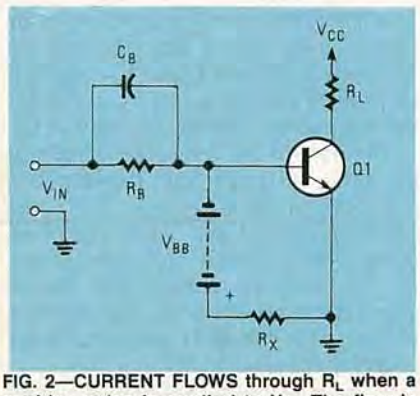

FIG. 2—CURRENT FLOWS through R_L when a positive pulse is applied to V_{IN}. The flow is stopped when that pulse is removed.

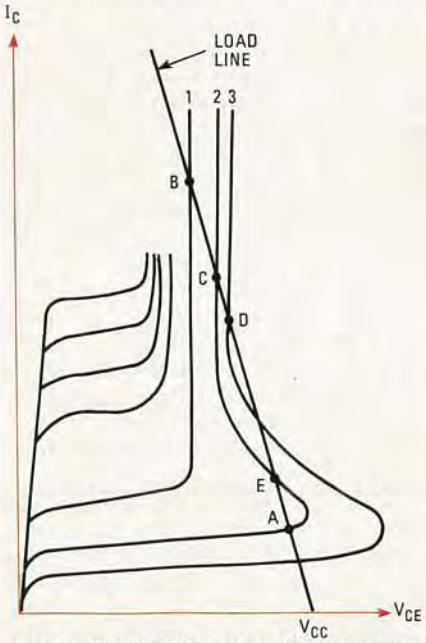

FIG. 3—IN THE AVALANCHE switching-mode transistors operate in the breakdown region of their characteristic curves.

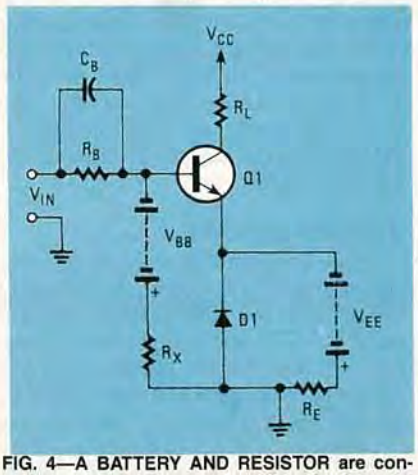

FIG. 4—A BATTERY AND RESISTOR are connected between the base and ground in a current-mode switching circuit.

only that diode voltage would be between the base and emitter of the transistor, keeping it turned on. But the transistor does get turned off due to the presence of the $-V_{BB}$ supply. To keep the transistor turned off, V_{BB} must be large enough to counter the voltage across the diode.

The real significance of the emitter circuit is seen when the transistor is turned on by a positive pulse at V_{IN}. If there's only a resistor in the emitter circuit, or a short as in Fig. 2, the collector current will be equal to the beta of the transistor multiplied by the base current I_{IN}. If I_{IN} is sufficiently large, the collector current can be driven into saturation. But the presence of D1, R_E and V_{EE} in the emitter circuit prevents that from happening so that the maximum transistor current level is less than its saturation current. That maximum is set by the components in the emitter circuit.

Because of the orientation of the diode in the circuit, no current from the emitter can flow through it. But it does limit the current through R_E because of the 0.7 volt developed across the diode. The current flowing through R_E is the maximum current that can flow through the emitter or collector circuit of the transistor. With that as the current limit when the transistor is turned on, the transistor will stay out of saturation if V_{CC}/R_L is greater than is the current in R_E. For practical purposes, the current through R_L should be limited to a maximum of V_{EE}/R_E.

Avalanche mode

In current- and saturation-mode switching, a voltage with a specific polarity must be maintained at the base of the transistor to keep it either in an on or an off state. The relative polarity of the applied voltage depends on whether you want to keep the transistor turned on or off. In the avalanche switching-mode, however, an instantaneous pulse is all that is required to keep the transistor in either an on or off state. An additional advantage for that arrangement is that the circuit switches at almost the instant that the switching pulse is applied.

The circuit used in that mode of operation is basically the same as is used for the saturation mode (see Fig. 2). Now, however, C_B is not needed to improve the switching speed, for it is quite rapid even without the capacitor in the base circuit. In addition, the V_{CC} voltage in the avalanche mode of operation is quite high, so that operation of the transistor is in the voltage breakdown region of the collector characteristic. The characteristic curves in that breakdown region, along with the load line for R_L, are shown in Fig. 3.

Curve 1 shows the collector characteristics when the base current is 0 mA; curve 2 is the collector voltage-current relationship when the base current is somewhat negative. Curve 3 is for the case where the base current is very negative but within the region where the transistor will not be destroyed. (Reverse base current obviously depends to a large degree upon the reverse base voltage applied for test purpose to the base circuit.) Besides the load line, the other curves shown illustrate the usual transistor characteristics when the base current is positive. The latter group of characteristics is the one usually shown on data sheets.

When the transistor is idling, assume that the negative base voltage, $-V_{BB}$, is of such magnitude that the transistor idles at point a on curve 2. A positive voltage at V_{IN} will push the idling point to a second curve. That second curve is determined by the magnitude of the positive voltage applied to the base. If we assume that that curve is for $I_B = 0$, then the new idling point is at B on curve 1. It remains on that curve as long as a base voltage is applied. At the instant the positive voltage is removed, the on-point drops to point C on curve 2 because only $-V_{BB}$ remains to bias the base-emitter junction. The transistor keeps idling at that point despite the absence of any voltage or additional pulse. It is stable because the slope of the load line, $1/R_L$, is less than the slope of the transistor curve. Ordinarily, a point on that portion of the curve would not be stable because of the transistor's negative resistance. But in this case, operation does not shift from point C because of the relative slopes of the load line and transistor curve.

A negative pulse must be applied to the circuit in order to turn the transistor off or to lower the collector-current level. If the negative pulse is of sufficient magnitude, the collector current will drop to point D on curve 3. When idling there, the transistor remains turned on. But at the instant the negative pulse is removed, operation reverts to a point on curve 2. That point is point E. Because the slope of the transistor curve around point E is less than the slope of the load line, the transistor cannot remain in an idling condition at that point. If the transistor is idling in the off state, it reverts rapidly to point A, the starting point. Here, current is at a minimum and the transistor is effectively turned off.

Switching FET's

Even though their switching speed is slower than that of bipolar devices, FET's have the advantage of superior on-to-off current ratios. The slower switching speed is due to the FET's large internal capacitances.

The characteristic curves of an n-channel FET, and the load line for the drain circuit, are shown in Fig. 5. Although the curves shown are not of any particular device, they can be used to describe the switching action of the FET in general. A schematic of an FET switching circuit is shown in Fig. 6.

With no positive voltage applied at V_{IN}, a negative voltage exists between the source and gate due to the $-V_{GG}$ supply.

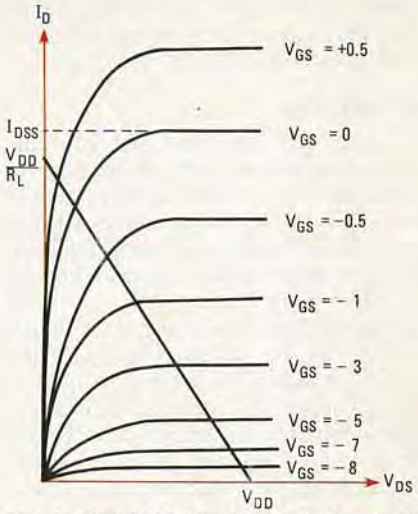

FIG. 5—THE CHARACTERISTIC CURVES of a typical FET, as well as a load line for the device, is shown here.

If that voltage is more negative than −8 volts (that is the pinch-off voltage for the device we are examining) very little current flows through the drain circuit. This can be found from the curves; note that I_D is very low when $V_{GS} = -8$. Thus, drain current is negligible because the transistor is operating in the pinch-off region.

A positive voltage at V_{IN}, or 0-volt at the gate, puts the operation of the transistor at the upper end of the I_D range where conduction is at a maximum. No matter what the collector load is, current flows through it.

FET switches can be considered in another way. When the transistor current is at a minimum, operation is in the pinch-off region (the right hand section of the curves). Because the curves there are almost parallel to the x-axis, the drain resistance is extremely high. That high resistance limits the drain current to minute levels.

Once it has been turned on, the FET operates in the ohmic region (the left-hand portion of the curves). In the ohmic region the characteristic is almost vertical and the drain resistance is extremely low, permitting relatively large amounts of

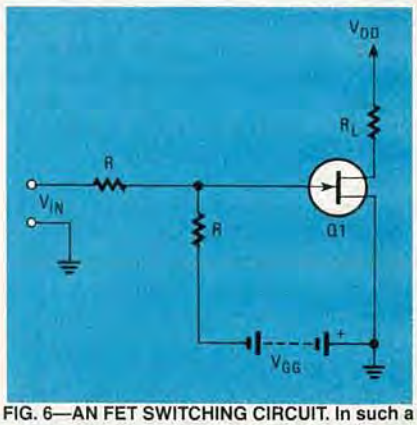

FIG. 6—AN FET SWITCHING CIRCUIT. In such a circuit, the ratio of the on and off resistances is very high.

drain current to flow. Those respective on and off resistances make the on-to-off current ratio of an FET extremely high.

IC switches

The 555 IC has been used as a time delay switch (among other things) for over a decade. Its operation revolves around three circuits—a comparator, an S-R flip flop, and an inverter. The comparator can be an op-amp without a feedback circuit, as shown in Fig. 7-a. In the circuit, a fixed voltage is applied to one input terminal while a variable voltage is applied to the other. Whether the output will be at $+V_{CC}$ or at $-V_{CC}$, the positive or negative supply voltage, depends upon the relative magnitudes and polarities of the voltages applied to the two input terminals. Note that in some circuits, $-V_{CC}$ is set equal to 0 volts, so that the output from the op-amp will vary from 0 to $+V_{CC}$.

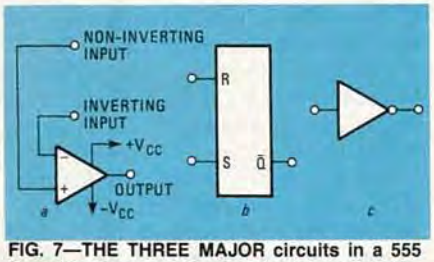

FIG. 7—THE THREE MAJOR circuits in a 555 timer IC. They are a comparator (*a*), an S-R flip-flop (*b*), and a NOT gate (*c*).

Suppose a fixed +5 volts is applied to the non-inverting input of the comparator and less than +5 volts (or even a negative voltage) is applied to the inverting input; then the output will be $+V_{CC}$ volts. Should the voltage at the inverting input be greater than +5, regardless of how little, the output becomes $-V_{CC}$. In a similar fashion, if the inverting input is set at a fixed +5 volts, the output is minus V_{CC} when the voltage at the non-inverting input is less than +5 volts, and is $+V_{CC}$ when the voltage at the non-inverting input is higher than +5 volts.

To sum up, the comparator compares the respective voltages at its input terminals. If the voltage at the non-inverting input is greater than that at the inverting input, the output is $+V_{CC}$, and if the voltage at the non-inverting terminal is less than that at the inverting terminal, the output is $-V_{CC}$. The change in polarity at the output occurs when the two input voltages are identical.

The second circuit in the IC is an S-R flip-flop; it is shown symbolically in Fig. 7-b. By itself, a flip-flop is a switch that's made up of digital logic circuits. In the type of flip-flop considered here, when the S terminal is low while the R terminal is high (the actual voltage levels for the high and low depend upon the flip-flop), the $\overline{Q}$ output is high. Should the conditions at the R and S inputs be reversed, the $\overline{Q}$ output is low.

Next, let's look at what happens when an input that's high is taken low again. Say, for instance, that the R input is high and the S input is low. When the R input is taken low again, the $\overline{Q}$ output does not go low again as you might expect; instead it is latched high and will remain so until the S input is taken high. If the conditions were reversed (i.e. the S input high and the R input low) the $\overline{Q}$ output would remain low until the R input is taken high. When both inputs are low the output remains in its previous state. Thus, this flip-flop can act as a switch. To change the state at the output all you need to do is reverse the states of the voltages at the inputs. In this type of flip-flop, care should be taken to prevent both inputs from being taken high at the same time.

The third circuit in the 555 is an inverter, often called a NOT gate; the symbol for that circuit is shown in Fig. 7-c. It gets its name from the fact that its output is the inverse of its input. Specifically, when the input to the gate is high the output is low, and vice versa.

A functional block diagram of a 555 is shown in Fig. 8. In it you can see how the three circuits we've just discussed are used in that device. The IC is idling when a voltage higher than $2V_{CC}/3$ is applied to pin 2. A 0.01-μF capacitor is usually connected between pins 5 and 1; that stabilizes the DC voltage at the input to comparator A. The switched voltage from the IC is developed across a load resistor, R_L, or some other device. That load is connected between pins 3 and 8.

In addition to the above, an R-C timing network is connected between pins 8 and 1, with the junction of the resistor and capacitor connected to pin 6. The time it takes to charge the capacitor is instrumental in determining the time it takes for the output to switch from a high to a low state. The charging process can take place only after a negative pulse has been applied to pin 2. Pin 7 is connected to pin 6 so that the capacitor will discharge after the internal transistor, Q1, connected to pin 7 has been turned on. All of the external components and connections we've discussed are shown in Fig. 9.

Before power is applied to pin 5, it is at ground potential because the capacitor connected there is fully discharged by the two identical internal resistors that run from it to ground. A slight potential may exist at pin 6 because the "hot" terminal of the capacitor in the timing circuit, C_T, is brought only close to ground potential through the internal discharging transistor (Q1 via pin 7), but is never precisely at ground. The slight voltage on the capacitor is due to the existence of a saturation voltage in the discharging transistor, just as it exists in any other transistor. That voltage, however small, is always across

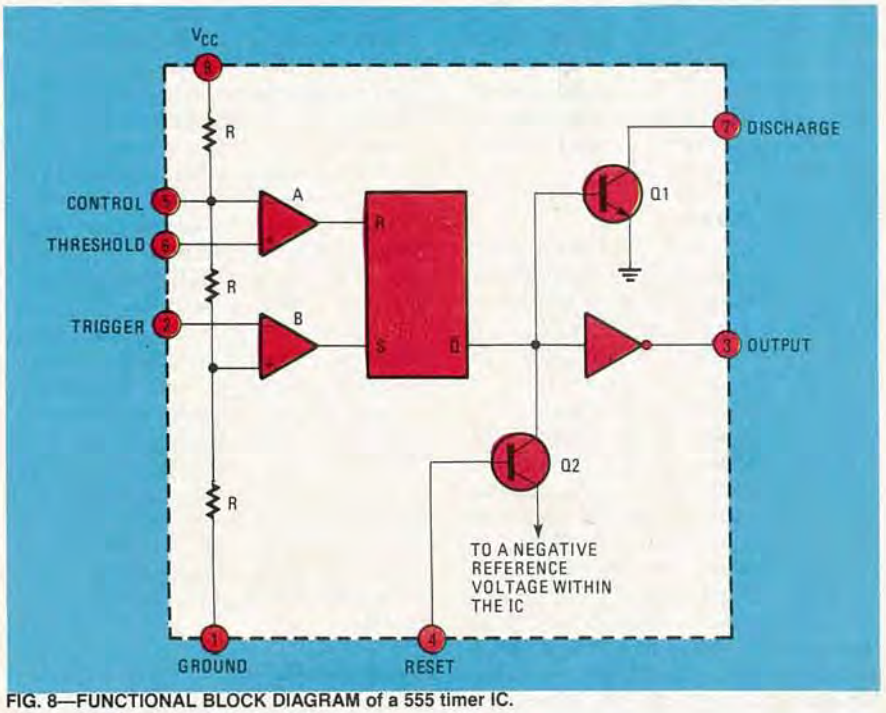

FIG. 8—FUNCTIONAL BLOCK DIAGRAM of a 555 timer IC.

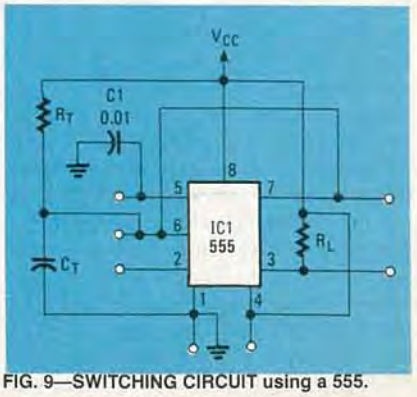

FIG. 9—SWITCHING CIRCUIT using a 555.

the transistor, and is consequently across the capacitor. As a result, voltage at the output of op-amp A is high at the instant that power is applied to the circuit.

Voltage at the output of op-amp B is at zero because when power is initially applied to the device, the non-inverting input of that op-amp is again grounded through an internal resistor in the IC. At the same time, the inverting input, which is tied to pin 2, is held at some value above $2V_{CC}/3$ as discussed above. That condition is one that must be satisfied if the 555 is not to be triggered.

The outputs from op-amps A and B are applied to the R and S inputs of the flip-flop respectively. Thus, when the output from op-amp B is low and the output from op-amp A is high, the $\overline{Q}$ output of the flip-flop is high. But the signal available at pin 3 of the 555 is low; that's because the output from the flip-flop is passed though the NOT gate before it is fed to pin 3. The discharge transistor, Q1, is turned on by the high voltage at $\overline{Q}$. The transistor shorts the timing capacitor, to maintain the status quo of the circuit and keep the output low.

The initial low output level from the IC is maintained from the time that power is applied to the circuit until a negative pulse is applied to the trigger input, pin 2. That status quo is maintained because almost immediately following the application of power, the supply voltage is applied, via a resistor, to the inverting input of op-amp A. Because of that, a low is applied to the R input of the flip-flop. As for op-amp B, its output is maintained low because the idling voltage from the trigger input, pin 2, which is high, is applied to the non-inverting input of that op-amp. As low voltages are at the R and S inputs of the flip-flop, the output from the IC cannot change states; it remains low. The discharge transistor remains turned on until the S input goes high.

When a short negative pulse with a voltage of less than $1/3V_{CC}$ is applied to pin 2, op-amp B's output goes high and that signal is applied to the S input of the flip-flop. That brings $\overline{Q}$ low. The low signal is subsequently inverted by the NOT gate and is available as a high at pin 3 of the 555. In the meantime, the low at the $\overline{Q}$ output of the flip-flop, which is connected directly to Q1, turns that discharging transistor off. That, in turn, removes the short from across the timing capacitor, C_T, allowing it to charge. When voltage across C_T exceeds the voltage at pin 6, or is more than $2/3V_{CC}$, the state of op-amp A changes and a high appears at its output. (The output from op-amp B went low immediately after the trigger pulse was completed.) That brings $\overline{Q}$ high, the output at pin 3 low, and the discharging transistor is once again turned on to discharge the timing capacitor.

The time it takes for the capacitor to charge and trip the circuits is $1.1R_TC_T$ seconds. During that time, voltage at the output is high. It stays there until the charging period has been completed. The capacitor is then discharged, the output becomes low, and the circuit awaits the next negative pulse to start the next timing cycle.

The charging cycle of the capacitor can be disturbed only by placing a low voltage pulse at the reset input of the IC, pin 4. That pulse turns on transistor Q2, which, in turn, turns on the discharging transistor. If the reset terminal is not to be used, it should be connected to a fixed high voltage such as the $+V_{CC}$ supply.

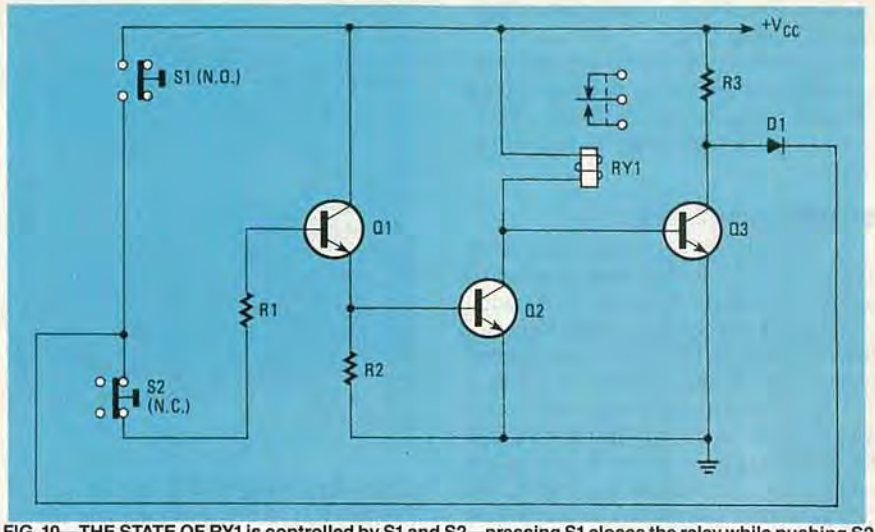

FIG. 10—THE STATE OF RY1 is controlled by S1 and S2—pressing S1 closes the relay while pushing S2 opens it.

Latching relay

Circuitry can be built around a mechanical relay so that its operation is controlled by a pair of momentary switches. Closing one switch closes the relay and closing the second switch opens it. A transistor circuit that can be used to accomplish that goal is shown in Fig. 10. When S1 is pressed, current flows through the the relay's coil and the contacts close. When S2 is pressed, the current ceases to flow and the contacts open. Of course, a normally closed relay could be used in place of RY1; in that case the action of the relay is reversed.

Let's start our look at the circuit by assuming that S2 has been pressed for an instant, thereby opening the circuit to the base of Q1. No current flows through it or through Q2, so that the supply voltage, $+V_{CC}$, is at the collector of Q2. This voltage is there because, in the absence of current, there is no voltage drop across the coil of the relay. The high voltage at the collector of Q2, and hence at the base of Q3, turns on the latter transistor. Collector current through Q3 is limited only by R3. Because of the voltage drop across R3, there is close to 0 volt at the collector of Q3. That is fed back and causes 0 volt to also be applied to the base of Q1, keeping both Q1 and Q2 turned off so that current does not flow through the relay coil.

Current will flow through the relay coil after S1 has been pressed momentarily. When that is done, $+V_{CC}$ is applied for an instant to the base of Q1. That turns on Q1 as well as Q2. Because Q2 then conducts, current flows through the relay coil. A voltage, very close to zero, is at the collector of Q2 due to the voltage drop across the transistor. That is also applied to the base of Q3 but is insufficient to turn that device on. The collector voltage of Q3 is high because there is no voltage drop across R3. That relatively high voltage is applied through D1, S2, and R1, to the base of Q1, keeping it and Q2 turned on.

Multivibrators

Two switching transistors are used to form a multivibrator. In their stable states, one transistor is turned on and one is turned off. The purpose of a multivibrator is to switch (and possibly even keep switching) the stable states of the two devices. To accomplish that, positive feedback is placed around the two transistors so that the circuit becomes unstable. That instability must be present if the states of the transistors are to be interchanged.

There are three basic types of multivibrator circuits. In one of those, the bistable multivibrator, both transistors are in stable states—one transistor is on and the second one is off. When a pulse is applied to the circuits, the states of the device reverses. The transistors remain in their new states until another pulse is applied; that once again reverses the states of the devices.

The second group of multivibrators are monostable. Here, the two transistors assume specific states, depending upon the circuitry. States are interchanged after a pulse has been applied but they do not remain indefinitely in those new states. After a period of time, the transistors in the monostable multivibrator revert to their original states. The time they remain

in the switched state depends upon a time constant in the circuit.

The last group of circuits are referred to as astable multivibrators. In those circuits no pulse is required to cause the transistors to change states; they do so continuously.

Bistable multivibrator

A bistable multivibrator circuit is shown in Fig. 11. Assume that when power is applied Q1 is on and in saturation while Q2 is turned off. If that is the case, the collector of Q1 is at about ground potential while the collector of Q2 is at $+V_{CC}$. Transistor Q2 is kept off because no current is supplied to its base through R_F2; that's because of the 0 volts at the collector of Q1. At the same time, the $-V_{BB}$ supply is applying a reverse bias voltage to the base through R_B2. Transistor Q1 is kept turned on despite the fact that the $-V_{BB}$ supply is applied to its base. That is because there is a current flowing through R_F1; that current is due to the voltage at the collector of Q2. The states of Q1 and Q2 are interchanged if a negative pulse is applied to the base of Q1 to turn it off while Q2 gets turned on. After that, the transistors remain in their newly acquired states. A similar change of states can be accomplished by applying a positive pulse to the base of Q2 to turn it on.

For the circuit to behave as described, several design criteria must be satisfied.

1. The values of R_C1 and R_C2 (as they are identical we'll simply refer to their value as R_C from now on) must be less than $V_{CC}/I_{C(sat)}$. $I_{C(sat)}$ is the minimum saturation current of the transistor.
2. Assume that $R_B1 = R_B2 = R_B$. To keep the off transistor in that state, V_{BB}/R_B must be greater than the leakage current, I_{CBO}, of the off transistor at the maximum temperature at which it is to be used.
3. Assume that $R_F1 = R_F2 = R_F$. For the transistor to be in saturation, beta multiplied by R_C must be greater than R_F. The Beta of both transistors should be about the same.
4. To keep the on transistor in saturation, the base current must be

$$\frac{I_{C\ (sat)}}{\beta\left(\frac{V_{CC}}{R_C + R_F} - \frac{V_{BB}}{R_B}\right)}$$

Monostable multivibrator

A monostable multivibrator is shown Fig. 12. In that circuit, Q1 is kept turned on because the $+V_{CC}$ supply provides base current to that transistor through R_B1. Transistor Q2 remains off because of the negative voltage applied to its base from the $-V_{BB}$ supply. Those states are interchanged after a negative pulse has been applied to the base of Q1. When such a pulse is applied, Q1 is turned off and the voltage at the collector jumps to $+V_{CC}$.

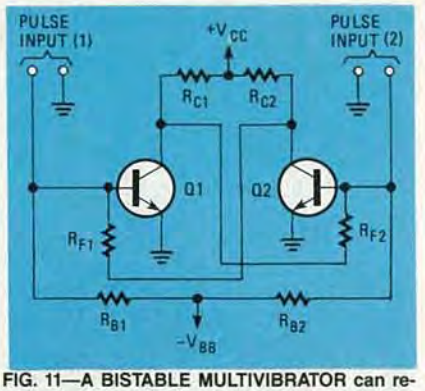

FIG. 11—A BISTABLE MULTIVIBRATOR can remain in either of two states for an indefinite period of time.

That voltage is applied to the base of Q2 through R_C1 and R_F, turning that device on. Transistor Q2 remains on until after capacitor C1 has had time to discharge through Q2 and R_B1. The time that Q2 remains on, is equal to about $0.69R_B1C1$. After that time, the transistors return to their original states.

For this circuit to perform properly, the following circuit details must be satisfied.

1. Q1 is on when V_{CC}/R_C1 is greater than $\beta(V_{CC}/R_B1)$.
2. From the transistor's specifications, determine the saturation voltage, $V_{CE(sat)}$, of Q2. If that information is not available, assume it to be 0.5 volt for a small signal transistor and 2 volts for a large power device. Use intermediate values for intermediate size devices. The base-emitter voltage, $V_{BE}1$, due to $V_{CE(sat)}$ is $V_{CE(sat)} \times R_B2/(R_F + R_B2)$. The base-emitter voltage, $V_{BE}2$, due to the $-V_{BB}$ supply, is $-V_{BB} \times R_F/(R_F - R_B)$. Q2 is off when $V_{BE}1 + V_{BE}2$ is negative.

Astable Multivibrator

The multivibrator behaves as an oscillator when used in an astable circuit. In that arrangement, both transistors are usually in identical circuits with the collector of one transistor coupled through a capacitor to the base of the second. The states of both devices keep changing from on to off, and back again, at a fixed rate. A basic arrangement of an astable multivibrator is in Fig. 13.

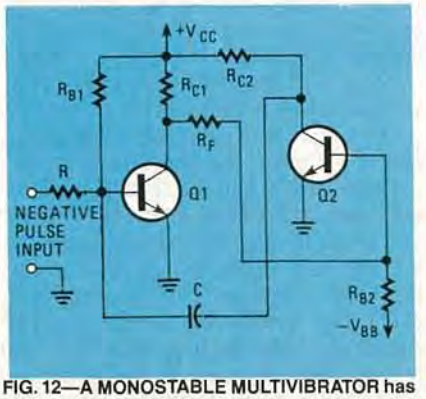

FIG. 12—A MONOSTABLE MULTIVIBRATOR has only one stable state.

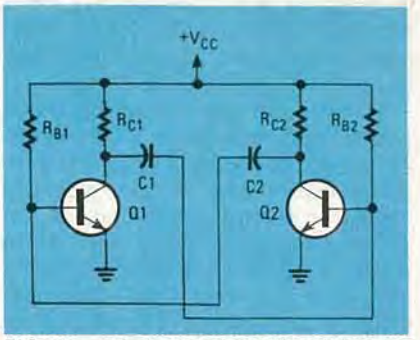

FIG. 13—AN ASTABLE MULTIVIBRATOR Changes states continuously.

Start by assuming that Q1 is turned fully on and is in saturation while Q2 is off. Because the collector of Q2 is at $+V_{CC}$, C2 charges to just under $+V_{CC}$, with the polarity as shown in the diagram. (The curved side of the capacitor represents the side at the lower potential.)

Capacitor C1 was charged, with the polarity as shown, during the previous half-cycle. When C1 is discharged, a base current flows in Q2 due to the current flowing through R_B2; the current in the resistor is caused by $+V_{CC}$. The presence of a base current turns Q2 on, putting its collector as well as the positive side of C2, at ground potential.

Because the voltage across C2 has the polarity shown, the base of Q1 is placed at a negative voltage with respect to ground. That turns Q1 off. While Q1 is off, C1 charges, with the polarity shown, to just under $+V_{CC}$, just as C2 did when the transistors were in their previous states. In the meantime, C2 is being discharged through R_B1 so there is no voltage left across C2 and thus none applied to the base of Q1. Transistor Q1 is turned on because the only major factors that now affect its base current are $+V_{CC}$ and R_B1. Transistor Q2 is turned off because of the negative voltage at its base. It is negative because the positive end of C1 is at ground potential after Q1 has been turned on.

The process continues without a stop. The time for switching from one state to the other is $0.69R_B1C2$ or $0.69R_B2C1$. If R_B1 is not equal to R_B2 and C1 is not equal to C2, then the time in which the transistors are in alternate states differ. Should $R_B1 = R_B2 = R_B$ and $C1 = C2 = C$, both switching times are identical. Fully symmetrical squarewave cycles will then be seen at the collector of either Q1 or Q2. The period of the full cycle is $1.38R_BC$ and the frequency will be $1/1.38R_BC$.

More switching devices

In this article, switching circuits using bipolar transistors, FET's, and IC's were described. But there are other semiconductor devices designed to perform as switching devices. Those include UJT's, SCR's, PUT's, and so on. Those and similar devices will be discussed in our next article. **R-E**