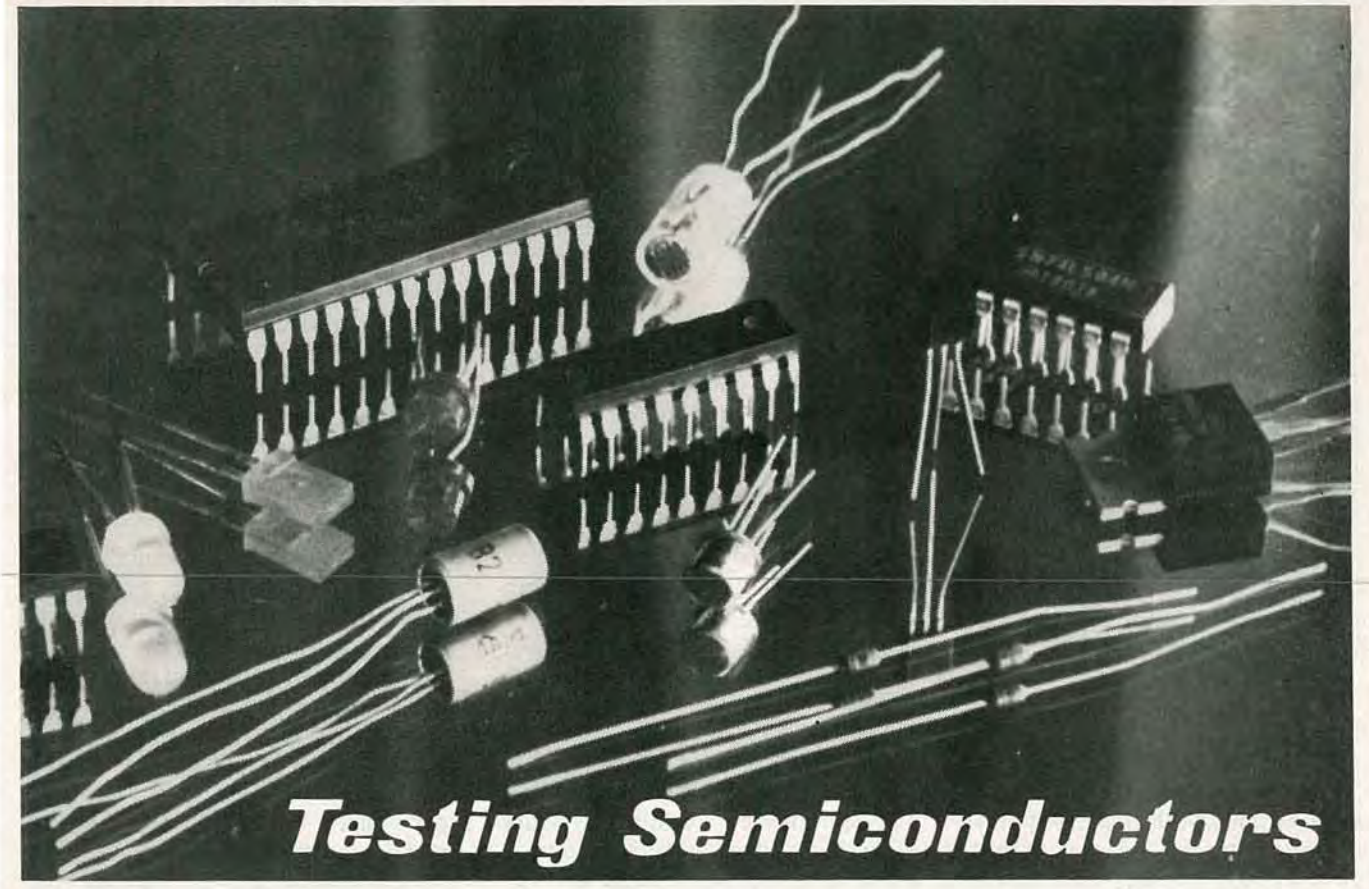

Testing Semiconductors

More on testing TTL devices, including low-power, high-speed, and Schottky types.

TJ BYERS

Part 9 LAST TIME WE EXamined the static (DC) characteristics of TTL gates. This month we will expand our discussion to encompass the entire family of TTL-compatible devices. That family includes five prominent members. They are standard TTL, low-power TTL (54L/74L00), high-speed TTL (54H/74H00), Schottky TTL (54S/74S00), and low-power Schottky TTL (54LS/74LS00). Each of those subfamilies within the TTL family serves to fill a specific characteristic that makes it more suitable for a given application.

Family traits

The patriarch of the family is, of course, the TTL gate. When there are no specific characteristics to fill, we often turn to TTL because it is readily available and inexpensive. TTL gates have moderate power consumption, good fan-out, and adequate operating speed for most applications.

The first two TTL subfamilies grew as a direct result of optimized TTL characteristics. The 54L/74L series capitalizes on the low-power aspects of TTL design, reducing typical gate power consumption by a factor of 10. Unfortunately, the operating speed of low-power TTL is only about ¼ that of standard TTL.

On the other hand, when emphasis is placed on speed, the price is power. A high-speed 54H/74H TTL gate can operate at up to twice the speed of standard TTL, but it consumes nearly 2½ times more power than a standard TTL gate, and 23 times more power than a 54L/74L gate.

The invention of Schottky TTL made possible devices that had both high speed and low power consumption. A standard Schottky TTL gate operates at about twice the speed of a high-speed 54H/74H TTL gate while consuming but ¾ the power.

Then a low-power version of the Schottky gate, the 54LS/74LS series, soon evolved from the original Schottky concept. That gate consumes only slightly more power than a low-power 54L/74L TTL gate while maintaining the speed characteristics of a standard TTL device.

Now the newest addition to the TTL family is a series of advanced Schottky TTL integrated circuits, designated as 54AS/74AS00 and 54ALS/74ALS00. Building on established Schottky TTL designs, those devices use improved construction techniques to enhance the speed of the already superior Schottky gate while reducing its power requirements. The specific switching speeds, as well as the typical power consumptions per gate for the entire TTL family, are listed in Table 1.

TABLE 1

Series	Propagation Delay	Power Dissipation	Frequency
54/74	10 ns	10 mW	35 MHz
54H/74H	6 ns	23 mW	50 MHz
54L/74L	33 ns	1 mW	3 MHz
54S/74S	3 ns	19 mW	125 MHz
54LS/74LS	9 ns	2 mW	45 MHz
54AS/74AS	1.7 ns	8 mW	200 MHz
54ALS/54ALS	4 ns	1.2 mW	70 MHz

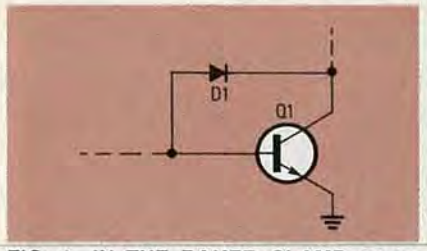

FIG. 1—IN THE BAKER CLAMP a germanium diode is placed across a transistor's base-collector junction.

Schottky TTL

Until the advent of Schottky TTL, all logic gates were pretty much the same internally, with emphasis put on certain features for speed or power. The first of the Schottky TTL devices to appear adhered to that design strategy with one important exception—they used Schottky transistors.

The Schottky transistor is what evolved from two earlier concepts: the *Baker clamp* and the *Schottky barrier-diode*.

The Baker clamp, as shown in Fig. 1, is a method of avoiding saturation in a discrete transistor. It has been established that saturated transistors take longer to switch from one state to another than do unsaturated transistors. Consequently, if the transistor can be prevented from going into saturation, the operating speed of the logic gate is improved.

The Baker clamp uses a germanium diode across the base-to-collector junction of the switching transistor to prevent saturation. The forward voltage drop of the germanium diode is 0.3 volt as compared to 0.7 volt for the base-emitter junction of a silicon transistor. When the transistor is turned on, base current drives the transistor toward saturation, decreasing the collector voltage. As the collector voltage drops, the germanium diode begins to conduct forward current, causing excess base-drive current to be diverted from the the base-emitter junction to the base-collector junction of the transistor. The result is that the transistor is held out of deep saturation, and the turn-off time is dramatically reduced.

Unfortunately, germanium does not integrate monolithically with silicon, making it impossible to use in silicon IC's. Therefore, the germanium diode must be replaced with a silicon equivalent that has a lower forward voltage drop than the base-collector junction of the transistor. A normal silicon p-n diode does not meet that requirement because its structure and forward voltage drop is identical to that of a silicon transistor. The Schottky-barrier diode, on the other hand, uses a metallic ohmic junction that gives the diode a lower forward-voltage drop, making it ideal for the application.

The Schottky diode is fabricated by depositing a metalization layer directly over the collector region, and tying it back to the base. The contact of the metal and the collector region forms a rectifying junction with a forward-voltage drop of about 0.4 volt, well below the 0.7 volt of the base-collector silicon junction. The arrangement is known as a Schottky transistor. A schematic of a typical Schottky gate is shown in Fig. 2.

Low-power Schottky TTL

The design of a low-power Schottky (LS) device varies somewhat from a traditional TTL design in that the input logic transistor does not have multiple emitters. Instead, Schottky barrier diodes are attached to the base of the input transistor, with each diode representing an input. A schematic of a typical low-power Schottky gate is shown in Fig. 3.

When a high is applied to either input of the gate, transistor Q1 receives base current from the 18K base resistor, which forces that transistor into conduction. When that happens, Q5 begins conducting, and as a result, Q4 is turned off, giving the gate a logic low output.

When a low signal is applied to either input of the device, the signal diverts some of Q1's base current through the input diode or diodes. Because the voltage drop across the Schottky-diode input is less than the base-emitter voltage (V_{BE}) of input transistor Q1, the transistor shuts off, causing the collector voltage to go high. That forces Q5 off and Q4 on, producing a high output signal.

That arrangement is essentially a modern version of DTL (*D*iode-*T*ransistor *L*ogic), a logic design that preceded TTL. Compared to the classic multi-emitter TTL structure, the low-power Schottky design is faster and dissipates less power.

All inputs are provided with Schottky clamping diodes, as shown in Fig. 3. Those diodes conduct when the input signal to the device goes negative, which limits undershoot and helps to control ringing.

The low-power Schottky series is functionally equivalent to standard

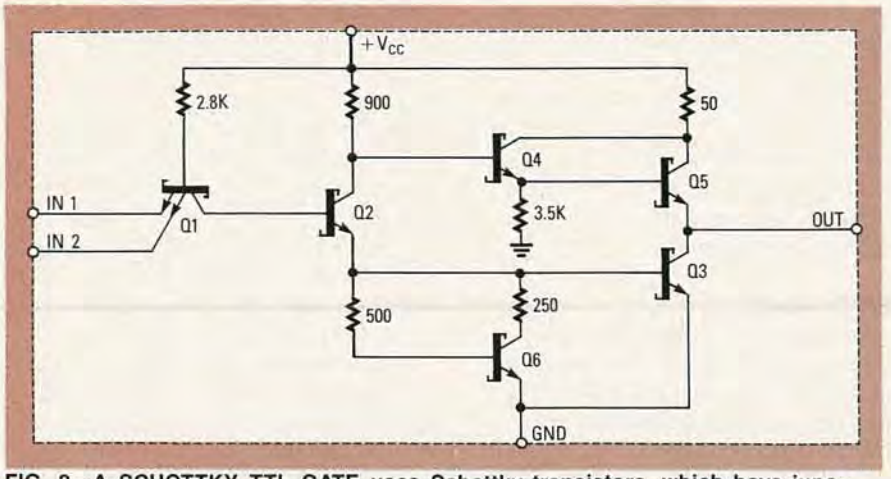

FIG. 2—A SCHOTTKY TTL GATE uses Schottky transistors, which have junctions having a lower voltage drop than that of standard silicon transistors.

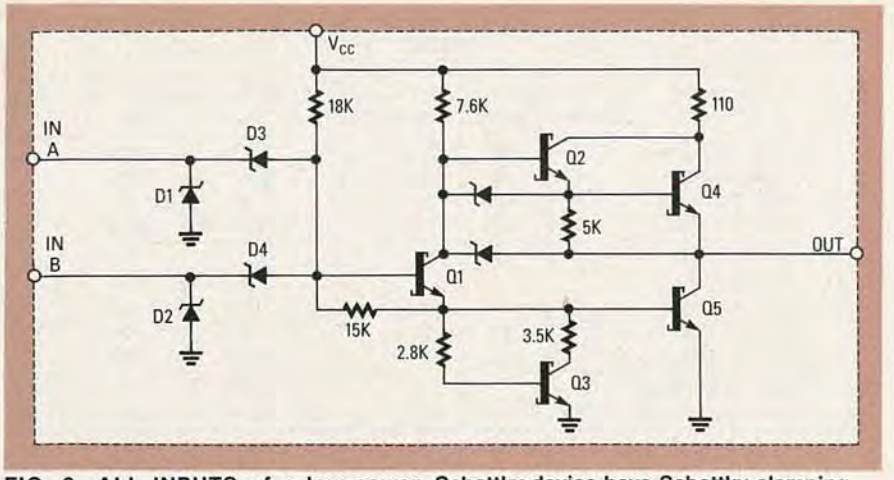

FIG. 3—ALL INPUTS of a low-power Schottky device have Schottky clamping diodes to control ringing.

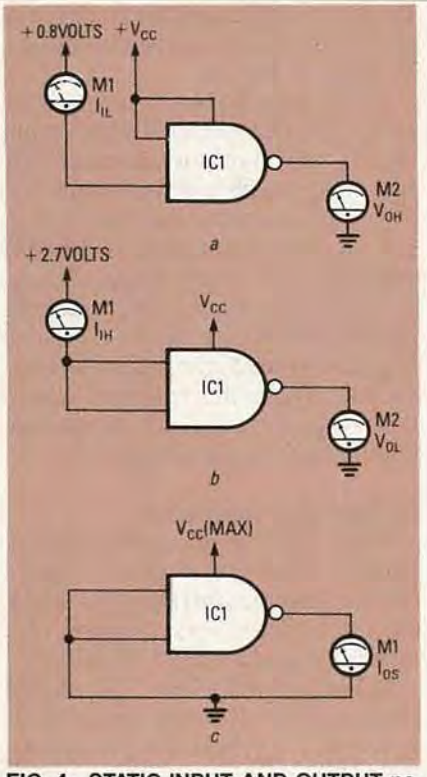

FIG. 4—STATIC INPUT AND OUTPUT parameters of standard, high-speed, and low-power TTL devices can be done using these circuits. The circuit in *a* tests I_{IL} and V_{OH}, the one in *b* tests for I_{IH} and V_{OL}, and the one in *c* tests for I_{OS}.

TTL, even in switching speed, but consumes typically one-fifth as much power. It's no wonder that it is the most popular TTL-type device.

Family feuds

It is quite possible to use more than one of the TTL subfamilies in a single system. An example might be where a high-frequency input signal is to be divided down to a lower frequency. There we might use a Schottky TTL in the front end of the divider chain, and standard TTL once the frequency has been scaled down.

But you must be very careful when mixing TTL logic. There is a wide variation in static parameters among the various TTL subfamilies.

Testing the static input and output characteristics of standard, low-power, and high-speed TTL devices can be done as described last time. Figure 4 shows a quick summary of the test circuits that are used and Table 2 shows typical results for each subfamily. Note that the test configurations are for negative (NAND, NOR) logic. To test positive logic devices (AND, OR), change the input levels accordingly.

Testing Schottky TTL

When testing 54S/74S00 TTL logic, remember that other than the use of Schottky-clamped transistors, the circuit configuration is basically the same as that of the other TTL families already discussed, and the device compares favorably with high-speed TTL. The only parameter that is different is the V_{OL} output voltage, which is typically 0.4 volt rather than 0.1 volt. Since that is still well below the maximum V_{IL} for a standard TTL gate, the 54S/74S series is fully compatible with other TTL logic.

With static testing of low-power Schottky and advanced Schottky TTL devices, what we have is an altogether different matter. Because of the modified input-circuit design, the input gates of those devices varies considerably from the norm.

Input characteristics

In general, most low-power and advanced Schottky input parameters can be measured using the techniques we explored last time; those include I_{IL}, I_{IH}, V_{IL}, and V_{IH}. The results of those measurements, though, are somewhat different.

Typically you will find that the input currents are considerably less than that of standard TTL. Typical values for I_{IH} and I_{IL} are 20 μA and 0.4 mA, respectively, as compared to 40 μA and 1.6 mA for TTL devices. That means that a standard 10-unit TTL driver can drive twice as many low-power Schottky gates as standard TTL gates.

Input voltages, on the other hand, tend to run a little lower because of the presence of the Schottky diodes. Where a TTL gate might trigger from high to low with a 1.4-volt input, the Schottky input may have to be reduced to 1.1 volts before a logic transition takes place. Since both values are well above the 0.8-volt maximum for V_{IL}, there is no significant difference in performance.

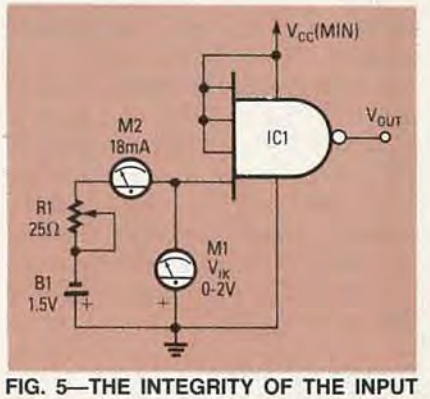

FIG. 5—THE INTEGRITY OF THE INPUT clamping diode can be tested using this setup.

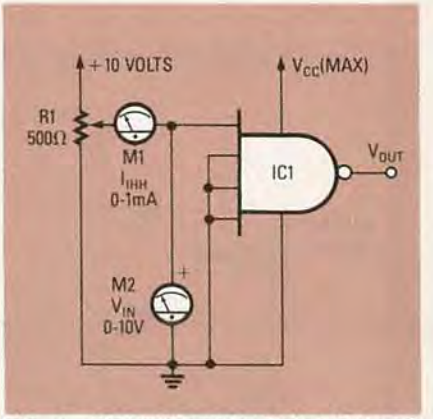

FIG. 6—INPUT BREAKDOWN VOLTAGE can be determined by applying 7 volts to an input and measuring the resulting input leakage current under worst-case power-supply conditions.

Measuring V_{IK}(MAX)

There is one test performed on low-power Schottky devices that is not performed on any other type of TTL logic. It a test for V_{IK}(MAX), the most negative voltage at an input when 18 mA is forced out of that terminal. That parameter guarantees the integrity of the Schottky input diode that is placed across the logic input and ground. Those diodes are normally reverse-biased and are there only to suppress transient currents.

Looking at Fig. 3, we see that as the input voltage to input A approaches ground, increasing amounts of current flow through D3 until it reaches I_{IL}. Beyond that point, the input voltage starts swinging negative, as would be the case if the input signal suffered from ringing. That effectively places ground at a positive voltage and the logic input at a negative voltage, forcing diode D1 into forward conduction. The input voltage is now clamped at the forward voltage drop of D1, which effectively dampens any ringing that may be present on the input signal.

The V_{IK}(MAX) parameter is measured using the test configuration shown in Fig. 5. In that circuit, only one input is tested at a time; all others are tied high. With V_{CC} set to V_{CC}(MIN), a −18-mA current from the 1½-volt battery is applied to the input under test. The current is set by adjusting potentiometer R1. The voltage between the input under test and ground is then measured in order to determine V_{IK}(MAX).

Breakdown voltage

Another consequence of using Schottky diodes for the logic input is an increase in the input breakdown voltage. The typical input breakdown voltage of a low-power Schottky gate is 15 volts or more.

However, testing for breakdown voltage is critical. Unlike the multi-emitter input of a standard TTL gate, which can sustain short periods of overload, the base-emitter junction of a Schottky transistor is small and can easily be over stressed by a transient caused by spikes on the input signal.

Two tests are used to measure input breakdown voltage. The simpler involves applying a voltage to the input and noting whether the device fails or not. That is commonly referred to as destructive testing because it renders the part useless.

More frequently, the gate input is subjected to an additional high-level input voltage and a leakage-current measurement is taken. Because there is a linear relationship between breakdown voltage and leakage current, the breakdown voltage of the input can be extrapolated by comparing the measured leakage current to already established guidelines.

The leakage measurement, which is unofficially called I_{IHH}, is done by applying 7.0 volts to an input under the worst-case power-supply voltage conditions and noting the results. The test configuration for measuring I_{IHH} is shown in Fig. 6.

In that test, the power supply is set to V_{CC}(MAX) and R1 is adjusted until a V_{IN} of 7.0 volts is achieved. Only one input can be tested at a time and all unused inputs are returned to ground. The current measured by M1 when V_{IN} is 7.0 volts is I_{IHH}. If I_{IHH} is greater than the maximum leakage current allowed for the device at that V_{IN}, it is assumed the input under test cannot sustain the repetitive breakdown voltages common to normal operation, and the part is rejected.

TABLE 2

Symbol	Parameter	54/74 Series	54H/74H Series	54L/74L Series	54S/74S Series	54LS/74LS Series	54AS/74AS Series	Units
I_{OH}	Output high current	400	500	100/200	1000	400	2000	µA
I_{OL}	output low current	16	20	2/3.6	20	4/8	20	mA
V_{OH}	output high voltage	3.4	3.5	3.2	3.4	3.4	3.0	V
V_{OL}	output low voltage	0.2	0.2	0.15/0.2	0.5	0.25/0.35	0.35	V
I_{IH}	input high current	40	50	10	50	20	20	µA
I_{IHH}	input high current					100	112	µA
I_{IL}	input low current	1.6	2	0.18	2	0.36	0.4	mA
V_{IH}	input high voltage	2	2	2	2	2	2	V
V_{IL}	input low voltage	0.8	0.8	0.7	0.8	0.8	0.8	V
V_{IK}	input clamp voltage					0.65	1.5	V
I_{OS}	short circuit current	18–55	40–100	3–15	40–100	6–40	60–224	mA

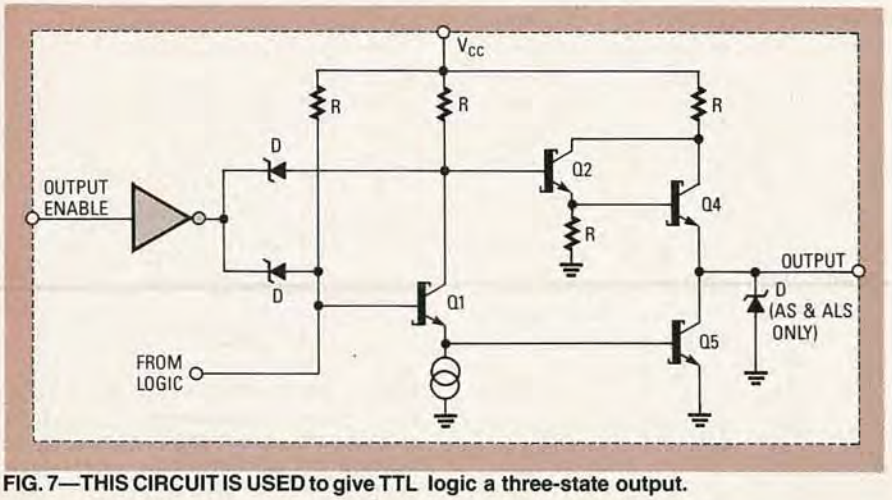

FIG. 7—THIS CIRCUIT IS USED to give TTL logic a three-state output.

Output characteristics

While low-power Schottky TTL retains the totem-pole output configuration we examined last time, the output circuitry has several features not found in conventional TTL devices.

Referring back to Fig. 3, note that the base of pull-down output transistor Q5 is returned to ground through Q3 and a pair of resistors instead of through a simple resistor. That arrangement is called a squaring network because it squares up the transfer characteristics of the logic transitions by preventing Q1 from conducting until the input voltage rises high enough to allow Q1 to supply sufficient base current to Q5 for a snappy transition.

The output pull-up circuit (Q2, Q4) is a Darlington circuit with the base of the output transistor returned to the output terminals through a 5K resistor. Compare that to the output circuit in 54H/74H and 54S/74S logic, which has its base returned to ground. The Darlington configuration con-

sumes less power while allowing the output to pull up to one V_{BE} below V_C for low values of output current. Note that 54AS/74AS and 54ALS/74ALS logic devices include a Schottky clamping diode across the output to control ringing on long signal lines.

Output characteristics I_{OL}, I_{OH}, V_{OL}, and V_{OH} are measured using the methods described last time, and are summarized in Fig. 4. Note, however, that the test parameters are changed slightly. Whereas V_{IL} is 2.4 volts for standard TTL, its value is 2.7 volts for Schottky devices. You will also find that Schottky output currents and voltages are slightly different than TTL. The differences are listed in Table 2.

Three-state output

An interesting twist was added to binary logic with the introduction of three-state logic. Conventional binary logic maintains that there are only two states for a logic device—its either on or off. Three-state logic, on the other hand, says that there may be three states: on, off, and "none" or high-impedance.

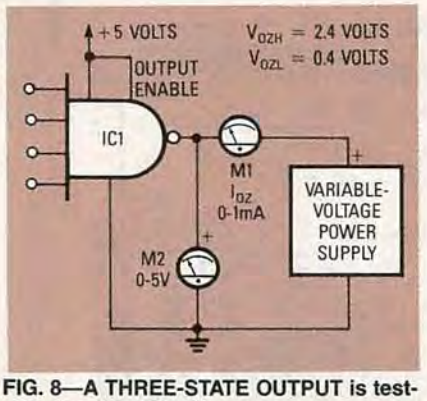

FIG. 8—A THREE-STATE OUTPUT is tested using this circuit.

In the none state, the output of the logic device is floated in a high-impedance mode. In essence, the gate is removed from the circuit without actually being physically removed.

The extra circuitry used to obtain the high-impedance output condition in three-state outputs is shown in Fig 7. When the OUTPUT ENABLE signal is high, both the phase-splitter transistor, Q1, and the Darlington pull-up pair, Q2 and Q4, are turned off. In that condition the output circuitry is nonconducting, which allows the outputs of two or more circuits to be connected together in a bus application in which only one output is to be enabled at any particular time.

Theoretically, no current flows either in or out of the output when it is in the three-state mode. Practically, some current does. Those currents are designated I_{OZH} and I_{OZL}.

I_{OZH} is the current that flows into a disabled three-state gate output with a specified high voltage applied to the output. I_{OZL} is the current that flows out of a disabled three-state gate output with a specified low voltage applied to the output. Both measurements are made using the test configuration shown in Fig. 8.

The gate is tested with the OUTPUT ENABLE pin tied high, placing the gate in the three-state mode. I_{OZH} is measured by applying 2.4 volts to the gate output, as indicated by M2, and reading the output current from M1. I_{OZL} is measured by applying 0.4 volts to the gate output and reading the output current from M1. Typical values for I_{OZH} and I_{OZL} are 20 μA and 0.4 mA, respectively. **R-E**