Ratings and Characteristics

Ratings are established for solid-state devices to help circuit and equipment designers use the performance and service capabilities of each type to maximum advantage. They define the limiting conditions within which a device must be maintained to assure satisfactory and reliable operation in equipment applications. A designer must thoroughly understand the constraints imposed by the device ratings if he is to achieve effective, economical, and reliable equipment designs. Reliability and performance considerations dictate that he select devices for which no ratings will be exceeded by any operating conditions of his application, including equipment malfunction. He should also realize, however, that selection of devices that have overly conservative ratings may significantly add to the cost of his equipment.

BASIS FOR DEVICE RATINGS

Three systems of ratings (the absolute maximum system, the design center system, and the design maximum system) are currently in use in the electronics industry. The ratings given in the RCA technical data for solid-state devices are based on the **absolute maximum system**. A definition for this system of ratings has been formulated by the **Joint Electron Devices Engineering Council (JEDEC)** and standardized by the **National Electrical Manufacturers Association (NEMA)** and the **Electronic Industries Association (EIA)**, as follows:

"**Absolute-maximum ratings** are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

"The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

"The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst possible operating conditions with respect to supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics."

The rating values specified in the technical data for RCA solid-state devices are determined on the basis of extensive operating and life tests and comparison measurements of critical device parameters. These tests and measurements define the limiting capabilities of a specific device type in relation to the rating factors being considered. The test and measurement conditions simulate, as closely as possible, the worst-case conditions that the device is likely to encounter in actual equipment applications.

Rating tests are expensive, time-consuming, and often destructive. Obviously, therefore, all individual solid-state devices of a given type designation cannot be subjected to these tests. The validity of the ratings is assured, however, by use of stringent processing and fabrication controls and extensive quality checks at each stage in the manufacturing process to assure product uniformity among all devices of a specific type designation and by testing of a statistically significant number of samples.

Ratings are given for those stress factors that careful study and experience indicate may lead to severe degradation in performance characteristics or eventual failure of a device unless they are constrained within certain limits.

All solid-state devices undergo irreversible changes if their temperature is increased

beyond some critical limit. A number of ratings are given for power transistors, therefore, to assure that this critical temperature limit will not be exceeded on even a very small part of the silicon chip. The ratings for power transistors normally specify the maximum voltages, maximum current, maximum and minimum operating and storage temperatures, and maximum power dissipation that the transistor can safely withstand.

In power transistors, the main design consideration is power-handling capability. This capability is determined by the maximum junction temperature a transistor can withstand and how quickly the heat can be conducted away from the junction.

In general, the basic physical theory that defines the behavior of any bipolar transistor in relation to charge-carrier interactions, current gain, frequency capabilities, voltage breakdown, and current and temperature ratings is not significantly different for power types. Power transistors, however, must be capable of large current densities and are required to sustain large voltage fields. For power types, therefore, the basic transistor theory must be expanded to include the effect that these conditions have on the physical behavior of the devices. In addition, the physical capabilities of power transistors must be defined in terms of factors, such as second-breakdown energy levels, safe operating area, and thermal-cycling stresses, that are not usually considered for small-signal types.

VOLTAGE RATINGS

Maximum voltage ratings are normally given for both the collector and the emitter junctions of a transistor. A V_{BEO} rating, which indicates the maximum base-to-emitter voltage with the collector open, is usually specified. The collector-junction voltage capability is usually given with respect to the emitter, which is used as the common terminal in most transistor circuits. This capability may be expressed in several ways. A V_{CEO} rating specifies the maximum collector-to-emitter voltage with the base open; a V_{CER} rating for this voltage implies that the base is returned to the emitter through a specified resistor; a V_{CES} rating gives the maximum voltage when the base is shorted to the emitter; and a V_{CEV} rating indicates the maximum voltage when the base is reverse-biased with respect to the emitter by a specified voltage. A V_{CEX} rating may also be given to indicate the maximum collector-emitter voltage when a resistor and voltage are both connected between base and emitter.

If a maximum voltage rating is exceeded, the transistor may "break down" and pass current in the reverse direction. The breakdown across the junction is usually not uniform, and the current may be localized in one or more small areas. The small area becomes overheated unless the current is limited to a low value, and the transistor may then be destroyed.

The collector-to-base or emitter-to-base breakdown (avalanche) voltage is a function of the resistivity or impurity doping concentration at the junction of the transistor and of the characteristics of the circuit in which the transistor is used. When there is a breakdown at the junction, a sudden rise in current (an "avalanche") occurs. In an abruptly changing junction, called a step junction, the avalanche voltage is inversely proportional to the impurity concentration. In a slowly changing junction, called a graded junction, the avalanche voltage is dependent upon the rate of change of the impurity concentration (grade constant) at the physical junction. Fig. 42 shows the two types of junction breakdowns. The basic transistor voltage-breakdown mechanisms and their relationship to external circuits are the basis for the various types of voltage ratings used by transistor manufacturers.

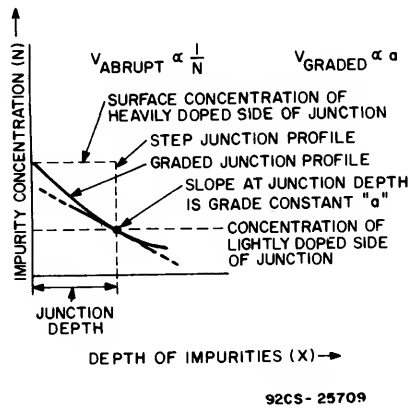


Fig. 42 - Step-junction and graded-junction breakdown.

CURRENT, TEMPERATURE, AND DISSIPATION RATINGS

The physical mechanisms related to basic transistor action are temperature-sensitive. If the bias is not temperature-compensated, the transistor may develop a regenerative condition, known as **thermal runaway**, in which the thermally generated carrier concentration approaches the impurity carrier concentration. [Experimental data for silicon show that, at temperatures up to 700° K, the thermally generated carrier concentration n_1 is determined as follows: $n_1=3.87 \times 10^{16} \times T \times (3/2) \exp(-1.21/2kT)$.] When this condition becomes extreme, transistor action ceases, the collector-to-emitter voltage V_{CE} collapses to a low value, and the current increases and is limited only by the external circuit.

If there is no current limiting, the increased current can melt the silicon and produce a collector-to-emitter short. This condition can occur as a result of a large-area average temperature effect, or in a small area that produces hot spots or localized thermal runaway. In either case, if the intrinsic temperature of a semiconductor is defined as the temperature at which the thermally generated carrier concentration is equal to the doped impurity concentration, the absolute maximum temperature for transistor action can be established.

The intrinsic temperature of a semiconductor is a function of the impurity concentration, and the limiting intrinsic temperature for a transistor is determined by the most lightly doped region. It must be emphasized, however, that the intrinsic temperature acts only as an upper limit for transistor action. The maximum operating junction temperature and the maximum current rating are established by additional factors such as the efficiency of heat removal, the yield point and melting point of the solder used in fabrication, and the temperature at which permanent changes in the junction properties occur.

The **maximum current rating** of a transistor indicates the highest current at which, in the manufacturer's judgment, the device is useful. This current limit may be established by setting an arbitrary minimum current gain or may be determined by the fusing current of an internal connecting wire. A current that exceeds the rating, therefore, may result in a low current gain or in the destruction of the transistor.

The basic materials in a silicon transistor allow transistor action at temperatures greater than 300° C. Practical transistors, however, are limited to lower temperatures by mounting systems and surface contamination. If the **maximum rated storage** or **operating temperature** is exceeded, irreversible changes in leakage current and in current-gain characteristics of the transistor result.

Junction-Temperature Ratings

The temperature of solid-state devices must be closely controlled not only during operation, but also during storage. For this reason, ratings data for these devices usually include maximum and minimum **storage temperatures**, as well as **maximum operating temperatures**.

The maximum allowable power dissipation in a solid-state device is limited by the temperature of the semiconductor pellet (i.e., the junction temperature). An important factor that assures that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device. For this reason, solid-state power devices should be mounted on a good thermal base (usually copper), and means should be provided for the efficient transfer of heat from this base to the surrounding environment.

When a solid-state device is mounted in free air, without a heat sink, the steady-state thermal circuit is defined by the **junction-to-free-air thermal resistance** given in the published data on the device. Thermal considerations require that there be a free flow of air around the device and that the power dissipation be maintained below that which would cause the **junction temperature** to rise above the maximum rating. When the device is mounted on a heat sink, however, care must be taken to assure that all portions of the thermal circuit are considered.

Solid-state power devices may also be adversely affected by temperature variations that result from changes in power dissipation during operation or in the temperature of the ambient environment. Such temperature variations produce cyclic mechanical stresses at the interface of the semiconductor pellet and the copper base to which the pellet is attached because of the different thermal-expansion coefficients of these materials. These thermally induced cyclic stresses may eventually lead to a wearout type of failure refered to as **thermal fatigue**.

In this section the thermal impedances that comprise the basic thermal circuit of a solid-state device are defined, the use and advantages of external heat sinks are described, and the effects of cyclic thermal stresses are analyzed. The basic principles explained are generally applicable to all solid-state power devices regardless of the particular type of device identified in specific examples.

Basic Thermal System

When current flows through a solid-state device, power is dissipated in the semiconductor pellet that is equal to the product of the voltage across the junction and the current through it. As a result, the temperature of the pellet increases. The amount of the increase in temperature depends on the power level and how fast the heat can flow away from the junction through the device structure to the case and the ambient atmosphere. The rate of heat removal depends primarily upon the thermal resistance and capacitance of the materials involved. The temperature of the pellet rises until the rate of heat generated by the power dissipation is equal to the rate of heat flow away from the junction; i.e., until thermal equilibrium has been established.

Thermal resistance can be compared to electrical resistance. Just as electrical resistance is the extent to which a material resists the flow of electricity, thermal resistance is the extent to which a material resists the flow of heat. A material that has a low thermal resistance is said to be a good thermal conductor. In general, materials which are good electrical conductors are good thermal conductors, and vice versa.

Power-Dissipation Ratings

Power is dissipated in the semiconductor material of a solid-state device in the form of heat, which if excessive can cause irreversible changes in the crystal structure or melting of the pellet. This dissipation is equal to the difference between the input power applied to the device and the power delivered to the load circuit. Because of the sensitivity of semiconductor materials to variations in thermal conditions, maximum dissipation ratings are usually given for specific temperature conditions.

In many instances, dissipation ratings for solid-state devices are specified for ambient, case, or mounting-flange temperatures up to 25° C. Such ratings must be reduced linearly for operation of the devices at higher temperatures. Fig. 43 shows a typical power-transistor derating chart that can be used to determine maximum permissible dissipation values at specific temperatures above 25° C. (This chart cannot be assumed to apply to transistor types

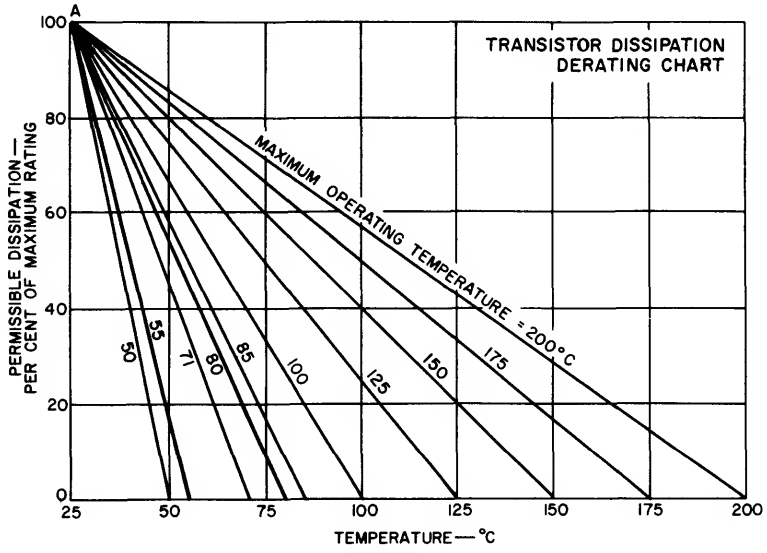


Fig. 43 - Chart showing maximum permissible percentage of maximum rated dissipation as a function of temperature.

other than the particular transistors for which it was prepared.) The chart shows the permissible percentage of the maximum dissipation ratings as a function of ambient or case temperature. Individual curves are shown for specific operating temperatures. If the maximum operating temperature of a particular transistor type is some other value, a new curve can be drawn from point A to the desired temperature value on the abscissa, as indicated by the dashed-line curves on the chart.

EFFECT OF EXTERNAL HEAT SINKS

The maximum allowable power dissipation in a solid-state device is limited by the temperature of the semiconductor pellet (i.e., the junction temperature). An important factor that assures that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device. For this reason, solid-state power devices should be mounted on a good thermal base (usually copper), and means should be provided for the efficient transfer of heat from this base to the surrounding environment.

Most practical heat sinks used in modern, compact equipment are the result of experiments with heat transfer through convection, radiation, and conduction in a given application. Although there are no set design formulas that provide exact heat-sink specifications for a given application, there are a number of simple rules that reduce the time required to evolve the best design for the job. These simple rules are as follows:

1. The surface area of the heat sink should be as large as possible to provide the greatest possible heat transfer. The area of the surface is dictated by case-temperature requirements and the environment in which the device is to be placed.

2. The heat-sink surface should have an emissivity value near unity for optimum heat transfer by radiation. A value approaching unity can be obtained if the heat-sink surface is painted flat black.

3. The thermal conductivity of the heat-sink material should be such that excessive thermal gradients are not established across the heat sink.

Although these rules are followed in conventional heat-sink systems, the size and cost of such systems often become restrictive in compact, mass-produced power-control and power-switching applications. The use of mass-produced prepunched parts, direct soldering, and batch-soldering techniques eliminates many of the difficulties associated with heat sinks by making possible the use of a variety of simple, efficient, readily fabricated heat-sink configurations that can be easily incorporated into the mechanical design of equipment.

For most efficient heat sinking, intimate contact should exist between the heat sink and at least one-half of the package base. The package can be mounted on the heat sink mechanically, with glue or epoxy adhesive, or by soldering. (Soldering is not recommended for transistors.) If mechanical mounting is employed, silicone grease should be used between the device and the heat sink to eliminate surface voids, prevent insulation buildup due to oxidation, and help conduct heat across the interface. Although glue or epoxy adhesive provides good bonding, a significant amount of resistance may exist at the interface resistance; an adhesive material with low thermal resistance, such as Hysol Epoxy Patch Material No. 6C or Wakefield Delta Bond No. 152, or their equivalent, should be used.

Types of Heat Sinks

Heat sinks are produced in various sizes, shapes, colors, and materials; the manufacturer should be contacted for exact design data. It is convenient for discussion purposes to group heat sinks into three categories as shown below:

1. **Flat vertical-finned types** are normally aluminum extrusions with or without an anodized black finish. They are unexcelled for natural convection cooling and provide reasonable thermal resistance at moderate airflow rates for forced convection.

2. **Cylindrical or radial vertical-finned types** are normally cast aluminum with an anodized black finish. They are used when maximum cooling in minimum lateral displacement is required, using natural convection.

3. **Cylindrical horizontal-finned types** are normally fabricated from sheet-metal rings and have a painted black matte finish. They are used in confined spaces for maximum cooling in minimum displaced volume.

It is also common practice to use the existing mechanical structure or chassis as a

heat sink. The design equations and curves for such heat sinks based upon convection and radiation are shown in Figs. 44, 45, and 46.

A useful nomograph which considers heat removal by both convection and radiation is given in Fig. 47. This nomograph applies for natural bright finish on the copper or aluminum.

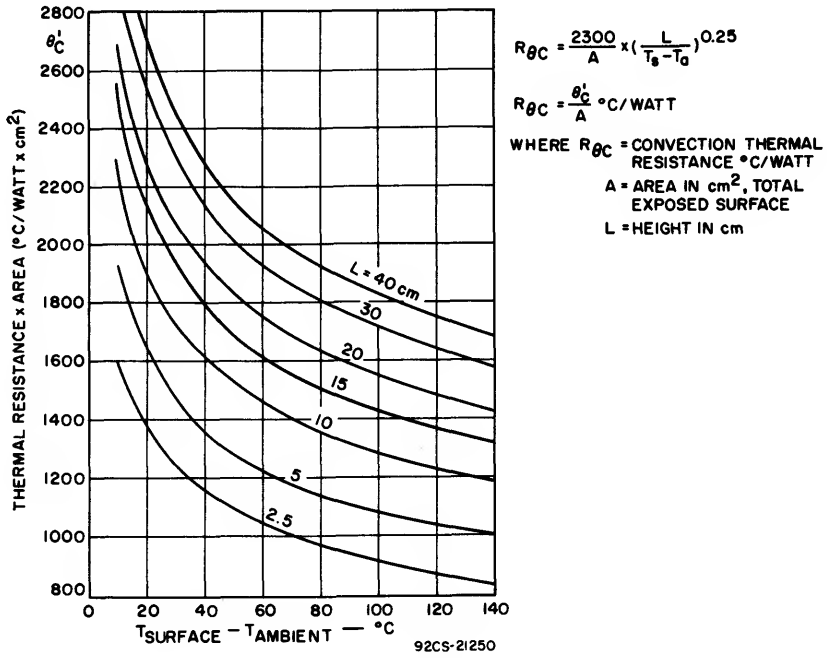


Fig. 44 - Convection thermal resistance as a function of temperature drop from the surface of the heat sink to free air for heat sinks of various heights. (Reprinted from Control Engineering, October 1956.)

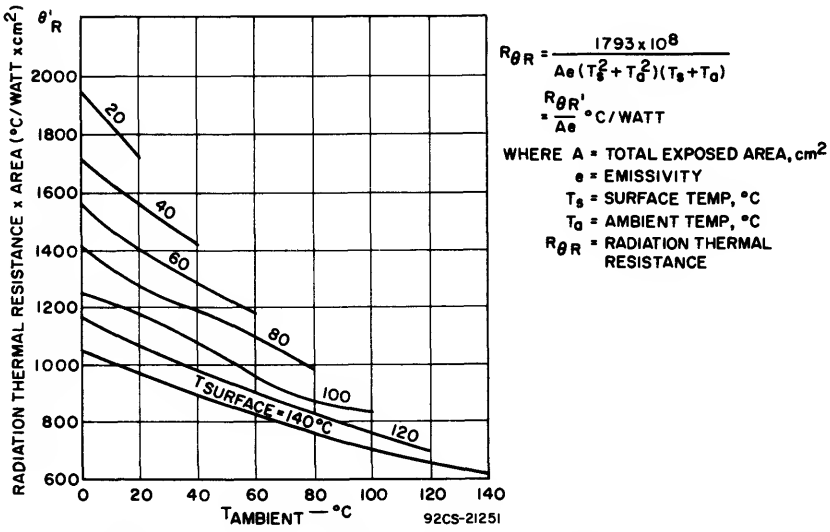


Fig. 45 - Radiation thermal resistance as a function of ambient temperature for various heat-sink surface temperatures. (Reprinted from Control Engineering, October 1956.)

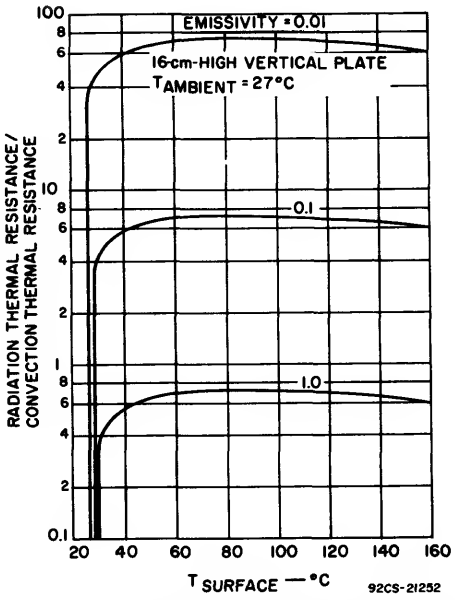


Fig. 46 - Ratio of radiation thermal resistance to convection thermal resistance as a function of heat-sink surface temperature for various surface emissivities. (Reprinted from Control Engineering, October 1967.)

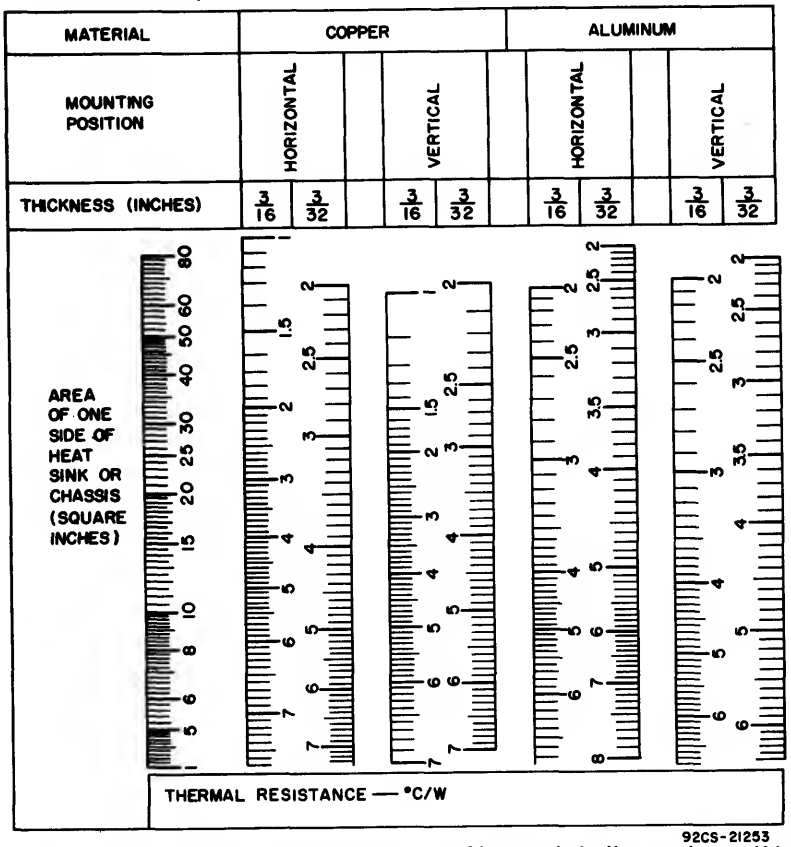


Fig. 47 - Thermal resistance as a function of heat-sink dimensions. (Nomograph reprinted from Electronic Design, August 16, 1961.)

Heat-Sink Performance

The performance that may be expected from a commercial heat sink is normally specified by the manufacturer, and the information supplied in the design curves shown in Figs. 44, 45, and 46 provides the basis for the design of flat vertical plates for use as heat sinks. In all cases, it must be remembered that the heat is dissipated from the heat sink by both convection and radiation. Although surface area is important in the design of vertical-plate heat sinks, other factors such as surface and ambient temperature, conductivity, emissivity, thickness, shape, and orientation must also be considered. An excessive temperature gradient can be avoided and the conduction thermal resistance in the heat sink can be minimized by use of a high-conductivity material, such as copper or aluminum, for the heat sink. Radiation losses are increased by an increase in surface emissivity. Best results are obtained when the heat sink has a black matte finish for which the emissivity is at least 0.9. When free-air convection is used for heat removal, a vertically mounted heat sink provides a thermal resistance that is approximately 30 per cent lower than that obtained with horizontal mounting.

In restricted areas, it may be necessary to use forced-convection cooling to reduce the effective thermal resistance of the heat sink. On the basis of the improved reliability of cooling fans, it can be shown that the over-all reliability of a system may actually be improved by use of forced-convection cooling because the number of components required is reduced.

Economic factors are also important in the selection of heat sinks. It is often more economical to use one heat sink with several properly placed transistors than to use individual heat sinks. It can be shown that the cooling efficiency increases and the unit cost decreases under such conditions.

Heat-Sink Insulators

As pointed out previously, when power transistors are to be mounted on heat sinks, some form of electrical isolation must be provided between the case and the heat sink. Unfortunately, however, good electrical insulators usually are also good thermal insulators. It is difficult, therefore, to provide electrical insulation without introduction of significant thermal resistance between case and heat sink. The best materials for this application are mica, beryllium oxide (Beryllia), and anodized aluminum. A comparison of the properties of these three materials for case-to-heat-sink isolation of the TO-3 package is shown in Table III. If the area of the seating plane, the thickness of the material, and the thermal conductivity are known, the case-to-heat-sink thermal resistance θ_{C-S} can be readily calculated by use of the following equation:

$$\theta_{cond} = d/4.186\ KA\ ^\circ C \text{ per watt}$$

where d is the length of the thermal path in centimeters, K is the thermal conductivity in cal/(sec) (cm) (° C), and A is the area perpendicular to the thermal path t in square centimeters. The number 4.186 is a conversion factor used to obtain the result in ° C per watt.

In all cases, this calculation should be experimentally verified. Irregularities in the bottom of the transistor seating plane or on the face of the heat sink or insulating washer may result in contact over only a very small area unless a filling compound is used. Although silicone grease has been used for years, recently newer compounds with zinc oxide fillers (e.g., Dow Corning #340 or Wakefield #120) have been found to be even more effective.

For small general-purpose transistors, such as the 2N2102, which use a JEDEC TO-5 package, a good method for thermal isolation of the collector from a metal chassis or

Table III - Comparison of Insulating Washers Used for Electrical Isolation of Transistor

TO-3 Case from Heat Sink			
Material	Thickness (inches)	θ_{C-S} (° C/W)	Capacitance (pF)
Mica	0.002	0.4	90
Anodized Aluminum	0.016	0.35	110
Beryllia	0.063	0.25	15

printed-circuit board is by means of a beryllium-oxide washer. The use of a zinc-oxide-filled silicone compound between the washer and the chassis, together with a moderate amount of pressure from the top of the transistor, helps to decrease thermal resistance. Fin-type heat sinks, which are commercially available, are also suitable, especially when transistors are mounted in Teflon sockets which provide no thermal conduction to the chassis or printed-circuit board. Fig. 48 illustrates both types of mounting.

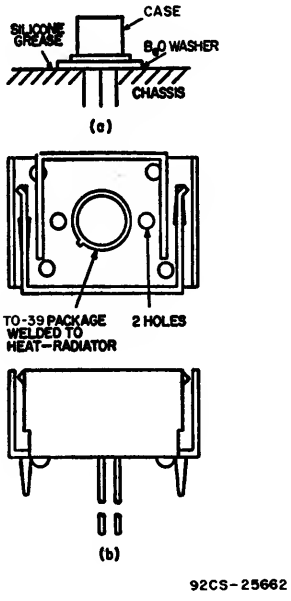


Fig. 48 - Suggested mounting arrangements for transistors having a JEDEC TO-5 package: (a) without heat sink; (b) with fin-type heat sink.

SECOND BREAKDOWN

A bipolar transistor operated at high power densities is subject to a failure mode termed "second breakdown" in which the emitter-collector voltage suddenly drops, usually 10 to 25 volts. Unless the power is rapidly removed, the transistor is destroyed or materially degraded by overheating. Second breakdown (S/b) is a thermal hot-spot formation within the transistor pellet. It has two phases of development. First is the constriction phase where, because of thermal regeneration, the current tends to concentrate in a small area. The second phase is the destruction phase. In this second phase, local temperatures and temperature gradients increase until they cause permanent device damage.

The constriction or regeneration phase of second breakdown may be initiated in any number of ways. One section of the emitter-base junction need only be higher in temperature than the others. Such a hot spot might be caused by resistive debiasing, divergent heat flow to the device heat sink, an inhomogeneity in the thermal path, or other irregularities or imperfections within the device. Once a slightly hotter emitter-base region is present, positive thermal feedback begins: the hot region injects more and therefore gets hotter. If the available power is limited or the effective thermal resistance of the hot spot is sufficiently low, the peak temperature remains below a critical temperature, and stable operation continues. When the peak temperature reaches a value such that local base-collector leakage currents reach base current magnitude, the device regenerates into second breakdown, often very rapidly.

Second breakdown may occur when the device operates with a forward-biased emitter-base junction or during the application of reverse bias. In the forward-biased form of second breakdown, shown in Fig. 49, the current $I_{s/b}$ above which the device switches into second breakdown is specified as part of the "safe-operating area" rating system developed by RCA for power transistors. (This system is explained later in this section.) Emitter

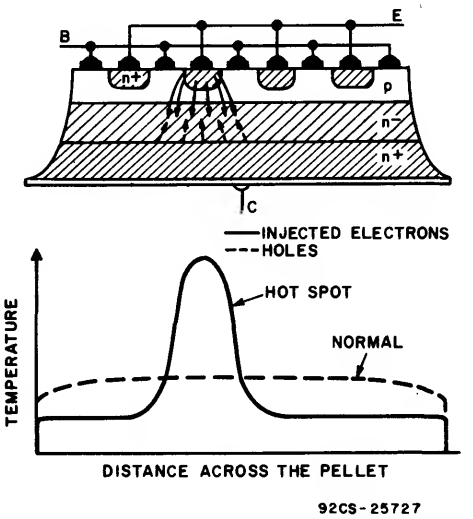


Fig. 49 - Forward-biased second breakdown.

and base resistive ballasting effectively increase forward-biased $I_{s/b}$ of a device. Emitter ballasting equalizes currents by inserting in each emitter region a voltage drop proportional to base current in the various base regions thus equalizing drive conditions within the device and maintaining uniformity. Thermal coupling between emitter regions may also be used to improve the forward biased $I_{s/b}$ performance of a transistor. This design approach tends to hold all regions of the emitter-base junction at the same temperature and same forward bias, thus maintaining uniform current flow.

Second breakdown is also observed when a transistor operating with an inductive load is turned off. Fig. 50 shows this form of second breakdown. When the emitter-base junction is

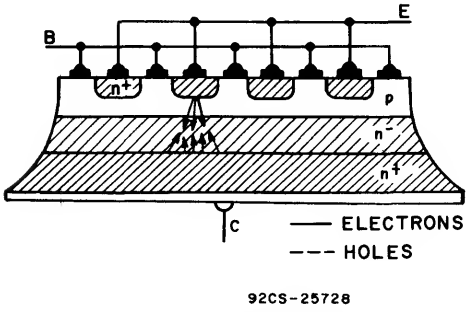


Fig. 50 - Reverse-biased second breakdown.

reverse biased, the edges of the emitters are quickly turned-off by the voltage drop caused by the reverse flow of the base current through the base resistance under the emitter. Collector current tends to be rapidly reduced; however, the inductive load responds to the decrease in collector current by driving the collector-emitter voltage to a value at which breakdown can occur in the collector-base space charge region $V_{(BR)CEX}$. The multiplied current resulting from the breakdown is focused towards the emitter centers, keeping the centers on for a longer time. When all center sections of the emitters behave alike, the power is dissipated uniformly by all emitters. If, however, a hot spot exists or develops, the energy stored in the load inductance is dumped into this region. The central region of this emitter rapidly rises in temperature, reaching a value where the hot spot sustains itself and second breakdown occurs. Emitter ballasting is not effective in protecting against reverse-biased second breakdown because the hogging portion of the emitter is fed internally from a current source, and this current source is insensitive to the relatively small differences in emitter potential: Ballasting against reverse-biased second breakdown is best done in the collector by the addition of a resistive layer which decreases the internal collector-emitter voltage in the affected region. The maximum energy that may be stored in the load inductance before second breakdown ($E_{s/b}$) is specified for most RCA power transistors intended for switching applications.

HIGH-VOLTAGE SURFACE EFFECTS

As the voltage ratings of a power transistor are increased, it becomes more difficult to achieve theoretical bulk breakdown values. Furthermore, both the breakdown voltage and junction leakage currents may vary under operating conditions. The problem is usually due to surface phenomena.

High-voltage transistors require large depletion widths in the base-collector junction. This requirement suggests that at least one side of the junction must be lightly doped. Fig. 51 shows what happens in a normal "mesa-type" device. The external fringing electrical fields terminate on the silicon and modify the depletion regions at the surface. If these fringing fields are large and configured as shown, a local high field condition is established at the surface and premature breakdown occurs. High-intensity fringing fields exist well outside the junction and contribute to the movement of ions external or internal to the applied passivation layers, leading to instabilities.

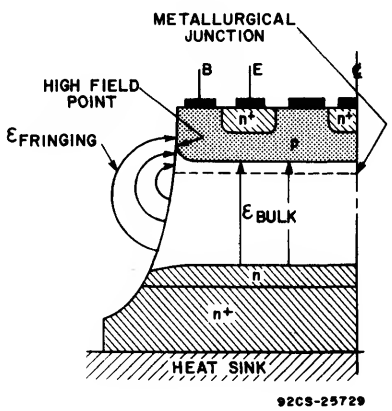


Fig. 51 - Electric field distribution in high-voltage "mesa" n-p-n transistor.

The state-of-the-art "cures" for these problems are: junction contouring to reduce the magnitude and the shape of the fringing fields; empirical determination of the proper surface etch and the optimum organic encapsulant; or glassing of the junctions to contain the fringing fields. The latter two solutions do not usually yield breakdown voltages equal to the bulk values, but they do lessen the surface instability.

To achieve breakdown voltages approaching the bulk values it is necessary that the fringing field be properly shaped, and once properly shaped it must be kept in this condition. Field electrodes are being investigated to accomplish this objective.

THERMAL-CYCLING RATINGS

A power transistor is often used in applications where the power in the device is cycled; the transistor is heated and cooled many times. Because the transistor is constructed of materials that have different thermal expansion coefficients, stress is placed on the chip, the metallurgical bond, and the heat spreader. If the stress is severe enough and sufficient cycles are encountered, the device fails. Usually the chip separates from the heat spreader or one of the contact connections opens. The stress is proportional to the size of the pellet, the temperature variation, elasticity of the connecting members, and the differences in thermal-expansion coefficients. Anything which concentrates the stress, such as voids in the mounting system, aggravates the condition.

The rate of degradation of a metallurgical bond under stressed conditions is also proportional to the average and peak temperature excursions of the bond. The failure-rate dependency of thermal fatigue and other phenomena can be as much as double for every 10°C increase in average and peak temperature. The most economical way to buy reliability in power transistor application is, therefore, to reduce these temperatures by careful consideration of heat flow during equipment design.

Several techniques are used to improve thermal-cycling capability within power transistors. One method is to mount the chip on a metal such as molybdenum, whose thermal expansion coefficient is similar to silicon, and to braze this metal to the package. In this way stresses are evenly distributed, as in a graded glass seal. Another method, applicable on units using the lead solder mounting technique, uses a controlled solder process in which the thickness and composition of the lead solder are carefully controlled at all times.

An equipment manufacturer should make certain that power-transistor circuits included in his systems are designed so that cyclic thermal stresses are mild enough to assure that no transistor fatigue failures will occur during the required operating life of his equipment.

RCA has developed a **thermal-cycling rating system** that relates the total power dissipation P_T and the change in case temperature ΔT_C to the total number of thermal cycles N that the transistor is rated to withstand.

Fig. 52 shows a typical **thermal-cycling rating chart** for a power transistor. This chart is provided in the form of a log-log presentation in which total transistor dissipation is denoted by the ordinate and the thermal-cycling capability (number of cycles to failure) is indicated by the abscissa. Rating curves are shown for various magnitudes of changes in

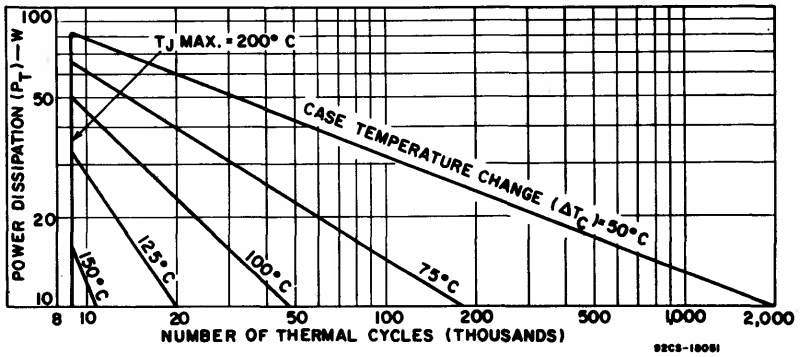


Fig. 52 - Thermal-cycling rating chart for an RCA hermetic power transistor.

case temperature. Use of the thermal-cycling rating charts makes it possible for a circuit designer to avoid transistor thermal-fatigue failures during the operating life of his equipment. In general, power dissipation is a fixed system requirement. The design can also readily determine the number of thermal cycles that a power transistor will be subjected to during the minimum required life of the equipment. For these conditions, the charts indicate the maximum allowable change in case temperature. If the rating point does not lie exactly on one of the rating curves, the allowable change in case temperature can be approximated by linear interpolation. The designer can then determine the minimum size of the heat sink required to restrict the change in case temperature within this maximum value.

RCA thermal-cycling ratings allow a circuit designer to use power transistors with assurance that thermal-fatigue failures of these devices will not occur during the minimum required life of his equipment. These ratings provide valid indications of the thermal-cycling capability of power transistors for all types of operating conditions.

SAFE-OPERATING-AREA RATINGS

During normal circuit operation, power transistors are often required to sustain high current and high voltage simultaneously. The capability of a transistor to withstand such conditions is normally shown by use of a safe-operating-area rating curve. This type of rating curve defines, for both steady-state and pulsed operation, the voltage-current boundaries that result from the combined limitations imposed by voltage and current ratings, the maximum allowable dissipation, and the second-breakdown ($I_{s/b}$) capabilities of the transistor.

If the safe-operating area of a power transistor is limited within any portion of the voltage-current characteristics by thermal factors (thermal impedance, maximum junction temperatures, or operating case temperature), this limiting is defined by a constant-power hyperbola ($I=KV^{-1}$) which can be represented on the log-log voltage-current curve by a straight line that has a slope of -1.

The energy level at which second breakdown occurs in a power transistor increases as the time duration of the applied voltage and current decreases. The power-handling capability of the transistor also increases with a decrease in pulse duration because thermal mass of the power-transistor chip and associated mounting hardware imparts an inherent thermal delay to a rise in junction temperature.

Fig. 53 shows a forward-bias safe-area rating chart for a typical silicon power transistor, the RCA-2N3585. The boundaries defined by the curves in the safe-area chart indicate, for both continuous-wave and nonrepetitive-pulse operation, the maximum current ratings, the maximum collector-to-emitter forward-bias avalanche breakdown-voltage rating [$V_{\alpha M}=1$, which is usually approximated by $V_{CEO(sus)}$], and the thermal and second-breakdown ratings of the transistors.

As shown in Fig. 53, the thermal (dissipation) limiting of the 2N3585 ceases when the collector-to-emitter voltage rises above 100 volts during dc operation. Beyond this point, the safe operating area of the transistor is limited by the second-breakdown ratings. During pulsed operation, the thermal limiting extends to higher values of collector-to-emitter voltage before the second-breakdown region is reached, and as the pulse duration decreases, the thermal-limited region increases.

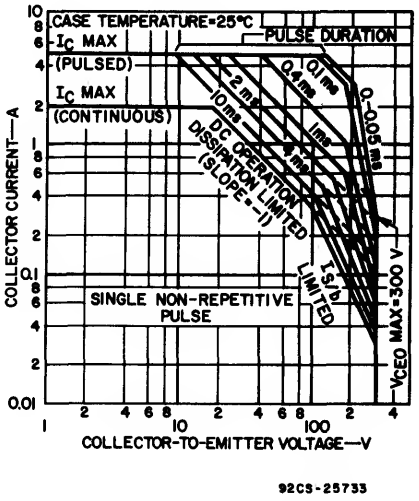


Fig. 53 - Safe-area rating chart for the RCA-2N3585 silicon power transistor.

If a transistor is to be operated at a pulse duration that differs from those shown on the safe-area chart, the boundaries provided by the safe-area curve for the next higher pulse duration must be used, or the transistor manufacturer should be consulted. Moreover,

as indicated in Fig. 53, safe-area ratings are normally given for single nonrepetitive pulse operation at a case temperature of 25° C and must be derated for operation at higher case temperatures and under repetitive-pulse or continuous-wave conditions.

Fig. 54 shows temperature derating curves for the 2N3585 safe-area chart of Fig. 53. These curves show that thermal ratings are affected far more by increases in case temperature than are second-breakdown ratings. The thermal (dissipation-limited) derating curve decreases linearly to zero at the maximum junction temperature of the transistor [T_J(max)= 200° C]. The second-breakdown ($I_{s/b}$-limited) temperature derating curve, however, is less severe because the increase in the formation of the high current concentrations that cause second breakdown is less than the increase in dissipation factors as the temperature increases.

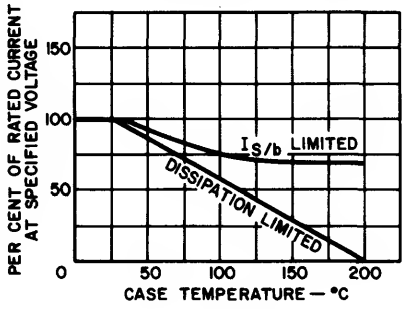


Fig. 54 - Safe-area temperature-derating curves for the RCA-2N3585 silicon power transistor.

Because the thermal and second-breakdown deratings are different, it may be necessary to use both curves to determine the proper derating factor for a voltage-current point that occurs near the breakpoint of the thermal-limited and second-breakdown-limited regions on the safe-area curve. For this condition, a derating factor is read from each derating curve. For one of the readings, however, either the thermal-limited section of the safe-area curve must be extrapolated upward in voltage or the second-breakdown-limited section must be extrapolated downward in voltage, depending upon which side of the voltage breakpoint the voltage-current point is located. The smaller of the collector-current values obtained from the thermal and second-breakdown deratings must be used as the safe rating.

For pulsed operation, the derating factor shown in Fig. 54 must be applied to the appropriate curve on the safe-area rating chart. For the derating, the effective case temperature T_C(eff) may be approximated by the average junction temperature T_J(av). The average junction temperature is determined as follows:

$$T_J(av)=T_C+P_{AV}(\theta_{J-C})$$

This approach results in a conservative rating for the pulsed capability of the transistor. A more accurate determination can be made by computation of actual instantaneous junction temperatures. (For more detailed information on safe-area ratings and temperature derating the reader should refer to the **RCA Power Circuits Designer's Handbook**, Technical Series SP-52.

BASIC TRANSISTOR CHARACTERISTICS

The term "characteristic" is used to identify the distinguishing electrical features and values of a transistor. These values may be shown in curve form or they may be tabulated. When the characteristics values are given in curve form, the curves may be used for the determination of transistor performance and the calculation of additional transistor parameters.

Characteristics values are obtained from electrical measurements of transistors in various circuits under certain definite conditions of current and voltage. **Static characteristics** are obtained with dc potentials applied to the transistor electrodes. **Dynamic characteristics** are obtained with an ac voltage on one electrode under various conditions of dc potentials on all the electrodes. The dynamic characteristics, therefore, are indicative of the performance capabilities of the transistor under actual working conditions.

Current-Voltage Relationships

The currents in a transistor are directly related to the movement of minority carriers in the base region that results from the application of voltages of the proper polarities to the emitter-base and collector-base junctions. A definite mutual relationship exists between the transistor currents and the voltages applied to the transistor terminals. Graphical representations of the variations in transistor currents with the applied voltages provide an excellent indication of the operation of a

transistor under different biasing conditions. Transistor manufacturers usually provide curves of current-voltage characteristics to define the operating characteristics of their devices. Such curves are provided for either common-emitter or common-base transistor connections. Fig. 55 shows the bias-voltage polarities and the current components for both common-emitter and common-base connections of a p-n-p transistor. For an n-p-n transistor, the polarities of the voltages and the directions of the currents are reversed.

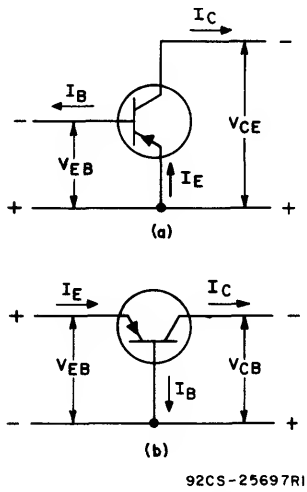


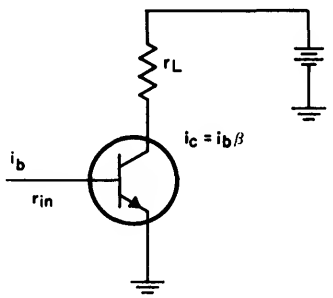
Fig. 55 - Transistor bias-voltage polarities and current components for (a) the common-emitter connection and (b) the common-base connection.

The common-emitter connection, shown in Fig. 55(a), is the more widely used in practical applications. In this connection, the emitter is the common point between the input (base) and output (collector) circuits, and large current gains are realized by use of a small base current to control a much larger emitter-to-collector current. The common-base connection, shown in Fig. 55(b), differs from the common-emitter connection in that the voltages applied to the transistor are referred to the base rather than to the emitter.

Published data for transistors include both electrode characteristic curves and transfer characteristic curves. These curves present the same information, but in two different forms to provide more useful data. Because transistors are used most often in the common-emitter configuration, characteristic curves are usually shown for the collector or output electrode. The **collector-characteristic curve** is obtained by varying collector-to-emitter voltage and measuring collector current for different values of base current. The **transfer-characteristic curve** is obtained by varying the base-to-emitter (bias) voltage or current at a specified or constant collector voltage, and measuring collector current.

Current-Gain Parameters

Power gain in transistor circuits is usually obtained by use of a small control signal to produce larger signal variations in the output current. The gain parameter most often specified is the current gain (β) from the base to the collector. The power gain of a transistor operated in a common-emitter configuration is equal to the square of the current gain β times the ratio of the load resistance r_L to the input resistance r_{in}, as indicated in Fig. 56.



INPUT CURRENT $= i_b$
INPUT VOLTAGE $= i_b\, r_{in}$
OUTPUT CURRENT $= i_c = i_b\beta$
OUTPUT VOLTAGE $= i_c r_L = i_b\beta r_L$
INPUT POWER $= i_b^2\, r_{in}$
OUTPUT POWER $= i_c^2\, r_L = i_b^2\, \beta^2\, r_L$
POWER GAIN $=$ *power output/power input*
$= i_b^2\beta^2 r_L / i_b^2 r_{in}$
$= \beta^2 r_L / r_{in}$

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Fig. 56 - Test circuit and simplified power-gain calculation for a transistor operated in a common-emitter configuration.

Although the input resistance r_{in} affects the power gain, as shown by the equations given in Fig. 56, this parameter is not usually specified directly in the published data on transistors because of the large number of

components of which it is comprised. In general, the input impedance is expressed as a maximum base-to-emitter voltage V_{BE} under specified input-current conditions.

A measure of the current gain of a transistor is its **forward current-transfer ratio**, i.e., the ratio of the current in the output electrode to the current in the input electrode. Because of the different ways in which transistors may be connected in circuits, the forward current-transfer ratio is specified for a particular circuit configuration.

The current gain (or current transfer ratio) of a transistor is expressed by many symbols; the following are some of the most common, together with their particular shades of meaning:

1. beta (β)—general term for current gain from base to collector (i.e., common-emitter current gain)
2. alpha (α)—general term for current gain from emitter to collector (i.e., common-base current gain)
3. h_{fe}—ac gain from base to collector (i.e., ac beta)
4. h_{FE}—dc gain from base to collector. (i.e., dc beta)

Common-base current gain, α, is the ratio of collector current to emitter current (i.e., $\alpha = I_C / I_E$). Although α is slightly less than unity, circuit gain is realized as a result of the large differences of input (emitter-base) and output (collector-base) impedances. The input impedance is small because the emitter-base junction is forward-biased, and the output impedance is large because the collector-base junction is reverse-biased.

Common-emitter current gain, β, is the ratio of collector current to base current (i.e., $\beta = I_C / I_B$). Useful values of β are normally greater than ten.

Transconductance

Extrinsic transconductance may be defined as the quotient of a small change in collector current divided by the small change in emitter-to-base voltage producing it, under the condition that other voltages remain unchanged. Thus, if an emitter-to-base voltage change of 0.1 volt causes a collector-current change of 3 milliamperes (0.003 ampere) with other voltages constant, the transconductance is 0.003 divided by 0.1, or 0.03 mho. (A "mho" is the unit of conductance, and was named by spelling "ohm" backward.) For convenience, a millionth of a mho, or a micromho (μmho), is used to express transconductance. Thus, in the example, 0.03 mho is 30,000 micromhos.

Cutoff Frequencies

For all transistors, there is a frequency f at which the output signal cannot properly follow the input signal because of time delays in the transport of the charge carriers. The three principal cut-off frequencies, shown in Fig. 57, may be defined as follows:

1. The **base cut-off frequency** $f_{\alpha b}$ is that frequency at which alpha (α) is down 3 dB from the low-frequency value.
2. The **emitter cut-off frequency** $f_{\alpha e}$ is that frequency at which beta (β) is down 3 dB from the low-frequency value.
3. The frequency f_T is that frequency at which beta theoretically decreases to unity (i.e., 0-dB gain) with a theoretical 6-dB-per-octave fall off. This term, which is a useful figure of merit for transistors, is referred to as the **gain-bandwidth product**.

The gain-bandwidth product f_T is the term that is generally used to indicate the high-frequency capability of a transistor. Other parameters that critically affect high-frequency

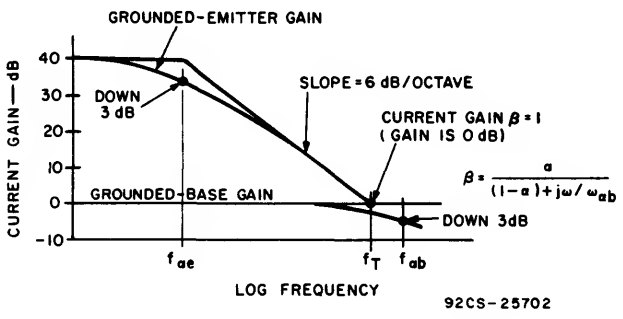

Fig. 57 - Cut-off frequencies.

performance are the capacitance or resistance which shunts the load and the input impedance, the effect of which is shown by the equations given in Fig. 56.

The base and emitter cut-off frequencies and the gain-bandwidth product of a transistor provide an approximate indication of the useful frequency range of the device, and help to determine the most suitable circuit configuration for a particular application.

The specification of all the characteristics which affect high-frequency performance is so complex that often a manufacturer does not specify all the parameters, but instead specifies transistor performance in a specific amplifier circuit. This information is very useful when the transistor is operated under conditions very similar to those of the test circuit, but is difficult to apply when the transistor is used in a widely different application. Some manufacturers also specify transistor performance characteristics as a function of frequency, which alleviates these problems.

Cutoff Currents

Cutoff currents are small steady-state reverse currents which flow when a transistor is biased into non-conduction. They consist of **leakage currents**, which are related to the surface characteristics of the semiconductor material, and **saturation currents**, which are related to the impurity concentration in the material and which increase with increasing temperatures. Collector-cutoff current is the steady-state current which flows in the reverse-biased collector-to-base circuit when the emitter-to-base circuit is open. Emitter-cutoff current is the current which flows in the reverse-biased emitter-to-base circuit when the collector-to-base circuit is open.

In the common-base configuration, the collector reverse (leakage) current, I_{CBO}, is measured with the emitter circuit open. The presence of the second junction, however, still affects the level of the current because the emitter acquires a small negative bias when it is open-circuited. This bias reduces the hole gradient at the collector and causes the reverse current to decrease. This current, therefore, is much smaller with the emitter open than it is when the emitter-base junction is short-circuited.

The reverse current increases with collector voltage, and may lead to avalanche breakdown at high voltages.

The common-emitter reverse collector current I_{CEO}, measured with zero input current (I_B=0 in this case), is very much larger than the reverse collector current I_{CBO} in the common-base connection. When the base current is zero, the emitter current adjusts itself so that the losses in the hole-injection and diffusion mechanisms are exactly balanced by the supply of excess electrons left in the vicinity of the collector by hole extraction. For this condition, the collector current is equal to the emitter current.

The common-emitter reverse collector current I_{CEO} increases with collector voltage, unlike the common-base reverse collector current I_{CBO}. This behavior is another consequence of the variation in the effective base width with collector voltage. The narrower the effective base region, the more efficient is the transfer of current from emitter to collector. The more efficient base transport with the higher collector voltage permits a higher emitter current to flow before the losses are again balanced by the supply of electrons from the vicinity of the collector.

Breakdown Voltages

Transistor breakdown voltages define the voltage values between two specified electrodes at which the crystal structure changes and current begins to rise rapidly. The voltage then remains relatively constant over a wide range of electrode currents. Breakdown voltages may be measured with the third electrode open, shorted, or biased in either the forward or the reverse direction. For example, Fig. 58 shows a series of collector-characteristic curves for different base-bias conditions. It can be seen that the collector-to-emitter breakdown voltage increases as the base-to-emitter bias decreases from the normal forward values through zero to reverse values. The symbols shown on the abscissa are sometimes used to designate collector-to-emitter breakdown voltages with the base open $V_{(BR)CEO}$, with external base-to-emitter resistance $V_{(BR)CER}$, with the base shorted to the emitter $V_{(BR)CES}$, and with a reverse base-to-emitter voltage $V_{(BR)CEV}$.

As the resistance in the base-to-emitter circuit decreases, the collector characteristic develops two breakdown points, as shown in Fig. 58. After the initial breakdown, the collector-to-emitter voltage decreases with increasing collector current until another breakdown occurs at a lower voltage. This

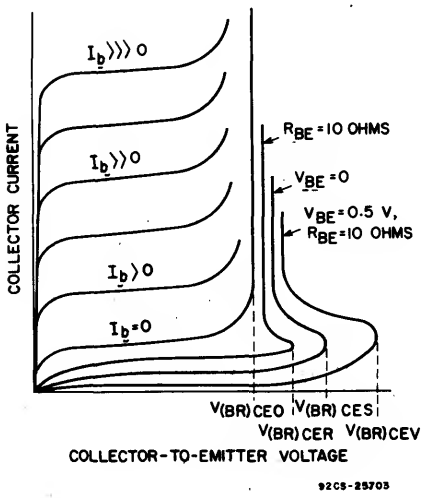

Fig. 58 - Typical collector-characteristic curves showing locations of various breakdown voltages.

minimum collector-to-emitter breakdown voltage is called the **sustaining voltage**.

Punch-Through Voltage

Punch-through (or reach-through) voltage defines the voltage value at which the depletion region in the collector region passes completely through the base region and makes contact at some point with the emitter region. This "reach-through" phenomenon results in a relatively low-resistance path between the emitter and the collector, and causes a sharp increase in current. Punch-through voltage does not result in permanent damage to a transistor, provided there is sufficient impedance in the power-supply source to limit transistor dissipation to safe values.

Saturation Voltage

The curves at the left of Fig. 58 show typical collector characteristics under normal forward-bias conditions. For a given base input current, the collector-to-emitter saturation voltage is the minimum voltage required to maintain the transistor in full conduction (i.e., in the saturation region). Under saturation conditions, a further increase in forward bias produces no corresponding increase in collector current. Saturation voltages are very important in switching applications, and are usually specified for several conditions of electrode currents and ambient temperatures.

Effect of Temperature on Transistor Characteristics

The characteristics of transistors vary with changes in temperature. In view of the fact that most circuits operate over a wide range of environments, a good circuit design should compensate for such changes so that operation is not adversely affected by the temperature dependence of the transistors.

Current Gain—The effect of temperature on the gain of a silicon transistor is dependent upon the level of the collector current, as shown in Fig. 59. At the lower current levels, the current-gain parameter h_{FE} increases with temperature. At higher currents, however, h_{FE} may increase or decrease with a rise in temperature because it is a complex function of many components.

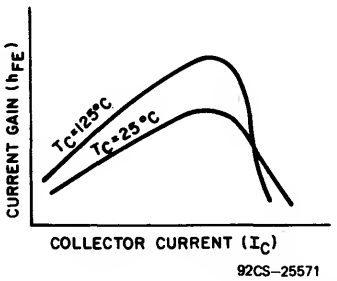

Fig. 59 - Current gain as a function of collector current at different temperatures.

Base-to-Emitter Voltage—Fig. 60 shows the effect of changes in temperature on the base-to-emitter voltage (V_{BE}) of silicon transistors. As indicated, the base-to-emitter voltage diminishes with a rise in temperature for low values of collector current, but tends to increase with a rise in temperature for higher values of collector current.

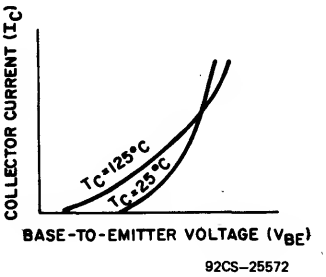

Fig. 60 - Collector current as a function of base-to-emitter voltage at different temperatures.

Collector-to-Emitter Saturation Voltage—The collector-to-emitter saturation voltage ($V_{CE}(sat)$) is affected primarily by collector resistivity (ρc) and the amount by which the natural gain of the device (h_{FE}) exceeds the gain with which the circuit drives the device into saturation. This latter gain is known as the forced gain (h_{FEf}).

At lower collector currents, the natural h_{FE} of a transistor increases with temperature, and the IR drop in the transistor is small. The collector-to-emitter saturation voltage, therefore, diminishes with increasing temperature if the circuit continues to maintain the same forced gain. At higher collector currents, however, the IR drop increases, and gain may decrease. This decrease in gain causes the collector-to-emitter saturation voltage to increase and possibly to exceed the room-temperature (25°C) value. Fig. 61 shows the effect of temperature on the collector-to-emitter saturation voltage.

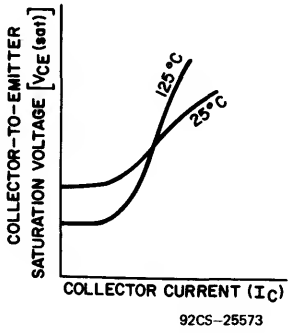

Fig. 61 - Collector current as a function of collector-to-emitter saturation voltage at different temperatures.

Collector Leakage Currents—Reverse collector current I_R is a resultant of three components, as shown by the following equation:

$$I_R = I_D + I_G + I_S$$

Fig. 62 shows the variations of these components with temperature.

Leakage currents are important because they affect biasing in amplifier applications and represent the off condition for transistors used in switching applications. The symbol I_R used in the preceding discussion represents any of several different leakage currents commonly specified by transistor manufacturers. The most basic specification is I_{CBO}, which indicates the leakage from collector to

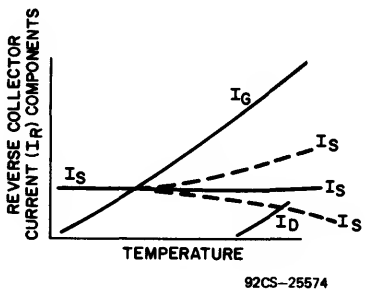

Fig. 62 - Reverse collector current as a function of temperature.

base with the emitter open. This leakage is simply the reverse current of the collector-to-base diode.

In addition to the I_{CBO} value, I_{CEV}, I_{CEO}, and I_{CER} specifications are often given for transistors. I_{CEV} is the leakage from the collector to emitter with the base-emitter junction reverse-biased. I_{CER} is the leakage current from the collector to the emitter with the base and emitter connected by a specified resistance, I_{CEO} is the leakage current from collector to emitter with the base open. I_{CEV} differs from I_{CBO} only very slightly and in most transistors the two parameters can be considered equal. (This equality is not maintained in symmetrical transistors.) I_{CEO} is simply the product of I_{CBO} at the voltage specified and the h_{FE} of the transistor at a base current equal to I_{CBO}. I_{CEO} is of course the largest leakage current normally specified. I_{CER} is intermediate in value between I_{CEV} and I_{CEO}.

POWER TRANSISTORS IN SWITCHING SERVICE

An important application of power transistors is power switching. Large amounts of power, at high currents and voltages, can be switched with small losses by use of a power transistor that is alternatively driven from cutoff to saturation by means of a base control signal. The two most important considerations in such switching applications are the speed at which the transistor can change states between saturation and cutoff and the power dissipation.

Transistor switching applications are usually characterized by large-signal nonlinear operation of the devices. The switching transistor is generally required to operate in either of two states: on or off. In transistor switching circuits, the common-emitter configuration is by far the most widely used.

Typical output characteristics for an n-p-n transistor in the common-emitter configuration are shown in Fig. 63. These characteristics are divided into three regions of operation, i.e., cutoff region, active region, and saturation region.

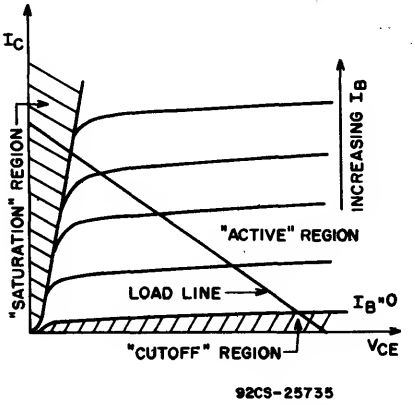

Fig. 63 - Typical collector characteristic of an n-p-n transistor showing three principal regions involved in switching.

In the cutoff region, both the emitter-base and collector-base junctions are reverse-biased. Under these conditions, the collector current is very small, and is comparable in magnitude to the leakage current I_{CEO}, I_{CEV}, or I_{CBO}, depending on the type of base-emitter biasing used.

Fig. 64 is a sketch of the minority-carrier concentration in an n-p-n transistor. For the cutoff condition, the concentration is zero at both junctions because both junctions are reverse-biased, as shown by curve 1 in Fig. 64.

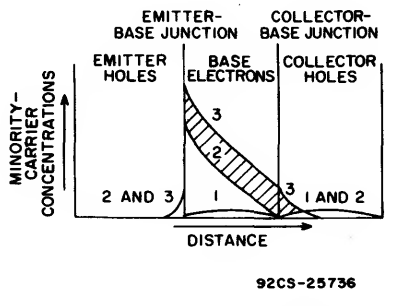

Fig. 64 - Minority-carrier concentrations in an n-p-n transistor: (1) in cutoff region, (2) in active region at edge of saturation region, (3) in saturation region.

In the active region, the emitter-base junction is forward-biased and the collector-base junction is reverse-biased. Switching from the cutoff region to the active region is accomplished along a load line, as indicated in Fig. 63. The speed of transition through the active region is a function of the frequency-response characteristics of the device. The minority-carrier concentration for the active region is shown by curve 2 in Fig. 64.

The remaining region of operation is the saturation region. In this region, the emitter-base and collector-base junctions are both forward-biased. Because the forward voltage drop across the emitter-base junction under this condition [$V_{BE}(sat)$] is greater than that across the collector-base junction, there is a net collector-to-emitter voltage referred to as $V_{CE}(sat)$. It is evident that any series-resistance effects of the emitter and collector also enter into determining $V_{CE}(sat)$. Because the collector is now forward-biased, additional carriers are injected into the base, and some into the collector. This minority-carrier concentration is shown by curve 3 in Fig. 64.

A basic saturated-transistor switching circuit is shown in Fig. 65. The voltage and current

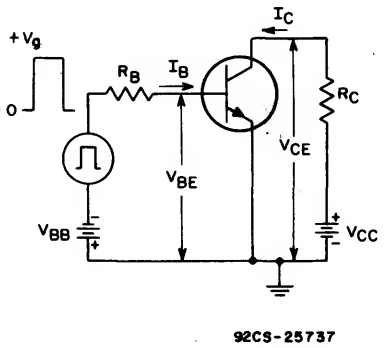

Fig. 65 - Basic saturated transistor switching circuit.

waveforms for this circuit under typical base-drive conditions are shown in Fig. 66. Prior to the application of the positive-going input pulse, the emitter-base junction is reverse-biased by a voltage $-V_{BE}(off)=V_{BB}$. Because the transistor is in the cutoff region, the base current I_B is the reverse leakage current I_{BEV}, which is negligible compared with I_{B1}, and the collector current I_C is the reverse leakage current I_{CEV}, which is negligible compared with V_{CC}/R_C.

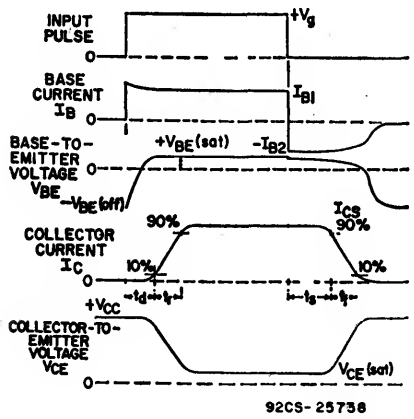

Fig. 66 - Voltage and current waveforms for saturated switching circuit shown in Fig. 65.

When the positive-going input pulse V_g is applied, the base current I_B immediately goes positive. The collector current, however, does not begin to increase until some time later. This delay in the flow of collector current (t_d) results because the emitter and collector capacitances do not allow the emitter-base junction to become forward-biased instantaneously. These capacitances must be charged from their original negative potential [$-V_{BE(off)}$] to a forward bias sufficient to cause the transistor to conduct appreciably. After the emitter-base junction is sufficiently forward-biased, there is an additional delay caused by the time required for minority carriers which are injected into the base to diffuse across the base and be collected at the collector. This delay is usually negligible compared with the delay introduced by the capacitive component. The collector and emitter capacitances vary with the collector-base and emitter-base junction voltages, and increase as the voltage V_{BE} goes positive. An accurate determination of total delay time, therefore, requries knowledge of the nonlinear characteristics of these capacitances.

When the collector current I_C begins to increase, the transistor has made the transition from the cutoff region into the active region. The collector current takes a finite time to reach its final value. This time, called rise time (t_r), is determined by the gain-bandwidth product (f_T), the collector-to-emitter capacitance (C_C), and the static forward current-transfer ratio (h_{FE}) of the transistor. At high collector currents and/or low collector voltages, the effect of this capacitance on rise time is negligible, and the rise time of collector current is inversely proportional to f_T. At low currents and/or high voltages, the effect of gain-bandwidth product is negligible, and the rise time of collector current is directly proportional to the product R_CC_C. At intermediate currents and voltages, the rise time is proportional to the sum ($\frac{1}{2}\pi f_T$) + R_CC_C. Under any of the above conditions, the collector current responds exponentially to a step of base current. If a turn-on base current (I_{B1}) is applied to the device, and the product $I_{B1}h_{FE}$ is less than V_{CC}/R_C, the collector current rises exponentially until it reaches the steady-state value $I_{B1}h_{FE}$. If $I_{B1}h_{FE}$ is greater than V_{CC}/R_C, the collector current rises toward the value $I_{B1}h_{FE}$. The transistor becomes saturated when I_C reaches the value I_{CS}($\approx V_{CC}/R_C$). At this point, I_C is effectively clamped at the value V_{CC}/R_C.

The rise time, therefore, depends on an exponential function of the ratio I_{CS}/I_{B1}:h_{FE}. Because the values of h_{FE}, f_T, and C_C are not constant, but vary with collector voltage and current as the transistor is switching, the rise time as well as the delay time is dependent on nonlinear transistor characteristics.

After the collector current of the transistor has reached a steady-state value I_{CS}, the minority-charge distribution is that shown by curve 3 in Fig. 66. When the transistor is turned off by returning the input pulse to zero, the collector current does not change immediately. This delay is caused by the excess charge in the base and collector regions, which tends to maintain the collector current at the I_{CS} value until this charge decays to an amount equal to that in the active region at the edge of saturation (curve 2 in Fig. 66). The time required for this charge to decay is called the storage time (t_S). The rate of charge decay is determined by the minority-carrier lifetime in the base and collector regions, on the amount of reverse "turn-off" base current (I_{B2}), and on the overdrive "turn-on" current (I_{B1}) which determined how deeply the transistor was driven into saturation. (In non-saturated switching, there is no excess charge in the base region, so that storage time is negligible.)

When the stored charge (Q_S) has decayed to the point where it is equal to that at the edge of saturation, the transistor again enters the active region and the collector current begins

to decrease. This fall-time portion of the collector-current characteristic is similar to the rise-time portion because the transistor is again in the active region. The fall time, however, depends on I_{B2}, whereas the rise time was dependent on I_{B1}. Fall time, like rise time, also depends on f_T and C_C.

The approximate values of I_{B1}, I_{B2}, and I_{CS} for the circuit shown in Fig. 65 are given by:

$$I_{B1} = \frac{V_G - V_{BB} - V_{BE}(sat)}{R_B}$$

$$I_{B2} = \frac{V_{BB} + V_{BE}(sat)}{R_B}$$

$$I_{CS} = \frac{V_{CC} - V_{CE}(sat)}{R_C}$$

Switching Characteristics

The electrical characteristics for a switching transistor, in general, differ from that for a linear-amplifier type of transistor in several respects. The static forward current-transfer ratio h_{FE} and the saturation voltages $V_{CE}(sat)$ and $V_{BE}(sat)$ are of fundamental importance in a switching transistor. The static forward current-transfer ratio determines the maximum amount of current amplification that can be achieved in any given circuit, saturated or non-saturated. The saturation voltages are necessary for the proper dc design of saturated circuits. Consequently, h_{FE} is always specified for a switching transistor, generally at two or more values of collector current. $V_{CE}(sat)$ and $V_{BE}(sat)$ are specified at one or more current levels for saturated transistor applications. Control of these three characteristics determines the performance of a given transistor type over a broad range of operating conditions. For non-saturated applications, $V_{CE}(sat)$ and $V_{BE}(sat)$ need not be specified. For such applications, it is important to specify V_{BE} at specific values of collector current and collector-to-emitter voltage in the active region.

Because the collector and emitter capacitances and the gain-bandwidth product influence switching time, these characteristics are specified for most switching transistors. The collector-base and emitter-base junction capacitances are usually measured at some value of reverse bias and are designated C_{ob} and C_{ib}, respectively. The gain-bandwidth product (f_T) of the transistor is the frequency at which the small-signal forward current-transfer ratio (h_{fe}) is unity. Because this characteristic falls off at 6 dB per octave above the corner frequency, f_T is usually controlled by specifying the h_{fe} at a fixed frequency anywhere from 1/2 to 1/10 f_T. Because C_{ob}, C_{ib}, and f_T vary nonlinearly over the operating range, these characteristics are generally more useful as figures of merit than as controls for determining switching speeds. When the switching speeds in a particular application are of major importance, it is preferable to specify the required switching speeds in the desired switching circuit rather than C_{ob}, C_{ib}, and f_T.

The storage time (t_S) of a transistor is dependent on the stored charge (Q_S) and on the driving current employed to switch the transistor between cutoff and saturation. Consequently, either the stored charge or the storage time under heavy overdrive conditions should be specified. Most recent transistor specifications require that storage time be specified.

Because of the dependence of the switching times on current and voltage levels, these times are determined by the voltages and currents employed in circuit operation.

Dissipation, Current, and Voltage Ratings

Up to this point, no mention has been made of dissipation, current, and voltage ratings for a switching transistor. The maximum continuous ratings for dissipation and current are determined in the same manner as for any other transistor. In a switching application, however, the peak dissipation and current may be permitted to exceed these continuous ratings depending on the pulse duration, on the duty factor, and on the thermal time constant of the transistor.

Voltage ratings for switching transistors are more complicated. In the basic switching circuit shown in Fig. 65, three breakdown voltages must be considered. When the transistor is turned off, the emitter-base junction is reverse-biased by the voltage $V_{BE}(off)$, (i.e., V_{BB}), the collector-base junction by $V_{CC}+V_{BB}$, and the emitter-to-collector junction by $+V_{CC}$. To assure that none of the voltage ratings for the transistor is exceeded under "off" conditions, the following requirements must be met:

The minimum emitter-to-base breakdown voltage $V_{(BR)EBO}$ must be greater than $V_{BE}(off)$.

The minimum collector-to-base breakdown voltage $V_{(BR)CBO}$ must be greater than $V_{CC}+V_{BE(off)}$.

The minimum collector-to-emitter breakdown voltage $V_{(BR)CERL}$ must be greater than V_{CC}.

$V_{(BR)EBO}$ and $V_{(BR)CBO}$ are always specified for a switching transistor. The collector-to-emitter breakdown voltage $V_{(BR)CEO}$ is usually specified under open-base conditions. The breakdown voltage $V_{(BR)CERL}$ (the subscript "RL" indicates a resistive load in the collector circuit) is generally higher than $V_{(BR)CEO}$. The requirement that $V_{(BR)CEO}$ be greater than V_{CC} is overly pessimistic. The requirement that $V_{(BR)CERL}$ be greater than V_{CC} should be used wherever applicable.

Coupled with the breakdown voltages are the collector-to-emitter and base-to-emitter transistor leakage currents. These leakage currents (I_{CEV} and I_{BEV}) are particularly important considerations at high operating temperatures. The subscript "V" in these symbols indicates that these leakage currents are specified at a given emitter-to-base voltage (either forward or reverse). In the basic circuit of Fig. 65, these currents are determined by the following conditions:

$$\left.\begin{matrix} I_{CEV} \\ I_{BEV} \end{matrix}\right\} \quad V_{CE} = V_{CC}$$

$$\left.\begin{matrix} I_{CEV} \\ I_{BEV} \end{matrix}\right\} \quad V_{BE} = V_{BE(off)} = -V_{BB}$$

In a switching transistor, these leakage currents are usually controlled not only at room temperature, but also at some higher operating temperature near the upper operational limit of the transistor.

Inductive Switching

Most inductive switching circuits can be represented by the basic equivalent circuit shown in Fig. 67. This type of circuit requires a rapid transfer of energy from the switched inductance to the switching mechanism, which may be a relay, a transistor, a commutating diode, or some other device. Often an accurate calculation of the energy to be dissipated in the switching device is required, particularly if that device is a transistor. If the supply voltage is low compared to the sustaining breakdown

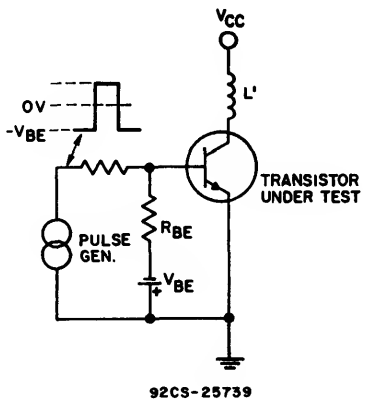

Fig. 67 - Basic equivalent circuit for inductive switching circuit.

voltage of the transistor and if the series resistance of the inductor can be ignored, then the energy to be dissipated is $\frac{1}{2} LI^2$. This type of rating for a transistor is called "reverse-bias second breakdown." The energy capability of a transistor varies with the load inductance and base-emitter reverse bias. A typical set of ratings which now appears in RCA published data is shown in Fig. 68.

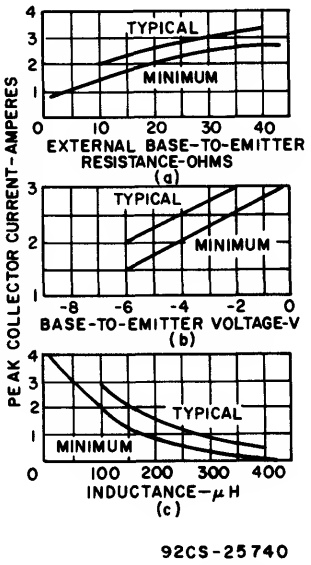

Fig. 68 - Typical reverse-bias second-breakdown ($E_{S/b}$) rating curves.